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LX7180A

4A Step-Down Regulator
Production Datasheet

Description

The LX7180A is a 4A step-down regulator with integrated MOSFETs packaged in a space saving QFN12 2mm x 2mm for today's mobile devices. It uses an ultra fast, constant frequency hysteretic control method to minimize external filter components while maintaining excellent regulation. The LX7180A reference voltage is programmable from 0.6V to 1.195V through a high speed (up to 3.4MHz), bi-directional I^2C bus.

The LX7180 operates from 3V to 5.5V rails and outputs 0.6V to 100% of the input voltage.

Cycle-by-cycle current limiting protects against over-current conditions. Hiccup mode provides protection for heavy over-load or short-circuit faults. Thermal protection shuts down the regulator under over-temperature conditions. Over voltage conditions will immediately shut off the output to protect against permanent damage. The LX7180A automatically restarts when all fault conditions are cleared.

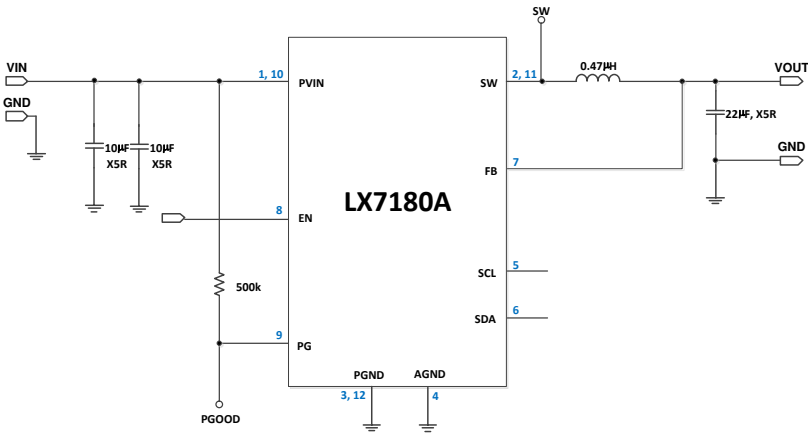

Figure 1: Typical Application

Features

- 0-4A Step-down Regulator
- Operational Input Supply Voltage Range: 3.0V-5.5V (short durations to 6.5V)
- Hysteretic Control Offers Best Transient Response
- PWM Switching at a Constant 1.65MHz
- Power Save Mode (PSM) can be Selected to Improve Light Load Efficiency.
- 100% duty ratio operation
- Input Under Voltage and Over Voltage Protection
- Enable and Power Good Function
- I^2C Serial Interface at 3.4Mbps
- Internal soft-start
- Cycle-by-Cycle Over Current Protection
- Hiccup Mode Protects Against Short Circuit Faults
- Seven Bit Adjustable Reference Voltage via I^2C Bus
- RoHS Compliant

Applications

- High Performance HDD
- LCD TV
- Notebook/Netbook
- Server and Workstations
- Video Cards
- PoE Powered Devices Smart Phone

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Analog Mixed Signal Group
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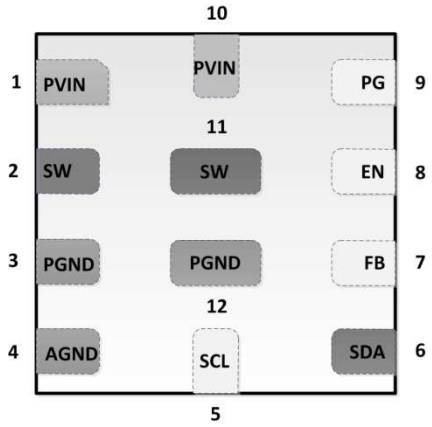
Pin Configuration and Pinout



LX7180A
Top View

80x1
YWWL

"x" is the 2LSB bits of the binary I^{2}C slave Address (see Part number below)
"1" is for the set output voltage (see Part number below)
YWWL = Year/Week/Lot Code
RoHS / Pb-free Matte Tin Pin Finish

Figure 2: Pinout

Ordering Information

Ambient Temperature	Type	Package	Slave Address	Set Output Voltage	Part Number	Packaging Type
0°C to 85°C	RoHS compliant, Pb-free	QFN 2x2mm 12L	0	0.9v	LX7180A-01CLQ	Bulk
			1		LX7180A-11CLQ	
			2		LX7180A-21CLQ	
			3		LX7180A-31CLQ	
					LX7180A-xyCLQ*	
			0	0.9v	LX7180A-01CLQ-TR	Tape and Reel
			1		LX7180A-11CLQ-TR	
			2		LX7180A-21CLQ-TR	
			3		LX7180A-31CLQ-TR	
					LX7180A-xyCLQ-TR*	

* Consult factory for other I^{2}C slave address and set output voltage options.
"x" is the 2 LSB bits of the binary I^{2}C slave address (0 to 3);
"y" is the set output voltage (0 is 0.6V, 1 is 0.9V, 2 is 0.95V, 3 is 0.97V)

Thermal Properties

Thermal Resistance(θ_{JA})	Typ	Units
QFN 2x2mm 12L	30	°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Pin Description

Pin Number	Pin Designator	Description
1, 10	PVIN	Supply Voltage. Bypass PVIN to ground plane as close as possible to the IC.
2, 11	SW	Switch Output. Drives the external L-C filter.
3, 12	PGND	Power Ground. Connect to ground plane.
4	AGND	Analog Ground. Connect to ground plane.
5	SCL	I^2C Serial Clock Digital Input.
6	SDA	I^2C Serial Data. Digital Input/Output.
7	FB	Feedback – Analog input, monitors the output voltage either directly or through a resistor divider.
8	EN	Enable – Digital input. Force high to enable the IC.
9	PG	Power Good – Open drain digital output. Pulls low to indicate a fault condition. Requires an external pull up resistor.

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

Parameter	Min	Max	Units
PVIN, EN, PG, SCL, SDA, SW to GND	-0.3	7	V
AGND to GND	-0.3	0.3	V
SW to GND (Shorter than 50ns)	-2	7	V
Junction Temperature Range	-10	150	°C
Storage Temperature Range	-65	150	°C
Peak Lead Soldering Temperature (40s, reflow)		260 (+0, -5)	°C

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Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Input Voltage	3.0	5.5	V
Output Voltage	0.6	5.5	V
Output Current (VIN = 3V to 5V)	0	4	A
Ambient Temperature	0	85	°C

Note: Corresponding Max Junction Temperature is 125°C

Block Diagram

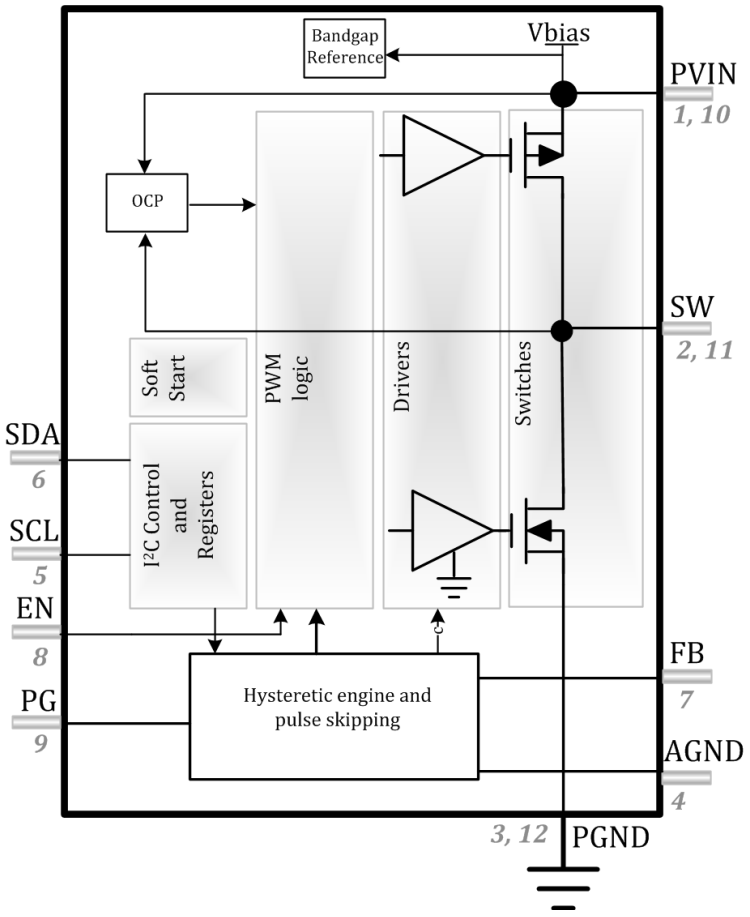

Figure 3: Block Diagram

Electrical Characteristics

Unless otherwise specified, the following specifications apply over the operating ambient temperature of 0°C ≤ T_A ≤ 85°C with the following test conditions: PVIN = 5V. Typical parameters refers to T_J = 25°C. VOUT is connected directly to FB for closed loop tests (default test condition). V_{REF} is set to 0.9V. VOUT is disconnected from FB for open loop tests. Default registers settings. I_{load} = 0. EN=high. GBD specifications are guaranteed by design and/or characterization and are not tested on a production basis. SCL and SDA set to PVIN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN						
I_{QPSM}	PSM Bias Current	Enable PSM. Force FB to 1V open loop.		350		µA
I_{SLEEP}	Input Current at Shutdown	EN = low		0.1	3	µA
$I_{In\_I^2C}$	I^2C Shutdown Sleep Current	Set VSEL(7)=low, EN=high.		20		µA
$UVLO_{RISING}$	Under Voltage Rising Threshold	PVIN rising			2.8	V
$UVLO_{HYST}$	UVLO Hysteresis	PVIN falling		0.2		V
OVP_R	Over Voltage Rising Threshold	PVIN rising. Will also trigger on DV/DT > 1V/µs		6.1		V
OVP_F	Over Voltage Falling Threshold	PVIN falling	5.5	5.85		V
VREF						
V_{REFMIN}	Minimum Reference Voltage	VSEL(6:0) = 00h.		0.6		V
$V_{REFMEAN}$	Mean Reference Voltage	VSEL(6:0) = 40h.		0.9		V
V_{REFMAX}	Maximum Reference Voltage	VSEL(6:0) = 7Fh.		1.195		V
T_{SS}	V_{REF} Slew Rate			5		mV/µs
T_{HICCUP}	Hiccup Time			1.2		ms

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
FB						
VFB_{SET}	V_{FB} Set Point Accuracy	Enable PWM. VSEL(6:0) = 40h	0.891	0.9	0.909	V
		Enable PWM. VSEL(6:0) = 00h	0.591	0.6	0.609	V
		Enable PWM. VSEL(6:0) = 7Fh	1.177	1.195	1.213	V
VFB_{PWM}	PWM FB Accuracy	Enable PWM. T_A = 25°C PVIN = 3V, I_{OUT} = 0A PVIN = 3V, I_{OUT} = 1A PVIN = 5.5V, I_{OUT} = 0A PVIN = 5.5V, I_{OUT} = 1A, Note 1	0.886	0.9	0.914	V
VFB_{PSM}	PSM FB Accuracy	Enable PSM. T_A = 25°C PVIN = 3V, I_{OUT} = 0A PVIN = 3V, I_{OUT} = 1A PVIN = 5.5V, I_{OUT} = 0A PVIN = 5.5V, I_{OUT} = 1A, Note 1	0.882	0.9	0.918	V
VFB_{LRPWM}	PWM Load Regulation	I_{LOAD} = 0A to 4A. Note 1		-0.17		%/A
	PWM Line Regulation	V_{OUT} = 0.9V. PVIN from 3V to 5.5V, Enable PWM, I_{LOAD} = 0.1A. Note 1		0.06		%/V
	PSM Line Regulation	V_{OUT} = 0.9V. PVIN from 3V to 5.5V, Enable PSM, I_{LOAD} = 0.1A. Note 1		0.07		%/V
FB_{IL}	FB Input Current				1	µA
FB_{UV}	FB Under Voltage Threshold	V_{OUT} below this threshold will initiate a hiccup sequence.		80		$\%V_{REF}$
R_{DISC}	Output Discharge Resistance	EN = low	80	314	500	Ω
SW						
R_{DSON_H}	High Side On Resistance			46		mΩ
R_{DSON_L}	Low Side On Resistance			21		mΩ
I_{RATED}	Rated Output Current	PVIN = 3V to 5V. Note 1	4			A

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CL}	Current Limit	Peak inductor current. PVIN = 3V to 5V. Note 1	5.7	7	8.6	A
T_{SH}	Thermal Shutdown Threshold	Note 1		150		°C
T_H	Thermal Shutdown Hysteresis	Note 1		20		°C
F_{SW}	PWM Switching Frequency	Vout ≥ 1.8V, T=25°C	1.55	1.65	1.75	MHz
EN, SDA (as input), SCL						
V_{IH}	Input High				1.1	V
V_{IL}	Input Low		0.4			V
I_{IN}	Input Current			0.01	1	µA
PG						
V_{PG90}	PGOOD VOUT Lower Threshold	V_{OUT} rising		90		% V_{REF}
V_{PG110}	PGOOD VOUT Upper Threshold	V_{OUT} falling		110		% V_{REF}
V_{PGHY}	Hysteresis			5		% V_{REF}
PG_{RDSON}	PGOOD Pull-down Resistance			13	50	Ω
PG_{ILEAK}	PGOOD Leakage Current	T_J = 25°C		0	1	µA
PG_{DELAY}	**PGOOD Delay**		25	45	65	mS

Note 1: These parameters are not tested, but guaranteed by design and characterization.

Typical Performance Curves (Efficiency)

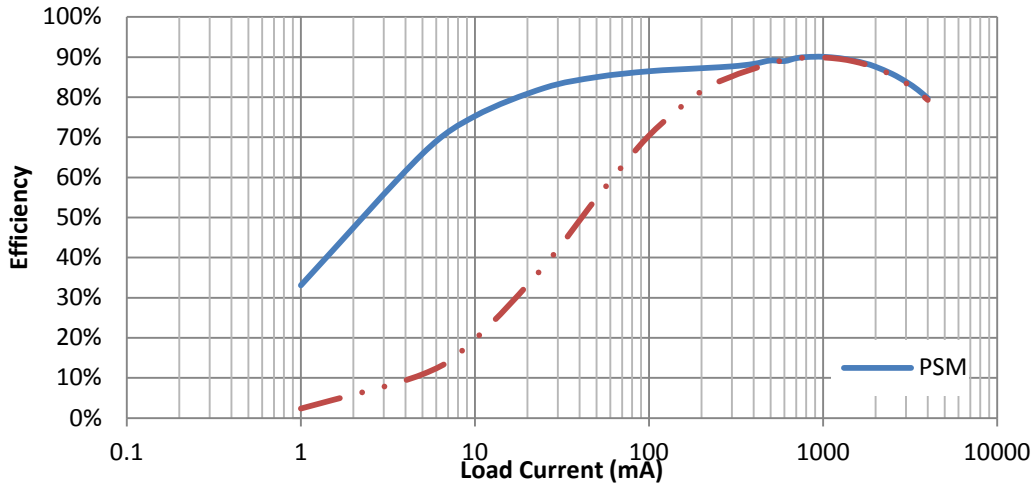


Figure 4: LX7180A PWM Efficiency with VIN = 5V, VOUT = 0.9V, L = 1.0µH, C_{OUT} = 66µF

Step Response (Load Current = 2A to 4A, L = 0.47µH, C_{OUT} = 22µF)

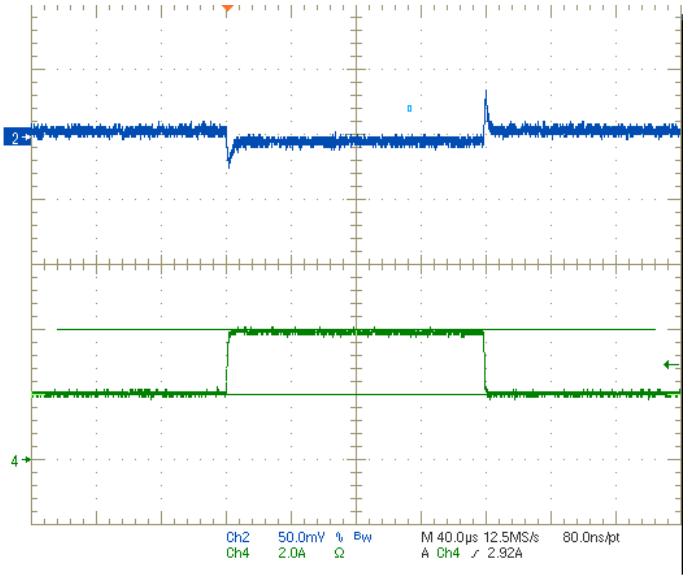


Figure 5. Step Response

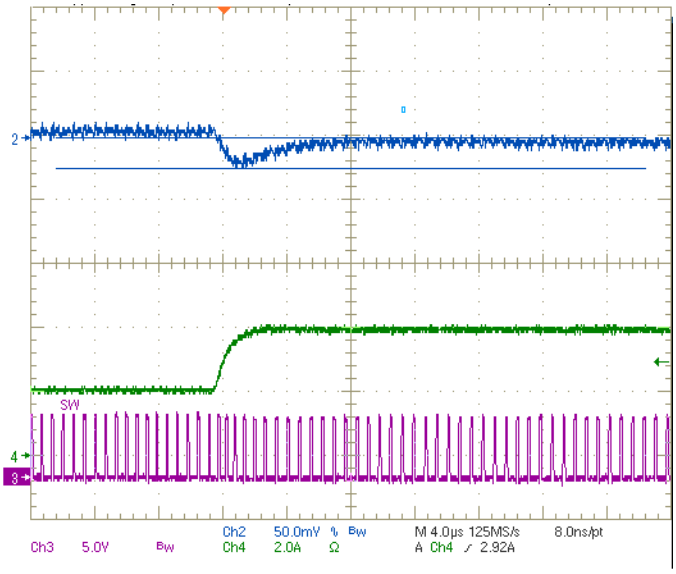


Figure 6. Step Response Rising Edge

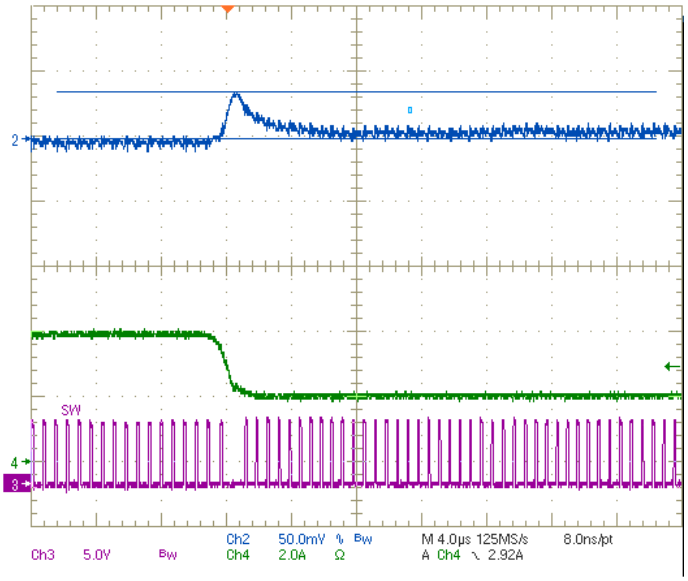


Figure 7. Step Response Falling Edge

I²C Timing Specifications

Symbol	Parameter	Conditions	C_b = 100 pF (max) (Note2)		C_b = 400 pF		Unit
			Min	Max	Min	Max	
f_{SCHL}	SCLH and SCL clock frequency		0	3.4	0	0.4	MHz
$t_{SU;STA}$	Set-up time for a repeated START condition		160	-	600	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition		160	-	600	-	ns
t_{LOW}	LOW period of the SCL clock		160	-	1300	-	ns
t_{HIGH}	HIGH period of the SCL clock		60	-	600	-	ns
$t_{SU;DAT}$	Data set-up time		10	-	100	-	ns
$t_{HD;DAT}$	Data hold time		47	70	0	-	ns
t_{rCL}	Rise time of SCLH signal		10	40	$20*0.1C_b$	300	ns
t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	$20*0.1C_b$	300	ns
t_{fCL}	Fall time of SCLH signal		10	40	$20*0.1C_b$	300	ns
t_{rDA}	Rise time of SDAH signal		10	80	$20*0.1C_b$	300	ns
t_{fDA}	Fall time of SDAH signal		10	80	$20*0.01C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		160	-	600	-	ns
t_{BUF}	Bus free time between a STOP and START condition		160	-	1300	-	ns
$t_{VD;DAT}$	Data valid time		-	160	-	900	ns
$t_{VD;ACK}$	Data valid acknowledge time		-	160	-	900	ns
C_b	Capacitive load for each bus line	SDAH and SCLH lines	-	100		400	pF
		SDAH + SDA line and SCLH + SCL line	-	400		400	pF

Note 1: All values referred to V_{IH}(min) and V_{IL}(max) levels of I/O stages table.
Note 2: Loads in excess of 100pf will restrict bus operation speed below 3.4MHz.

Operation Theory

Basic Operation

The LX7180A compares the FB voltage to an internal reference, V_{REF}. When FB is lower than V_{REF}, the upper switch turns on and the lower switch turns off. When FB is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp and a frequency control loop keep the switching frequency constant when in constant conduction mode (CCM) over a wide range of output capacitor values and parasitic components (i.e. ESR, ESL).

At light loads, if enabled, the converter automatically reduces the switching frequency to optimize efficiency.

An integrated I^2C bus interface, operating up to 3.4Mbps, allows the following user programmability to the converter:

1. On the fly programming of the reference voltage in 4.7mV increments.
2. Enable / Disable the regulator.
3. Enable power save mode (PSM) or limit operation to continuous conduction only (PWM).
4. Set the V_{REF} slew rate.
5. Enable/Disable VIN over voltage protection.
6. Force PGOOD to respond to both under and over voltages or just under voltage.

Setting the Output Voltage

The reference voltage can be programmed with the I^2C bus VSEL register value.

$$V_{REF} = 0.6V + V_{SEL} \cdot 0.0047V \quad (2)$$

Where VSEL is programmable from 0 to 127.

Startup

The LX7180A is enabled when EN is high and PVIN rises above the UVLO threshold. At start up, after all the internal bias voltages and currents stabilize, V_{REF} ramps up from 0V to the target voltage at the defined slew rate. While VREF ramps, PGOOD is held low. At the end of the ramp time, PGOOD is allowed to go high 45mS after FB has reached the PGOOD rising threshold. During the ramp time, the LX7180A always runs in PSM to allow discontinuous operation. This switchover is independent of the programmed MODE bit setting

Over Current Protection

The LX7180A protects against all types of short circuit conditions. Cycle by cycle over current protection turns off the upper switch when the current exceeds the ICL threshold. When this occurs, the upper switch is kept off for about 360nS before being allowed to turn on again. After startup, if FB drops below the FBUV threshold, a hiccup sequence will be initiated where both output switches are shut off for 1.2mS before initiating another soft start. This protects against a crowbar short circuit. FB under voltage detection is not active during startup.

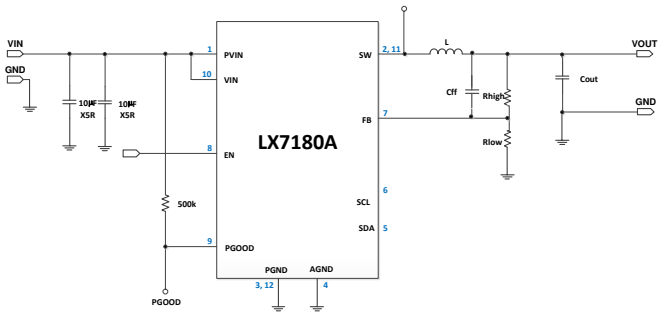
Recommended Output Filter Components

The following tables show the recommended feedback component values (R_{HIGH}, R_{LOW}, Cff) for different input/output voltages, power inductor (L), and output capacitance (C) values that result in optimum closed loop response of the regulator in each case. The estimated crossover frequency is also shown in the table in each case. If the L*C factor exceeds a certain number the regulator would run with low phase margin, or become unstable. The L and C range provided in the table provides 30°, or higher of phase margin. Therefore, it is not recommended to increase L*C factor beyond what is given in the table.

It is a good practice to determine L such that the peak-to-peak inductor ripple current in continuous conduction mode operation is roughly equal to 30% of converter's rated output current. In general, increasing the inductance slows down the closed loop response of the regulator. Hence, for applications that require fast line/load transient response, lower inductance values should be preferred over larger ones. Output capacitance can be determined based on desired output ripple voltage staying within the limits provided in the table depending on the inductance value.

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	Cff (pF)	F crossover (kHz)
5.0	0.9	2.2	2x22	0	∞	none	110
			1x22				180
		1.5	4x22				95
			3x22				110
			2x22				140
			1x22				240
		1.0	5x22				110
			4x22				120
			3x22				140
			2x22				190
			1x22				325
		0.47	5x22				170
			4x22				200
			3x22				240
			2x22				350
			1x22				650
		0.33	5x22				220
			4x22				260
			3x22				325
			2x22				475

Note: V_{REF} = 0.6V if FB network exists



Recommended Output Filter Components - Continued

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	Cff (pF)	F crossover (kHz)
3.0	0.9	2.2	1x22	0	∞	none	130
		1.5	2x22				110
			1x22				162
		1.0	3x22				110
			2x22				140
			1x22				220
		0.47	5x22				120
			4x22				140
			3x22				170
			2x22				220
			1x22				400
		0.33	5x22				150
			4x22				180
			3x22				220
			2x22				300
			1x22				550

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	Cff (pF)	F crossover (kHz)
5.0	1.8	2.2	5x22	240	120	20	49
			4x22				57
			2x22				70
			3x22			15	85
			1x22				150
		1.5	5x22			15	58
			4x22				68
			3x22				84
			2x22				120
			1x22				200
		1.0	5x22			15	77
			4x22				92
			3x22				120
			2x22			8	130
			1x22				260
		0.47	5x22			8	110
			4x22				130
			3x22				180
			2x22	120	60		190
			1x22				475
		0.33	5x22	240	120	8	150
			4x22				190
			3x22				260
			2x22	60	30		220
			1x22				500

Recommended Output Filter Components - Continued

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	Cff (pF)	F crossover (kHz)
3.0	1.8	2.2	5x22	240	120	20	36
			4x22				42
			3x22				50
			2x22			15	60
			1x22				100
		1.5	5x22			15	42
			4x22				49
			3x22				60
			2x22				79
			1x22				140
		1.0	5x22			15	55
			4x22				64
			3x22				79
			2x22			8	87
			1x22				150
		0.47	5x22			8	76
			4x22				89
			3x22				110
			2x22				160
			1x22				350
		0.33	5x22			8	97
			4x22				120
			3x22				150
			2x22				240
			1x22				525

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	Cff (pF)	F crossover (kHz)
5.0	3.3	2.2	5x22	540	120	30	58
			4x22				67
			2x22				81
			3x22				110
			1x22				170
		1.5	5x22				75
			4x22				87
			3x22				100
			2x22				140
			1x22				240
		1.0	5x22			43	100
			4x22				120
			3x22				140
			2x22				190
			1x22				325
		0.47	5x22			43	170
			4x22				200
			3x22				240
			2x22				350
			1x22	225	50	8	450
		0.33	5x22	540	120	30	220
			4x22				260
			3x22				325
			2x22				475
			1x22	135	30	8	525

Operation Theory (Continued)

Positive Voltage Transitions

After the initial start up sequence, the output voltage can be programmed to a new value by programming the VSEL register bits and then asserting the GO bit. V_{REF} will transition to the new value at the programmed slew rate. During the transition time the PGOK bit will be low and will go high when the transition completes.

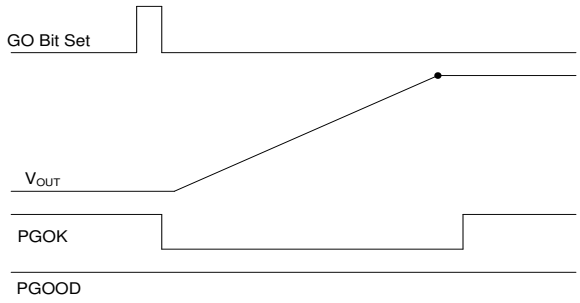


Figure 8: Positive Voltage Transition

Negative Voltage Transitions

A negative voltage transition occurs when a lower output voltage is programmed into the Vsel register, and initiated by asserting the GO bit. During the transition, when in PFM mode of operation, the upper PGOOD threshold is disabled if set.

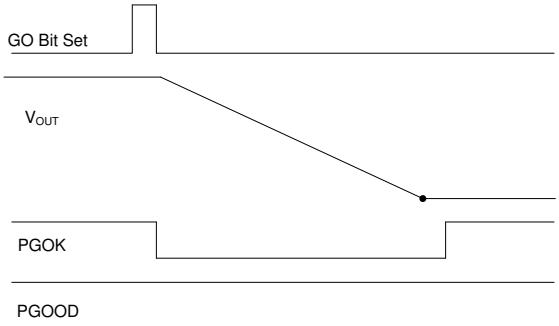


Figure 9: Negative Voltage Transition

If the FB voltage does not drop within 10% of the programmed voltage within 30mS, then PGOOD will go low. During a transition when in PWM only mode of operation, the PGOOD thresholds will not be disabled but will trigger if the output falls outside the 10% tolerance window around the ramped programmed voltage.

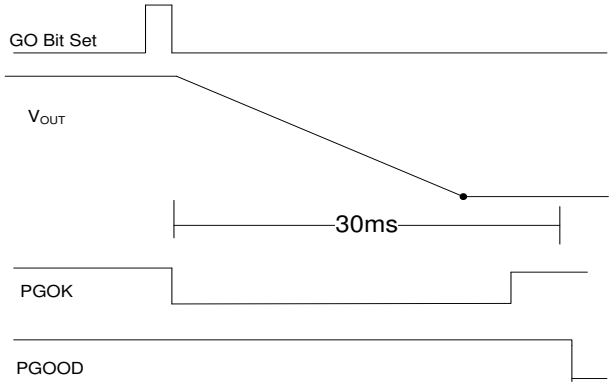


Figure 10: Negative Voltage Transition PGOOD Fail

Enabling Regulator from I^2C Bus

In addition to the EN pin, the regulator can be enabled and disabled via the I^2C bus by programming the control register. During disable, the regulator and most of the support circuitry is turned off. However, the I^2C bus circuitry is still active and may be programmed.

I²C Interface

I²C Port Functional Description

- Simple two wire, bidirectional, serial communication port.
- Multiple devices on same bus speeds from 400kbps (FS-Mode) to 3.4Mbps (HS-Mode).
- SOC Master controls bus.
- Devices listen for the unique address that precedes data.

General I²C Port Description

The LX7180A includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage when they are not being controlled by a device on the bus. The serial port is an I²C slave that is clocked by the incoming SCL clock. The I²C port will support both the Fast mode (400kHz max) and typically the High speed mode(3.4MHz max). The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

Register Map

There are five 8-bit user-accessible registers. See the register map table below.

Slave Address

In the table below, the A1 and A0 are the binary value of the address given in the ordering information shown on page 2.

7	6	5	4	3	2	1	0
1	1	0	1	0	A1	A0	R/W

Table 1: I²C Slave Address

START and STOP Commands

When the bus is idle, both SCL and SDA must be high except in the power up case where they may be held high or low during the system power up sequence.

The STX SOC (bus master) signals START and STOP bits signify the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The STX SOC acts as the I²C master and always generates the START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transfer, STX SOC master can generate repeated START conditions. The START and the repeated START conditions are functionally equivalent.

I²C Interface (Continued)

Data Transfers

Data is transferred in 8 bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the master. The acknowledge occurs when the transmitter master releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver slave during the 9th clock pulse to signify acknowledgment. A receiver slave which has been addressed must generate an acknowledgement ("ACK") after each byte has been received.

After the START condition, the STX SOC (I^2C) master sends a chip address. The standard I^2C address is seven bits long. Making the eighth bit a data direction bit (R/W). For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a receiver slave doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP command to abort the transfer. If a slave receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP command. The data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid STOP command has been performed.

I²C Electrical Characteristics

The minimum HIGH and LOW periods of the SCL clock specified the I^2C Timing Specification table determine the maximum bit transfer rates of, 400 kbit/s for Fast-mode devices, and 3.4 Mbits/s for HS-mode Plus. Devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the I^2C clock synchronization procedure, which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Figure 14 and Figure 15 show all timing parameters for the HS & FS-mode timing. The 'normal' START condition S does not exist in HS-mode. Timing parameters for Address bits, R/W bit, Acknowledge bit and DATA bits are all the same. Only the rising edge of the first SCL clock signal after an acknowledge bit has a larger value because the external Rp has to pull-up SCL without the help of the internal current-source.

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I²C Interface (Continued)

The HS & FS-mode timing parameters for the bus lines are specified in the I²C Timing Specification Table. The minimum HIGH and LOW periods and the maximum rise and fall times of the SCL clock signal determine the highest bit rate.

With an internally generated SCL signal with LOW and HIGH level periods of 200ns and 100ns respectively, an HS-mode master fulfills the timing requirements for the external SCL clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4 Mbit/s. So a basic frequency of 10 MHz, or a multiple of 10 MHz, can be used by an HS-mode master to generate the SCL signal. There are no limits for maximum HIGH and LOW periods of the SCL clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load up to 100 pF for each bus line allowing the maximum possible bit rate of 3.4 Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400 pF are specified in I²C Timing Specification Table, allowing a maximum bit rate of 1.7 Mbit/s. For capacitive bus loads between 100 pF and 400 pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDA and SCL to prevent reflections of the open ends.

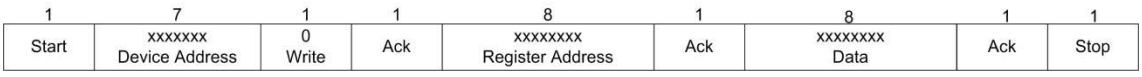


Figure 12: Write Protocol

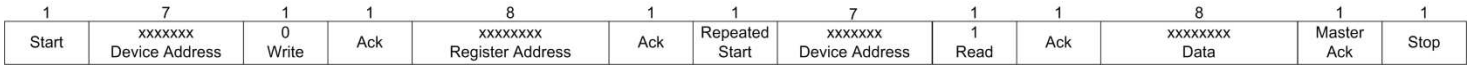


Figure 13: Read Protocol

I²C Interface (Continued)

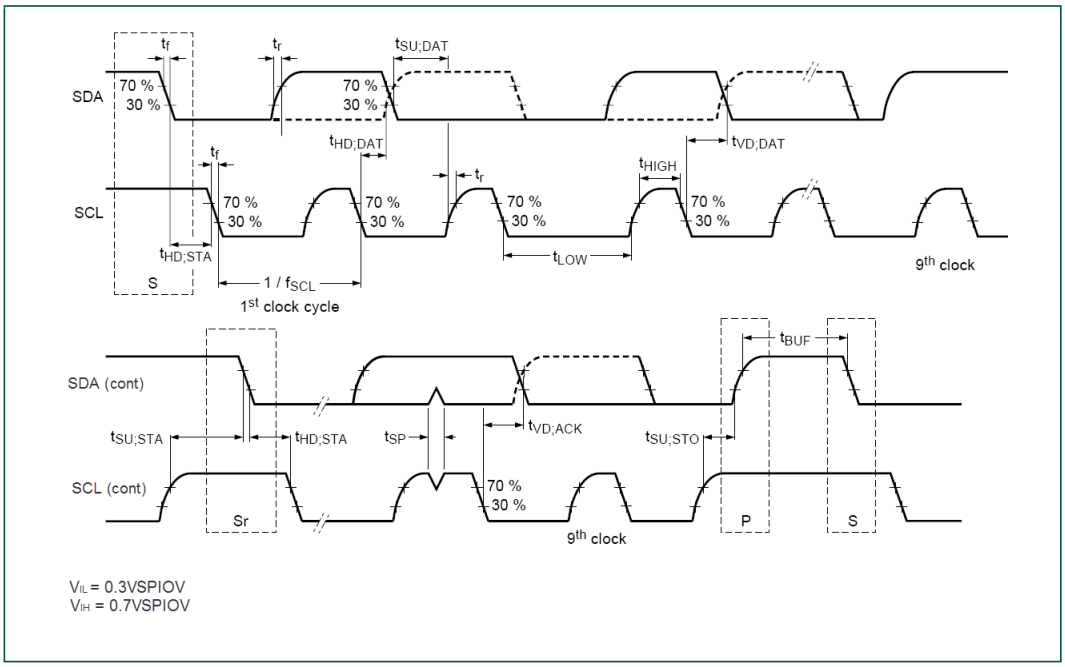


Figure 14: Definition for FS-Mode devices on the I²C Port

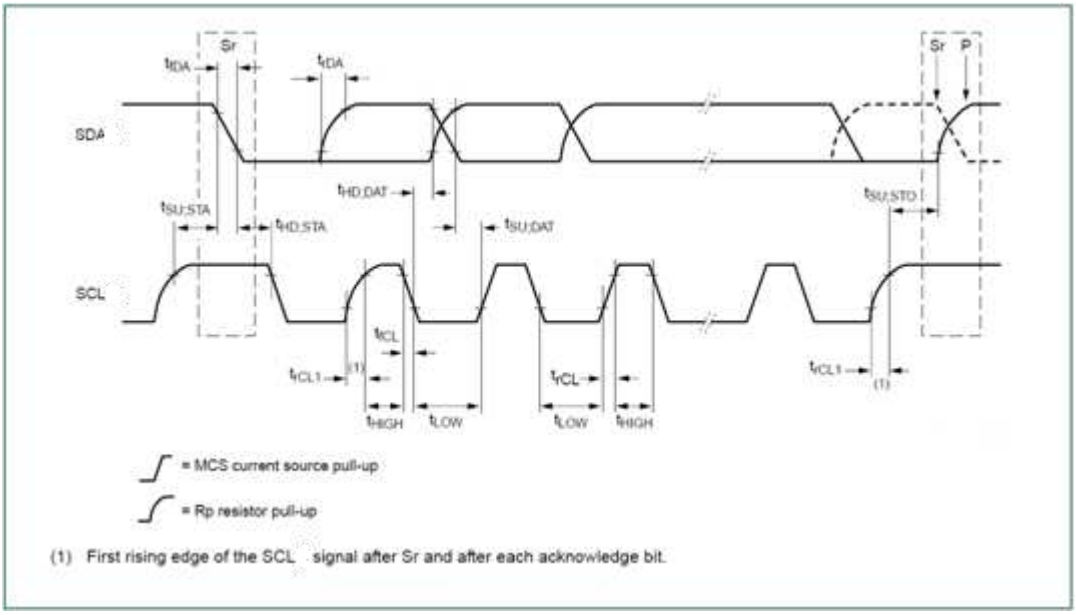


Figure 15: Timing definition for HS-mode devices on the I²C Port

I²C Interface (Continued)

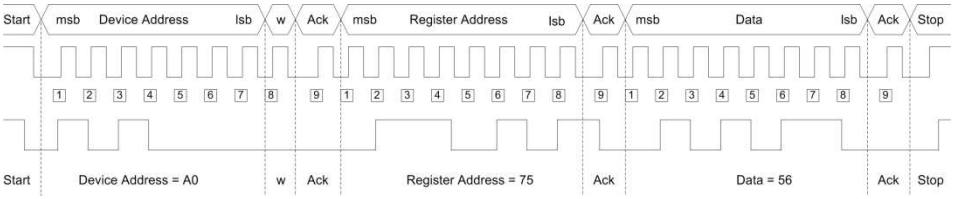


Figure 16: Write Cycle Diagram

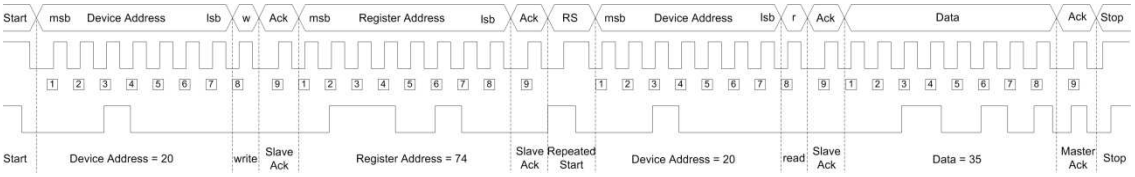


Figure 17: Read Cycle Diagram

Control Register Bit Definition

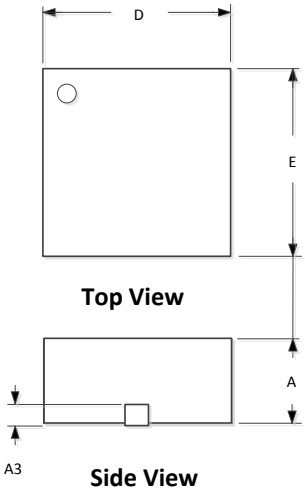
Bit	Name	Value	Description
Status, Address 00h			
7:3	Reserved		
2	OCP	0-d	Latched to 1 if the over current limit is reached. Write a "1" to reset the status flag.
1	OTP	0-d	Latched to 1 if an over temperature event occurs. Write a "1" to reset the status flag.
0	FB_UVLO	0-d	Latched to 1 if a FB_UVLO event occurs. Write a "1" to reset the status flag.
VSEL, Address 01h, (aka dac)			
7	EN	1-d	Device enabled.
		0	Device disabled.
6:0	VSEL[6:0]		7-bit DAC value to set V_{REF}. The default value is 0.9V.

Bit	Name	Value	Description
Ctrl1, Address 02h, (aka reg2)			
7:6	Reserved	00-d	
5	DLY_DIS	1-d	45ms delay on PGOOD is disabled when this bit is high.
4	ctrl1	0-d	Not used
3	SW_RATE	1-d	Normal high efficiency rise rate.
		0	Reduced switch node rise rate.
2	PG_LOHI	1-d	PGOOD will detect both a positive and negative excursion of VOUT from the reference.
		0	PGOOD senses only a negative voltage excursion of VOUT from the reference.
1	VIN_OVP	1-d	When VIN reaches VIN Max, the converter turns off.
		0	VIN OVP disabled. Converter will continue to operate
0	MODE	1-d	PWM – Always run in continuous conduction
		0	PSM – Power Save Mode allows the converter to run in discontinuous conduction
Vendor ID, Address 03h (Read Only)			
7:4	VID[3:0]	0010	Microsemi Vendor ID .
3:2	A1A0	00	Designates the slave address version. These bits will correspond to the two LSB bits.
1:0	VREF	01	Designates the default output voltage version, 00 = 0.6V, 01 = 0.9V, 10 = 1.0V, 11 = 1.1V.
Ctrl2, Address 04h, (aka reg4)			
7:6	Reserved		
5	GO	1	Write “1” to this bit to start a Vref transition
		0-d	The VOUT is ramped to the default VSEL Value.
4	Discharge	1	When the regulator is disabled, the output voltage is discharged through the SW pin.
		0-d	When the regulator is disabled, the output voltage is not discharged.
3	PGOK	1	Is high when output is in regulation, read only dynamic signal
		0	Is low during a output voltage transition, read only dynamic signal
2:0	SLEW	000	Reserved.
		001	Reserved.
		010	V_{REF} slews at 2.5mV/µs.
		011-d	V_{REF} slews at 5mV/µs; this is the default setting.
		100	V_{REF} slews at 10mV/µs.
		101	V_{REF} slews at 20mV/µs.
		110	V_{REF} slews at 40mV/µs.
		111	Single Step Mode: No slew rate limiting.

Note: -d is the default value at startup.

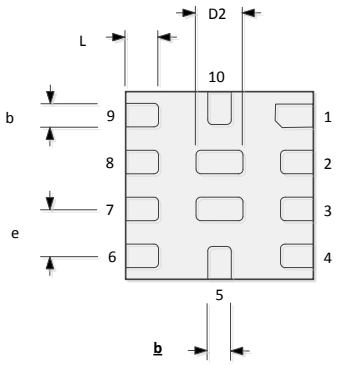
Package Dimensions

QFN 2x2mm 12L Package



Top View

Side View



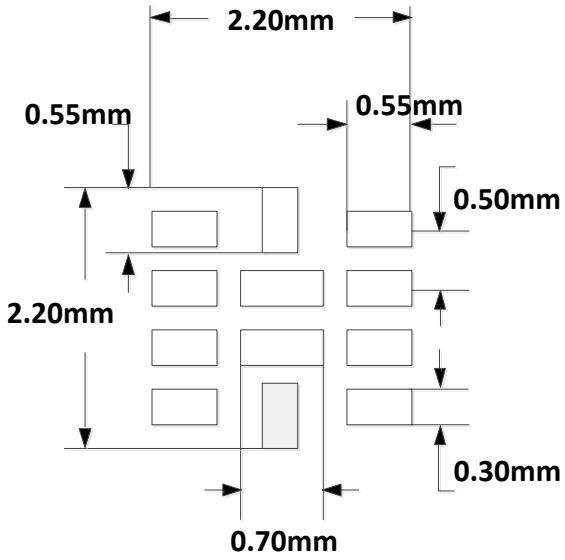
Bottom View

Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	.039
A3	0.20 REF		0.008 REF	
B	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
D2	0.50BSC		0.02BSC	
E	1.90	2.10	0.075	0.083
e	0.50 BSC		0.020 REF	
L	0.30	0.45	0.012	0.018

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

Recommended Footprint



Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

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