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User Guide
LX7730 Daughter Board

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in July 2017. It was the first publication of this document.

2 Overview

The LX7730 is a spacecraft telemetry manager IC that contains a 64 universal input multiplexer that can be configured as a mix of differential- or single-ended sensor inputs. There is also a programmable current source that can be directed to any of the 64 universal inputs. The universal inputs can be sampled with a 12-bit analog-to-digital converter at a sample rate up to 13 kSPS. The universal inputs can also function as variable bi-level inputs with the threshold set by an internal 8-bit digital-to-analog converter. There is an additional 10-bit digital-to-analog current DAC with complementary outputs. Finally, there are 8 fixed threshold bi-level inputs.

The LX7730 is register programmable with 17 addressable 8-bit registers. Two options are available for communication with the host FPGA. First, there is an 8-bit parallel bus with 5 address bits and a read /write bit that can communicate at a speed of up to 25 MHz. The second option is a pair of 12.5 Mbps SPI interfaces that can support redundant (alternating not simultaneous) communication to two different hosts.

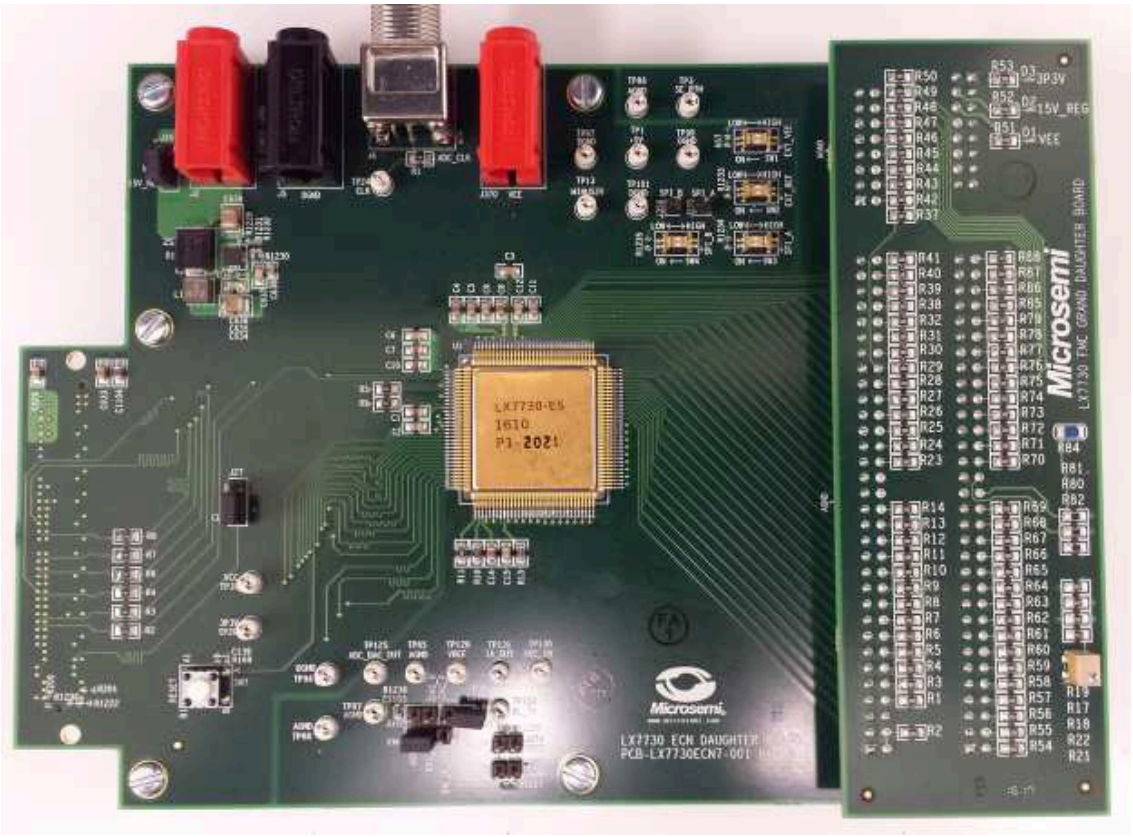
The LX7730 daughter board is designed to allow the user to exercise the controller's feature through RTG4 evaluation board and the provided application interface. The included granddaughter board is used to provide LX7730 input sensor data.

3 Kit Contents—LX7730 Daughter Board

The following list shows what is included with the LX7730 daughter board.

- LX7730 Daughter Board
- LX7730 Granddaughter Board
- LX7730 Daughter Board User Guide
- LX7730-RTG4 Interface Reference Design Application Note (downloadable from https://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4#documents)

Figure 1 • LX7730 Daughter and Granddaughter Board



4 Setup Procedure

The following sections describe the setup procedure for the LX7730 daughter board.

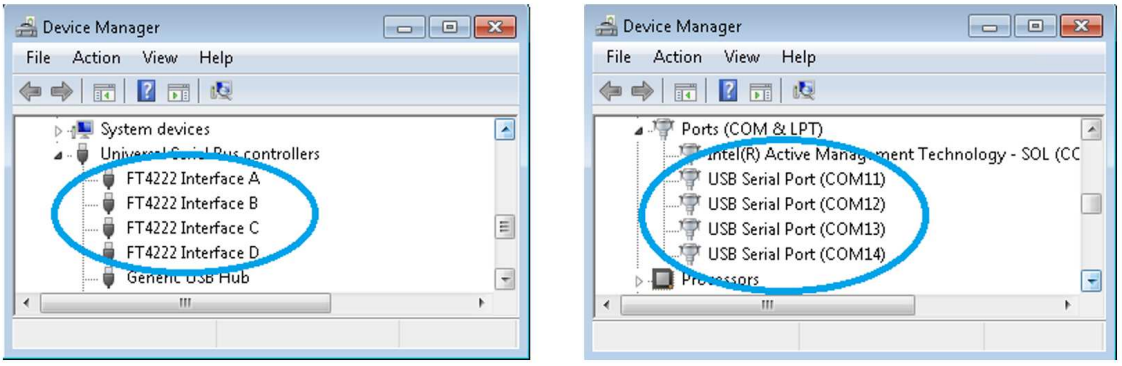
4.1 Hardware Connections

Connect the RTG4 development kit to a host PC through a USB-mini cable. Then, connect the LX7730 daughter card to the RTG4 board through the HPC1 (FMC) connector—on the shorter edge of the board. The LX7730 granddaughter board is connected to the daughter board through heads (J353, J354, J359, and J376) by default. Connect the wall power adapter in RTG4 kit to the RTG4 evaluation board. Then, turn on the power switch on the RTG4 board. Check the LED light indicators (3P3V,15V_REG, VEE). They should be on, otherwise check the jumpers on the board to make sure they are in correct positions.

4.2 Software

Install the FTDI FT4232 drivers (CDM v2.12.16 WHQL Certified.zip) on your local PC, once installed plug in the USB-mini cable. The device manager should indicate 4 active USB Serial Port devices, as shown in the following illustration.

Figure 2 • Device Manager

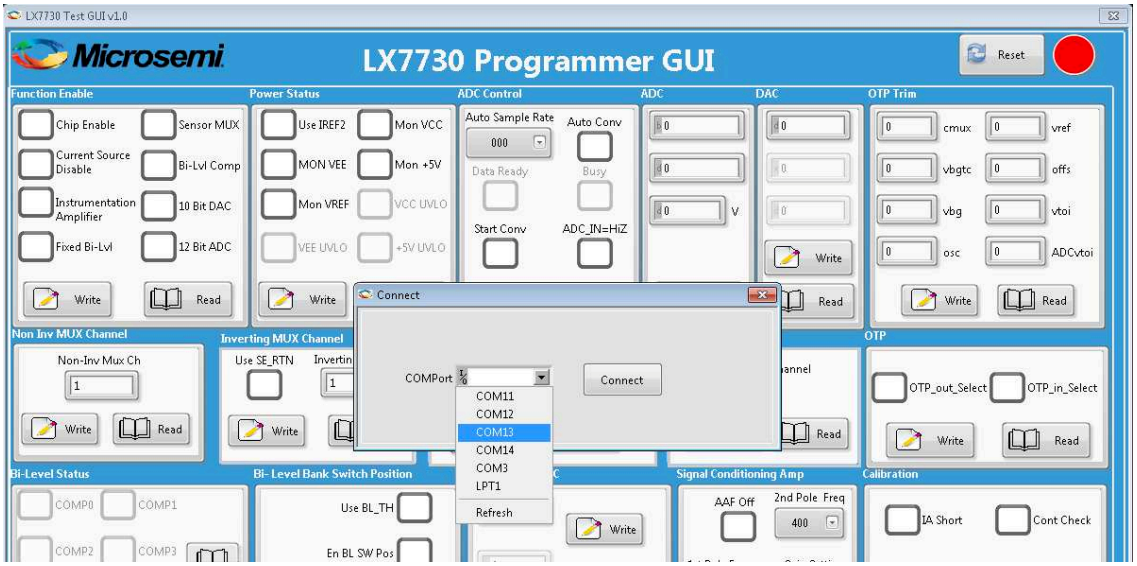


Run Flashpro to program RTG4 using file RT_LX7730_interface.stp. Run LX7730_GUI_Installer and run setup.exe to install GUI on your local PC. RTG4 programming file and GUI download links can be found in LX7730-RTG4 Interface Reference Design Application Note.

5 Powering on the Device

Execute the GUI software (LX7730.exe), select the third COM port corresponding to the RTG4 device from the drop-down menu, and click **Connect**. For example, If COM11, COM12, COM13, and COM14 are detected, select **COM13**. The GUI will close if the device is not powered on or if a wrong port is selected.

Figure 3 • Powering On the Device



SPIA is the default communication between LX7730 and RTG4 when GUI is started. Make sure switch SW3 on the LX7730 board is set low when the GUI is started. To switch between SPIA, SPIB, and parallel communication, click **SPI Selection** and choose the communication port. Set the switches SW3, SW4 on LX7730. The following table lists the combination of switches.

Table 1 • Combination of Switches

SW3	SW4	Communication Port
Low	High	SPIA
High	Low	SPIB
High	High	Parallel

Push the reset button SW7 on the LX7730 daughter board to start the new communication port.

To execute a command in the GUI, enter the information for the section and then click **Write** for the section. Then click **Read** for the section to verify the command was received. Entering information without a write will do nothing.

6 Using the Software GUI

The following sections describe how to use the software GUI for the LX7730 daughter board.

6.1 Master Reset

The master reset button is used to write register 0 and perform a master reset, which returns all internal registers to the power-on (default) state. The register's value shown in GUI will be refreshed after reset.

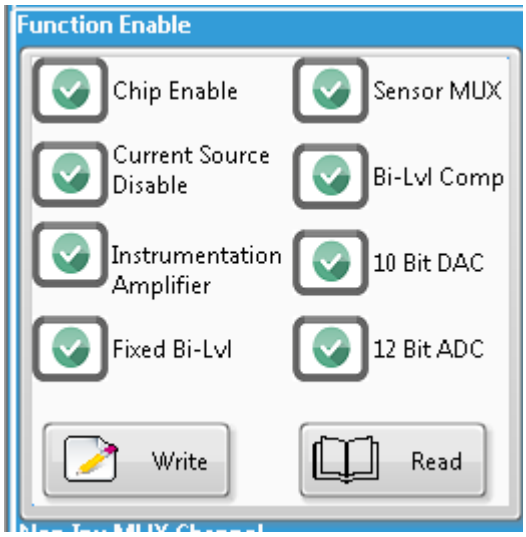
Figure 4 • Master Reset

6.2 Function Enable

The Function Enable screen provides the option to power down selected functions that are not needed—the default state is everything enabled as indicated. This feature allows the user flexibility to conserve power while keeping needed functions alive.

It is recommended to read back and verify the actual state of the LX7730's registers, and if necessary write again. The following illustration shows the function enable GUI.

Figure 5 • Function Enable



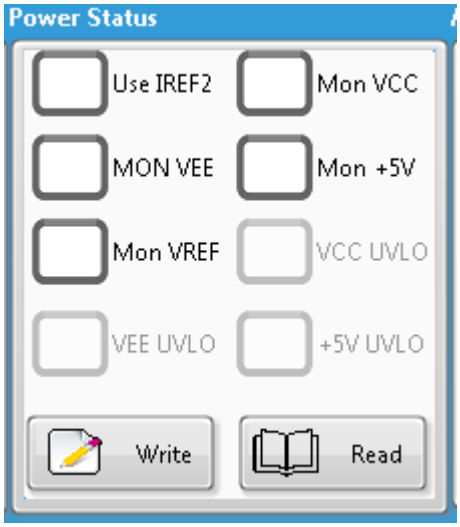
6.3 Power Status

The power supply pins for the LX7730 can be monitored by selecting special calibration registers: MON VCC, MON VEE, MON +5 V, MON VREF. The voltages are divided down by a factor of six for the VCC and VEE rails and a factor of two for the 5 V and VREF. Selecting one of these power monitoring registers overrides the register settings of the Analog MUX Inverting and non-inverting MUX Channel. The selected pin voltage is routed to the non-inverting terminal of the instrumentation amplifier (IA) for positive voltage and VEE is routed to the inverting terminal of the IA. GND is routed to the inverting terminal of the IA for the positive voltages and routed to the non-inverting input of the IA for Mon VEE.

For example, if Mon VCC is selected and the Signal Conditioning Amp Gain Setting is set to a gain of 0.4 and the ADC Controls Auto Conv box is checked then when reading the analog-to-digital converter (ADC), a measurement of about
1 V, should be indicated. (15 V divided by a gain of six (internal divider), times 0.4 (gain setting.)

The following illustration shows the power status GUI.

Figure 6 • Power Status



The LX7730 provides a redundant precision reference current IREF2 that can be selected should IREF 1 fail. The GUI allows selection of IREF2 internal IC resistor by checking the box in the Power Status window.

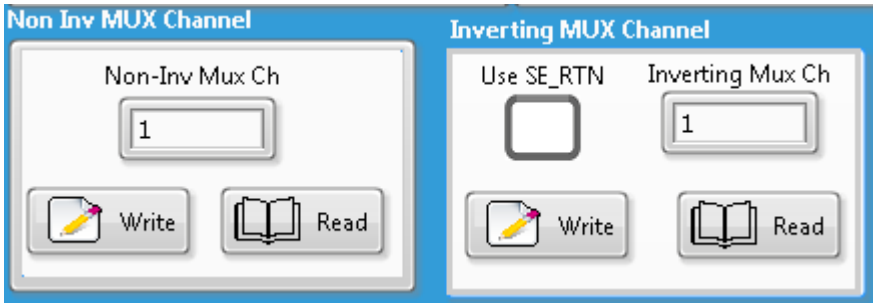
The VCC UVLO, VEE UVLO, and +5 V UVLO flags will be asserted when VCC, VEE, or +5 V respectively are below their corresponding UVLO thresholds. To find the UVLO status for any of these supplies select the Read button, and look for the corresponding status box check mark. They are greyed-out because they are output only and cannot be selected.

6.4 Analog MUX

The analog multiplexer (AMUX) consists of 64 inputs. The Bi-level MUX and the AMUX are not independent; the En BL Sw Pos must be de-selected in order to use the AMUX. For a single-ended input measurement the common SE_RTN reference pin can be selected by checking the box Use SE_RTN. When selecting SE_RTN, the SE_RTN pin is used as a common return for single-ended sensor inputs. When using differential sensor inputs the AMUX is physically divided into eight banks of eight inputs. Only one CH#, from one input bank can be selected at a time which means that differential measurements must consist of two CH#s from two different input banks.

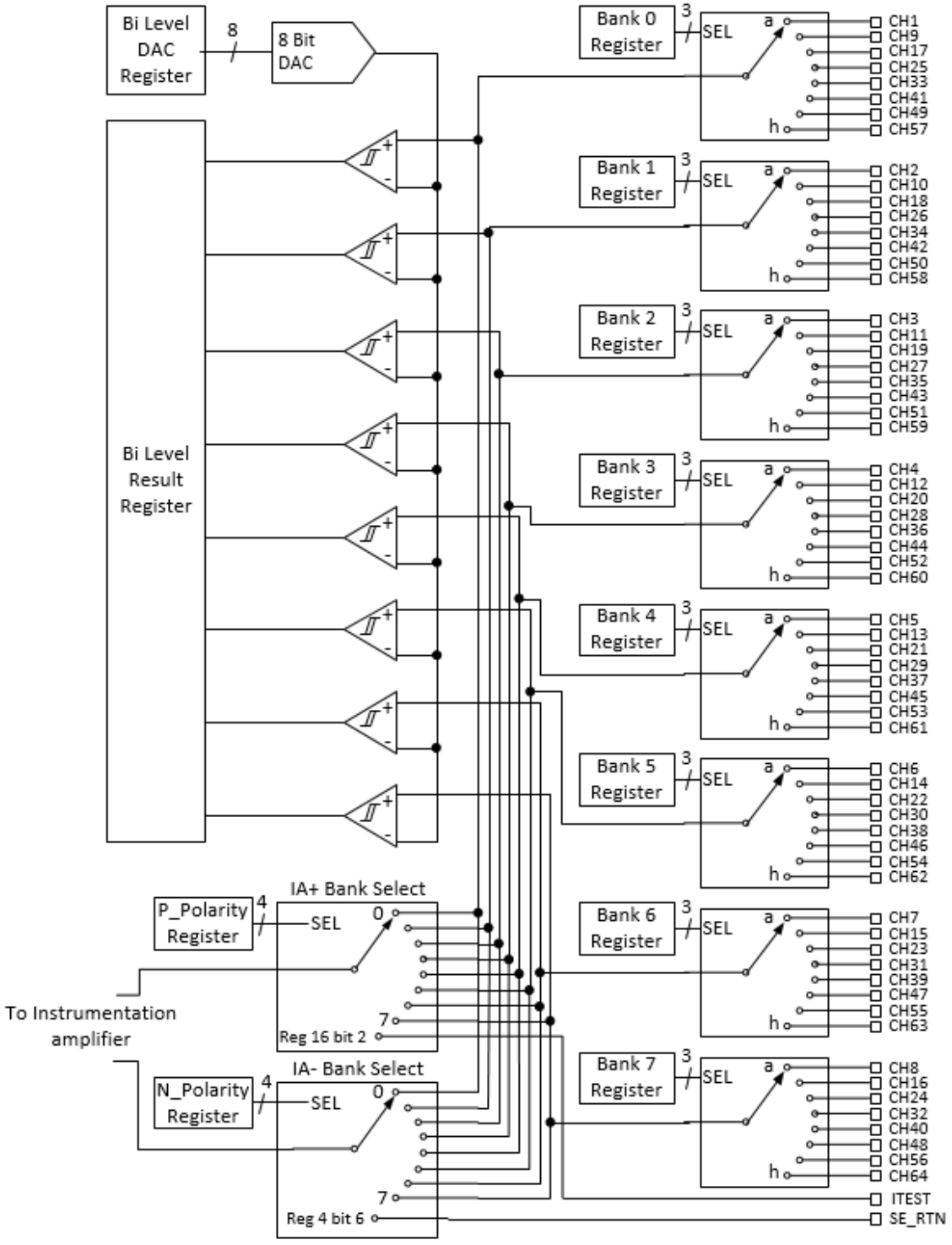
The following illustration shows the Non Inv MUX Channel and Inverting MUX Channel GUI.

Figure 7 • Analog MUX



The following illustration shows the sensor multiplexer block diagram.

Figure 8 • Sensor Multiplexer Block Diagram

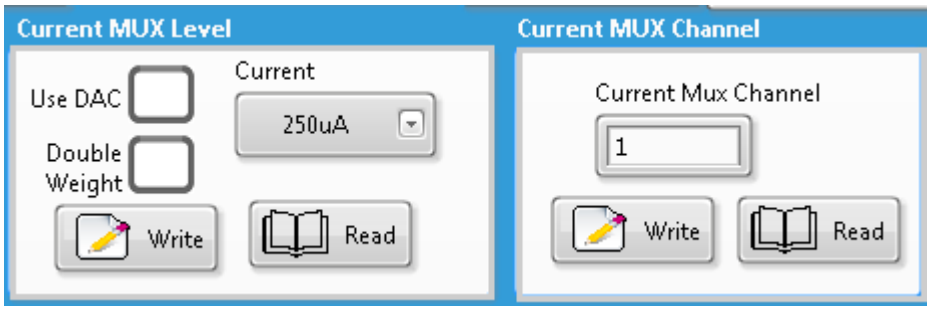


6.5 Current De-Mux

The current de-mux routes a programmable current to whichever of the 64 channel inputs is selected. The default channel in CH1, the default current is 250 µA. There are several modes of operation depending on the current amplitude required.

The following illustration shows the current MUX level and channel GUI.

Figure 9 • Current De-Mux



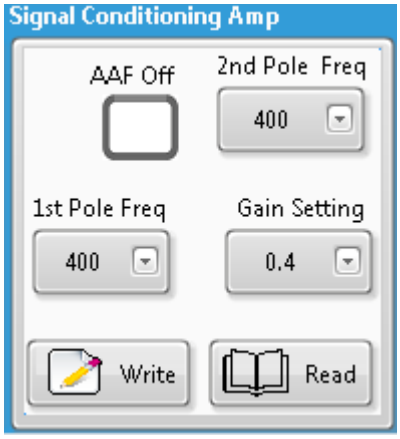
There are eight selectable levels range from 250 µA to 2 mA using the drop down box. When the Double Weight box is checked, the selected value is doubled for a range from 500 µA to 4 mA. If the Use DAC box is selected, the 10-bit DAC is used to set the de-mux current instead of the programmable current source—each LSB has a weight of 10 µA. A maximum of 300 µA is suggested (code 31) when operating in this mode. The current de-mux can be shut off selecting the Current Source Disable box in Function Enable; the current De-Mux defaults to the off state at power up and must be selected to activate.

6.6 Signal Conditioning Amp

The instrumentation amplifier, anti-aliasing filter, and ADC range scaling reside between the output of the analog multiplexer and the input to the ADC. The output of the entire gain and filter stage is accessible at the pin ADC_IN. If the AAF off box is selected the AAF filter is off and the ADC can be driven from ADC_IN.

The following illustration shows the signal conditioning amp GUI.

Figure 10 • Signal Conditioning Amp



The AAF poles are set to nominally 00, 01, and 10 for 400, 2k, or 10k in Hertz, respectively. Either one or both poles can be selected. The ADC sensitivity is set by adjusting the amplifier gain. The gain can be set to 10, 2, or 0.4.

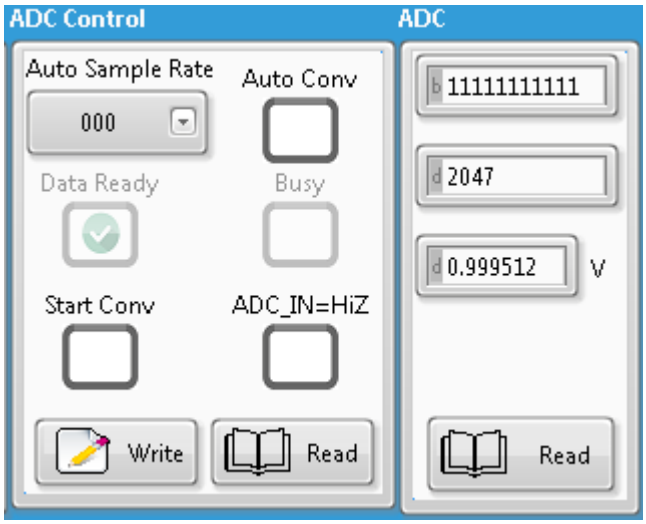
To allow operating room for the ADC (which operates from a 5 V rail), the ADC_IN range is 0 V to 2 V. If an external input is to be sampled by the ADC, the internal circuitry driving the ADC_IN pin can be made high impedance by setting the Hi-Z bit in the ADC programming register.

6.7 Analog to Digital Converter

The ADC uses a successive approximation register (SAR) design. The CLK input sequences the ADC logic. The Auto Sample Rate is set to multiples of the Sample Period (t_{SAMP}). This 3-bit N binary value sets the ADC auto sample rate = $t_{SAMP} \times 2^N$. The ADC can be set to convert continuously (Auto Conv) or to convert on request using (Start Conv). Whenever a conversion is in process, the Busy status bit is asserted. When the conversion is complete, the Data Ready bit is set. The ADC value registers are updated when the Data Ready bit is asserted, but will not change during the process of a data read which starts by reading the upper byte and ends by reading the lower byte. Click **Read** and Data Ready or Busy will display.

The following illustration shows the ADC and ADC control GUI.

Figure 11 • ADC Control



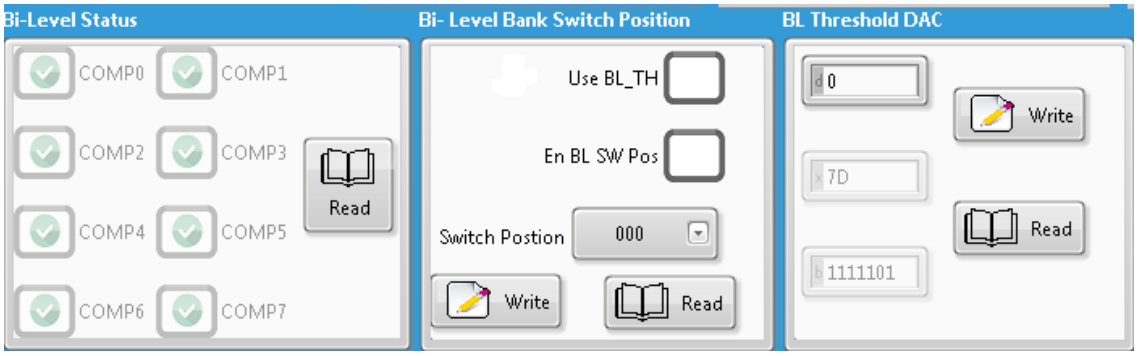
The ADC window will display the result of the latest conversion when the Read button is selected.

6.8 Bi-Level Inputs

There are two sets of 8 bi-level inputs on the LX7730. First the 64 sensor inputs can be used as bi-level detection inputs. The bi-level mux and the AMUX are not independent; the En BL Sw Pos must be selected to use the bi-Level mux. The bi-level detection comparators monitor one position simultaneously from each of the input banks; the position is register selectable (bank 0 to 7,000 to 111). For more information, see Sensor Multiplexer Block Diagram (see page 9). For example, code 000 will connect CH1 to CH8 to the 8 bi-level comparators, and code 001 to CH9 to CH16 respectively. The comparators are sampled during the clock cycle where the Bi-Level Status is read, and the result is placed in the Bi-Level Result Register shown in the GUI as Bi-Level Status.

The following illustration shows the bi-level inputs.

Figure 12 • Bi-Level Inputs



The outputs of the group of 8 comparators available in this register are continuously updated and can be polled to monitor the status. The GUI allows you to see the status of the Bi-Level Result Register in the Bi-Level Status window using the Read button. These functions are greyed-out because they cannot be selected and show a change by the check mark appearing or disappearing.

The selected eight bi-level inputs are compared to a common adjustable threshold that is developed using an 8-bit binary DAC.

In addition to these register based bi-level comparators utilizing the sensor inputs, the IC and the evaluation board include 8 external bi-level input pins (BLI1 to BLI8) that can be compared to either an internal 2.5 V reference level or an external threshold voltage (BL_TH) selected by checking **Use BL_TH** in the GUI. BLO1 to BLO8 are the comparator outputs of these 8 inputs and are referenced to VDD logic levels.

The following illustration shows the BLO1 to BLO8 logic results at the bottom of the GUI window.

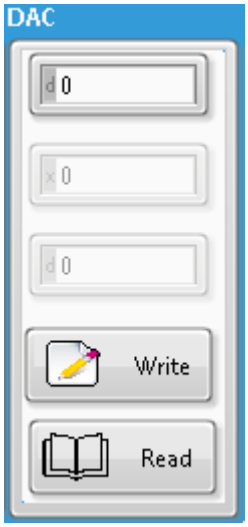
Figure 13 • BLO1 to BLO8 Logic Results

6.9 Current DAC

The output of the DAC should be terminated in a resistor that is less than 1.5 kΩ to insure the DAC stays within its compliance range. A parallel 1 nF or greater capacitor can also be used to help reduce bit change glitches. The DAC has complementary outputs that are accomplished by steering the current between the two outputs based on the DAC setting. At zero LSBs, the DAC_N is full scale and DAC_P is off.

The following illustration shows the DAC GUI.

Figure 14 • DAC

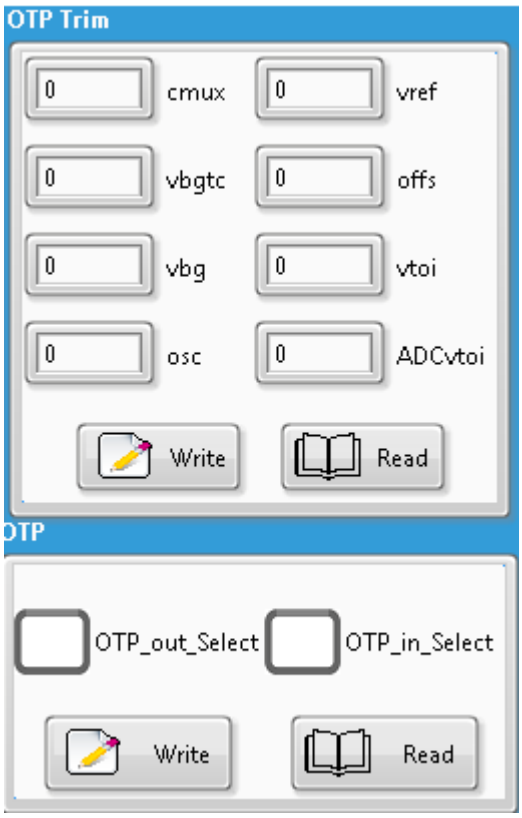


6.10 Power and Reference Adjust (OTP)

When Otp_out _select is checked and written to LX7730, the setting in the OTP trim boxes will override the default settings in the trimming register. These settings are temporary and must be re-written with a power cycle. If **Otp_out_select** is unchecked and **Write** is clicked, the contents of the trim registers will revert back to the default values. If **Otp_in_select** is checked and written, the default OTP bits are read into the display upon Read.

The following illustration shows the OTP and OTP Trim GUI.

Figure 15 • OTP Trim



6.11 Calibration

The calibration buttons write to register 16 and are used to perform calibration of the amplifier offset and testing of the multiplexer switches and programmable current source multiplexer. For more information, see the LX7730 datasheet that includes diagrams depicting the following modes.

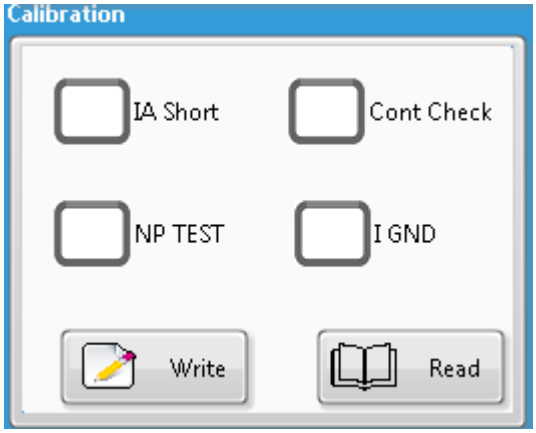
Table 2 • Calibration Modes

Name	Default	Description
IA Short	0	If selected, this action overrides the setting of the sensor mux and causes a switch closure that shorts the inverting terminal of the instrumentation amplifier to the non-inverting terminal.
Cont Check	0	If selected, a current source is applied to the non-inverting input of the instrumentation amplifier. Current flows out of the AMUX to the selected CH# input pin. If the current encounters an open circuit in the AMUX or at the CH# pin, the voltage at the IA non-inverting pin will clamp. If the external sensor is properly attached, the voltage read by the ADC will include the impedance of the sensor plus the impedance of the two AMUX switches encountered in the current path.
NP TEST	0	If selected, a current source is applied to the inverting input of the instrumentation amplifier and the non-inverting terminal is connected to VREF. Current flows out of the AMUX to the selected Inverting MUX CH# input pin. If the current encounters an open circuit in the AMUX or at the CH# pin, the voltage at the IA inverting pin will clamp. The non-inverting terminal is connected to VREF_DIV for this test. If the external sensor is properly attached, the voltage read by the ADC will be the difference of VREF_DIV and the product of the current source and the impedance of the sensor plus the impedance of the two AMUX switches encountered in the current path. The impedance of the NP_MUX can be calculated once the other impedances are known using the CONT CHECK.

Name	Default	Description
I GND	0	If selected, this action overrides the setting of the register of address 4 and causes a switch closure which shorts the inverting terminal of the instrumentation amplifier to IC GND.

The following illustration shows the calibration modes.

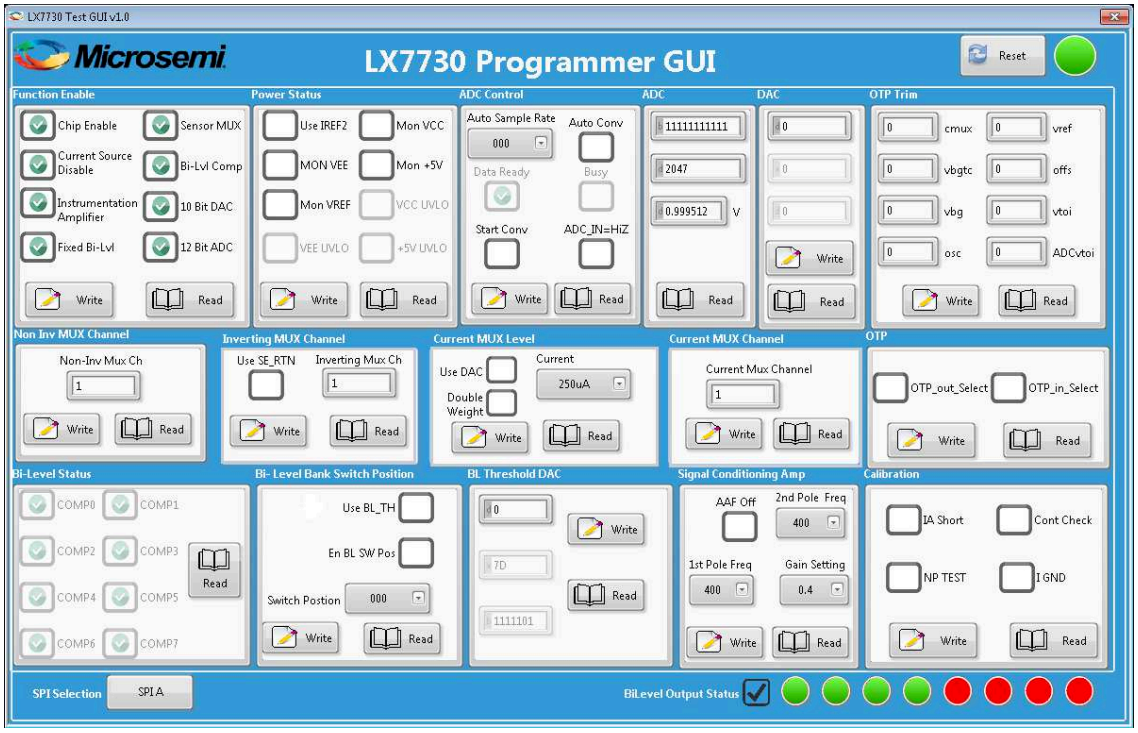
Figure 16 • Calibration



7 Programming Screen

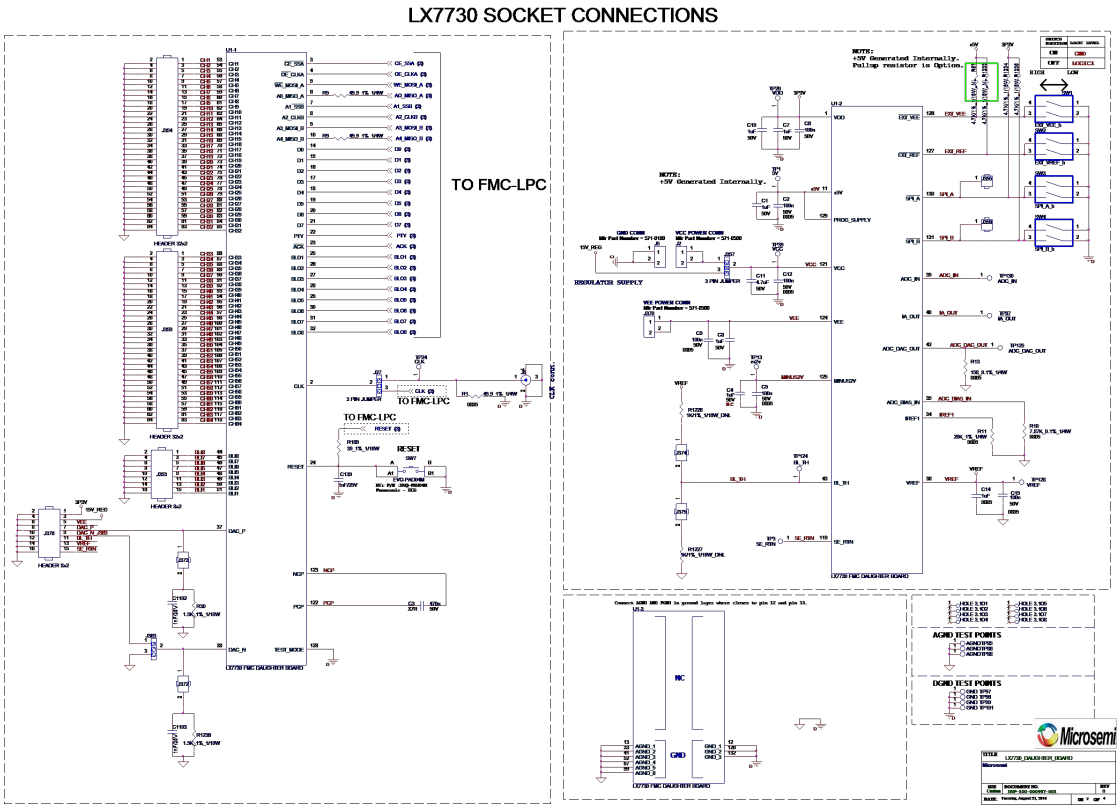
The following illustration shows the programmer GUI of the LX7730 device.

Figure 17 • Programmer GUI Screen



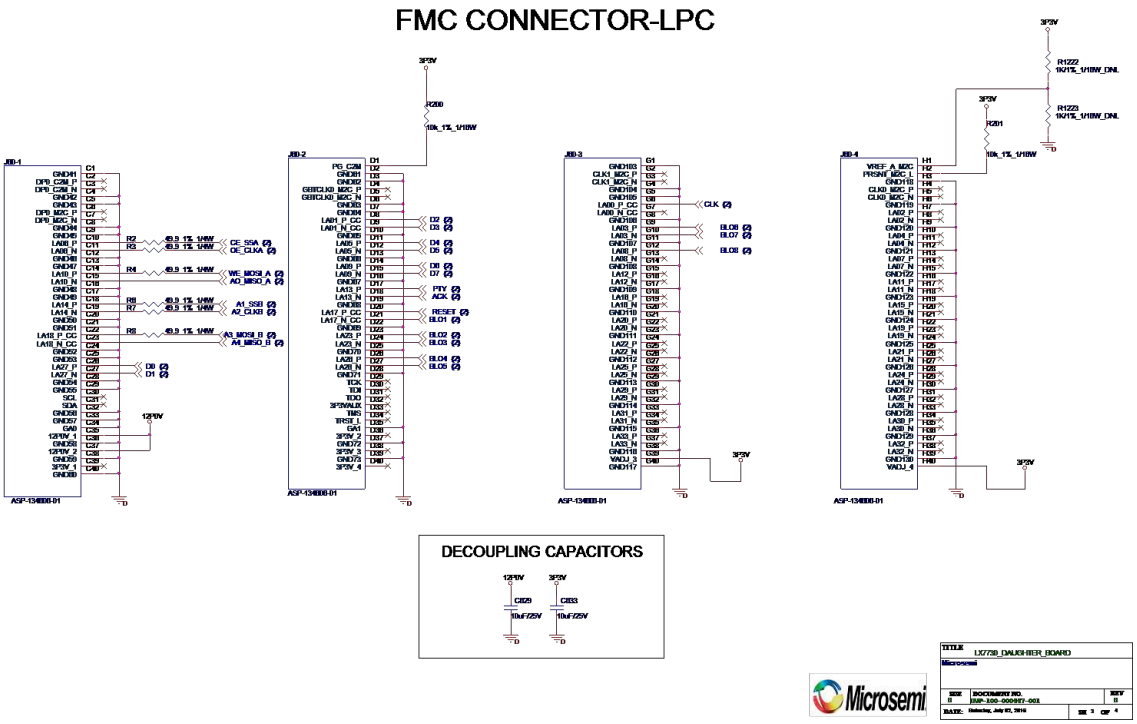
The following illustration shows the socket connections of the LX7730 device.

Figure 18 • Socket Connections



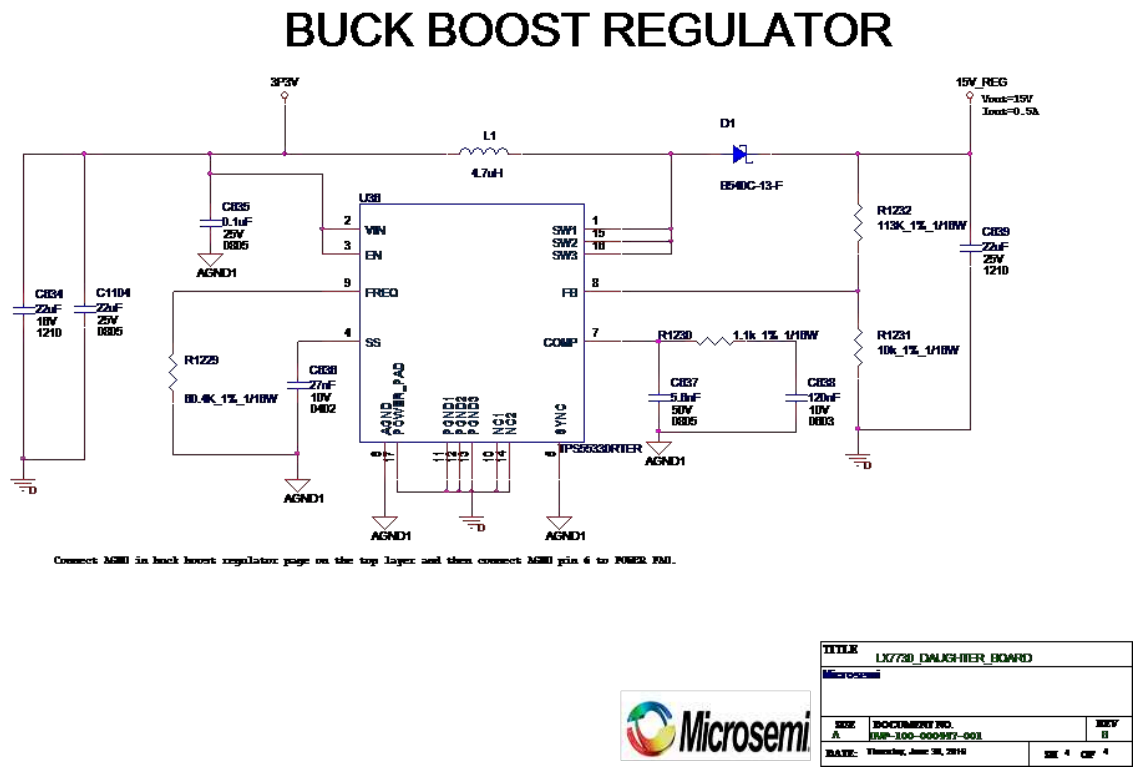
The following illustration shows the FMC connector-LPC.

Figure 19 • FMC Connector-LPC



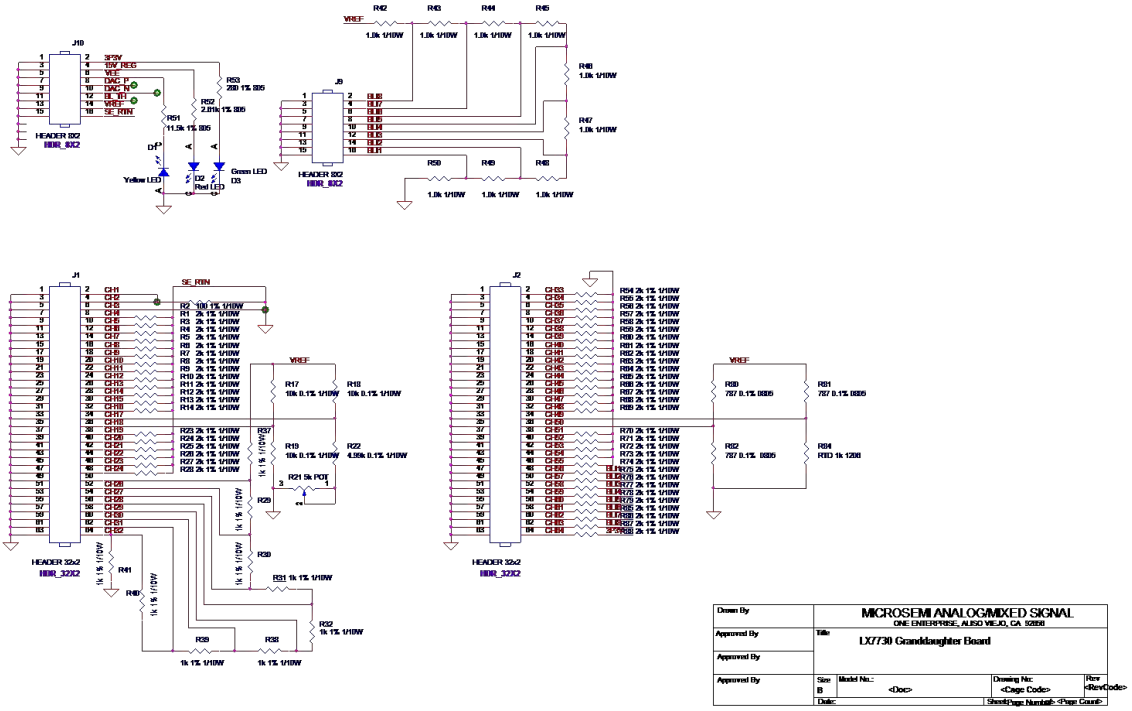
The following illustration shows the buck boost regulator.

Figure 20 • Buck Boost Regulator



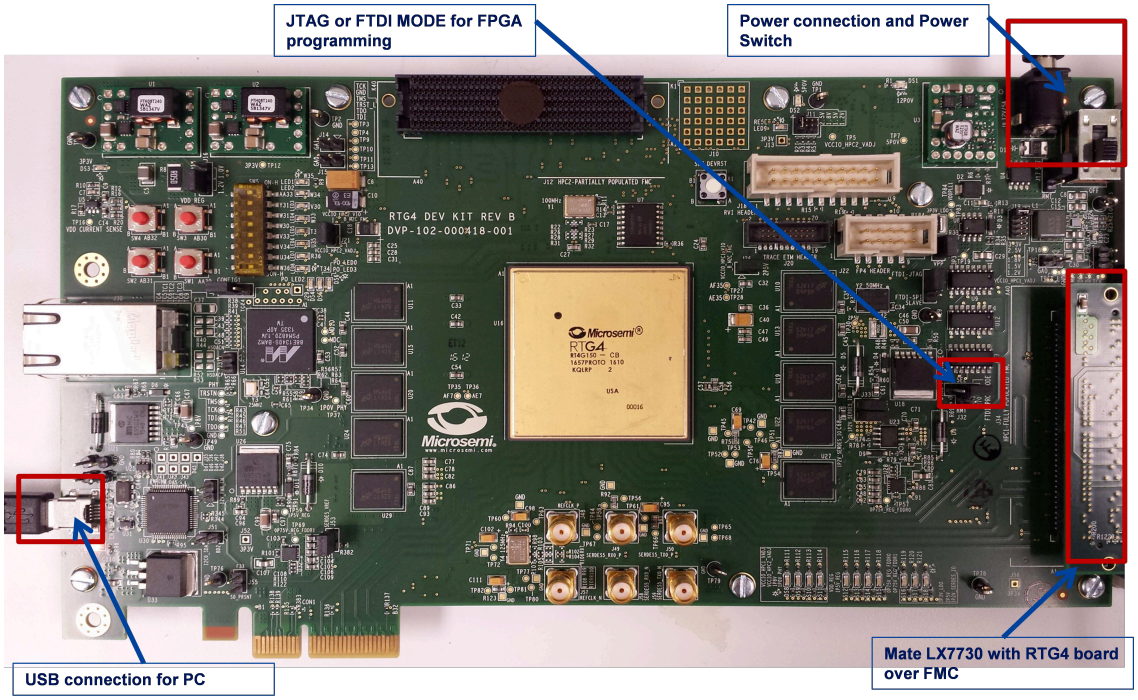
The following illustration shows the granddaughter board schematic of the LX7730 device.

Figure 21 • Granddaughter Board Schematic



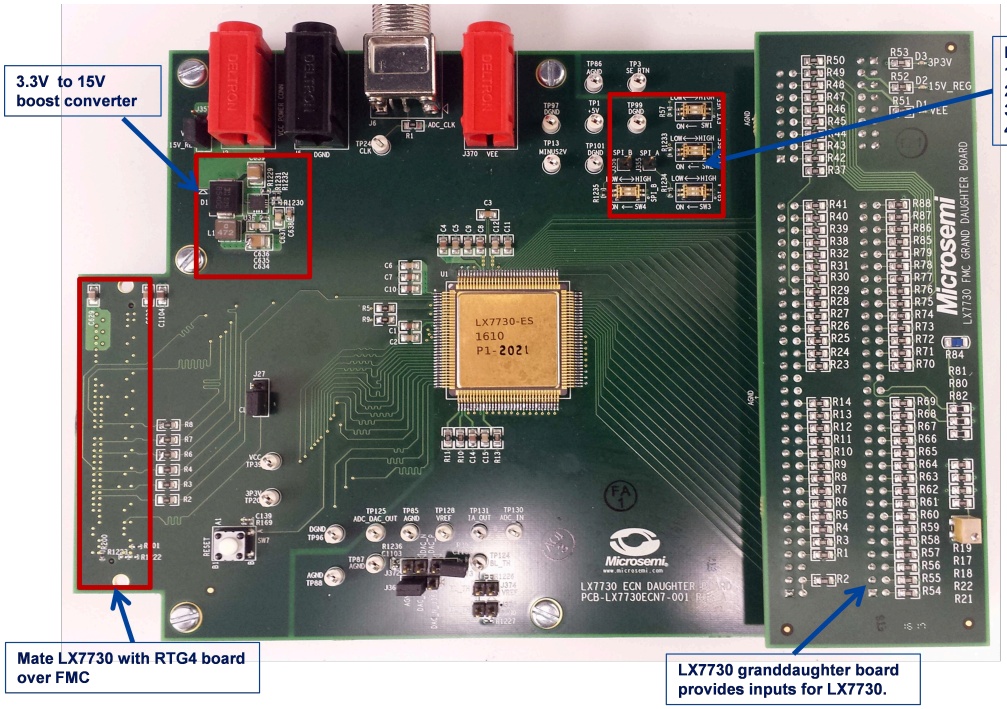
The following illustration shows the RTG4 board connector setup.

Figure 22 • RTG4 Board Connector Setup



The following illustration shows the daughter and granddaughter board connector setup.

Figure 23 • Daughter and Granddaughter Board Connector Setup



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