



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



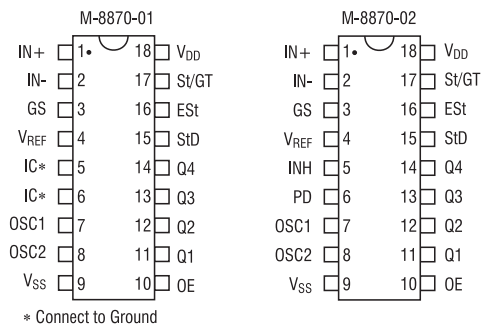
## Features

- Low Power Consumption
- Adjustable Acquisition and Release Times
- Central Office Quality and Performance
- Power-down and Inhibit Modes (-02 only)
- Inexpensive 3.58 MHz Time Base
- Single 5 Volt Power Supply
- Dial Tone Suppression

## Applications

- Telephone switch equipment
- Remote data entry
- Paging systems
- Personal computers
- Credit card systems

## Pin Configuration



## Description

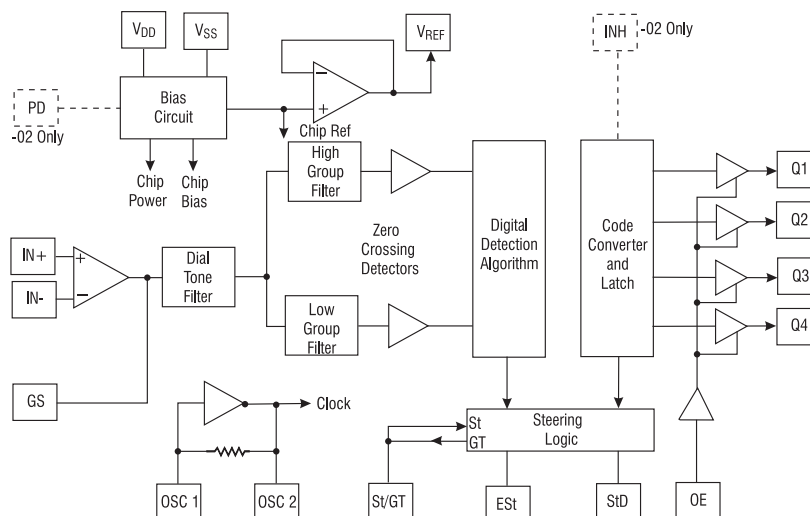
The M-8870 is a full DTMF Receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP or SOIC package. Manufactured using CMOS process technology, the M-8870 offers low power consumption (35 mW max) and precise data handling. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on-chip differential input amplifier, clock generator, and latched tri-state interface bus. Minimal external components required include a low-cost 3.579545 MHz color burst crystal, a timing resistor, and a timing capacitor.

The M-8870-02 provides a “power-down” option which, when enabled, drops consumption to less than 0.5 mW. The M-8870-02 can also inhibit the decoding of fourth column digits (see Tone Decoding table on page 5).

## Ordering Information

Part #	Description
M-8870-01	18-pin plastic DIP
M-8870-01SM	18-pin plastic SOIC
M-8870-01SMTR	18-pin plastic SOIC, tape and reel
M-8870-02	18-pin plastic DIP, power-down, option
M-8870-02SM	18-pin plastic SOIC, power-down, option
M-8870-02T	18-pin plastic SOIC, power-down option, tape and reel

## Block Diagram





## Absolute Maximum Ratings

Parameter	Symbol	Value
Power supply voltage ( $V_{DD} - V_{SS}$ )	$V_{DD}$	6.0 V max
Voltage on any pin	$V_{DC}$	$V_{SS} - 0.3, V_{DD} + 0.3$
Current on any pin	$I_{DD}$	10 mA max
Operating temperature	$T_A$	-40°C to + 85°C
Storage temperature	$T_S$	-65°C to + 150°C

**Note:**

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

*Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and effect its reliability.*

## DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating supply voltage	$V_{DD}$	4.75	-	5.25	V	-
Operating supply current	$I_{DD}$	-	3.0	7.0	mA	-
Standby supply current (see Note 3)	$I_{DDQ}$	-	-	100	$\mu$ A	$PD = V_{DD}$
Power consumption	$P_O$	-	15	35	mW	$f = 3.579$ MHz, $V_{DD} = 5.0$ V
Low level input voltage	$V_{IL}$	-	-	1.5	V	-
High level input voltage	$V_{IH}$	3.5	-	-	V	-
Input leakage current	$I_{IH}/I_{IL}$	-	0.1	-	$\mu$ A	$V_{IN} = V_{SS}$ or $V_{DD}$ (see Note 2)
Pullup (source) current on OE	$I_{SO}$	-	6.5	15.0	$\mu$ A	OE = 0 V
Input impedance, signal inputs 1, 2	$R_{IN}$	8	10	-	$m\Omega$	@ 1 kHz
Steering threshold voltage	$V_{TSt}$	2.2	-	2.5	V	-
Low level output voltage	$V_{OL}$	-	-	0.03	V	No load
High level output voltage	$V_{OH}$	$V_{DD} - 0.03$	-	-	V	No load
Output low (sink) current	$I_{OL}$	1.0	2.5	-	mA	$V_{OUT} = 0.4$ V
Output high (source) current	$I_{OH}$	0.4	0.8	-	mA	$V_{OUT} = V_{DD} - 0.4$ V
Output voltage $V_{REF}$	$V_{REF}$	2.4	-	2.7	V	No load
Output resistance $V_{REF}$	$R_{OR}$	-	10	-	$k\Omega$	-

\*Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

## Operating Characteristics - Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input leakage current	$I_N$	-	$\pm 100$	-	nA	$V_{SS} < V_{IN} < V_{DD}$
Input resistance	$R_{IN}$	4	-	-	$M\Omega$	-
Input offset voltage	$V_{OS}$	-	$\pm 25$	-	mV	-
Power supply rejection	PSRR	50	-	-	dB	1 KHz
Common mode rejection	CMRR	55	-	-	dB	$-3.0V < V_{IN} < 3.0V$
DC open loop voltage gain	$A_{VOL}$	60	-	-	dB	-
Open loop unity gain bandwidth	$f_C$	1.2	1.5	-	MHz	-
Output voltage swing	$V_O$	3.5	-	-	$V_{P-P}$	$RL \approx 100$ $k\Omega$ to $V_{SS}$
Tolerable capacitive load (GS)	$C_L$	-	-	100	pF	-
Tolerable resistive load (GS)	$R_L$	-	-	50	$k\Omega$	-
Common mode range	$V_{CM}$	2.5	-	-	$V_{P-P}$	No load

\*Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

**Notes:**

1. All voltages referenced to  $V_{SS}$  unless otherwise noted. For typical values,  $V_{DD} = 5.0V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ .

## Functional Description

M-8870 operating functions (see block diagram on page 1) include a bandsplit filter that separates the high and low tones of the received pair, and a digital decoder that verifies both the frequency and duration of the received tones before passing the resulting 4-bit code to the output bus.

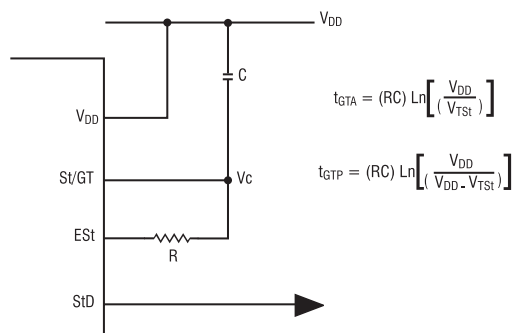
## Filter

The low and high group tones are separated by applying the dual-tone signal to the inputs of two 6th order switched capacitor bandpass filters with bandwidths that correspond to the bands enclosing the low and high group tones. The filter also incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section that smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators provided with hysteresis to prevent detection of unwanted low-level signals and noise. The comparator outputs provide full-rail logic swings at the frequencies of the incoming tones.

## Decoder

The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immunity to talkoff and tolerance to interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as signal condition), it raises the Early Steering flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

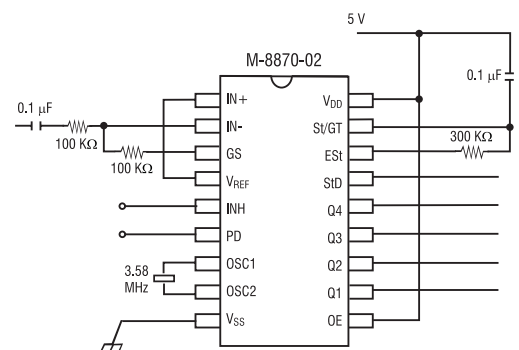
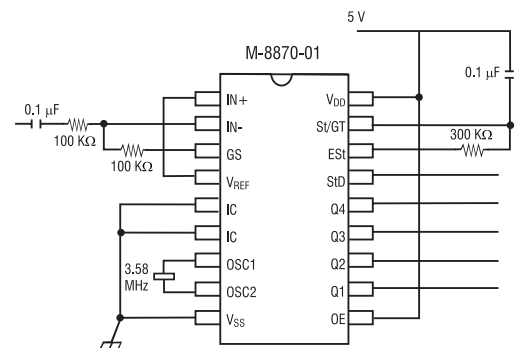
## Basic Steering Circuit



## Steering Circuit

Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as character-recognition-condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes VC (see block diagram on page 1) to rise as the capacitor discharges. Provided that signal condition is maintained (ESt remains high) for the validation period ( $t_{GTF}$ ),  $V_C$  reaches the threshold ( $V_{TSt}$ ) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (see DC Characteristics on page 2) into the output latch. At this point, the GT output is activated and drives  $V_C$  to  $V_{DD}$ . GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropouts) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

## Single-Ended Input Configuration



All resistors are  $\pm 1\%$  tolerance.  
All capacitors are  $\pm 5\%$  tolerance.

# M-8870

## Pin Functions

Pin	Name	Description
1	IN+	Non-inverting input
2	IN-	Inverting input
3	GS	Gain select. Gives access to output of front-end amplifier for connection of feedback resistor.
4	V <sub>REF</sub>	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.
5	INH*	Inhibits detection of tones representing keys A, B, C, and D.
6	PD*	Power down. Logic high powers down the device and inhibits the oscillator. Internal pulldown.
7	OSC1	Clock input
8	OSC2	Clock output
9	VSS	Negative power supply (normally connected to 0 V).
10	OE	Tri-statable output enable (input). Logic high enables the outputs Q1 - Q4. Internal pullup.
11-14	Q1, Q2, Q3, Q4	Tri-statable data outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received (see Tone Decoding table on page 5).
15	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below VTSt.
16	Est	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause Est to return to a logic low.
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of Est and the voltage on St. (See Common Crystal Connection on page 5).
18	V <sub>DD</sub>	Positive power supply. (Normally connected to +5V.)

\* -02 only. Connect to V<sub>SS</sub> for -01 version

## Guard Time Adjustment

Where independent selection of signal duration and interdigit pause are not required, the simple steering circuit of Basic Steering Circuit is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} @ 0.67 RC$$

The value of  $t_{DP}$  is a parameter of the device and  $t_{REC}$  is the minimum signal duration to be recognized by the receiver. A value for C of 0.1  $\mu$ F is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a  $t_{REC}$  of 40 ms would be 300 k $\Omega$ . A typical circuit using this steering configuration is shown in the Single - Ended Input Configuration on page 4. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present ( $t_{GTP}$ ) and tone-absent ( $t_{GTA}$ ). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause.

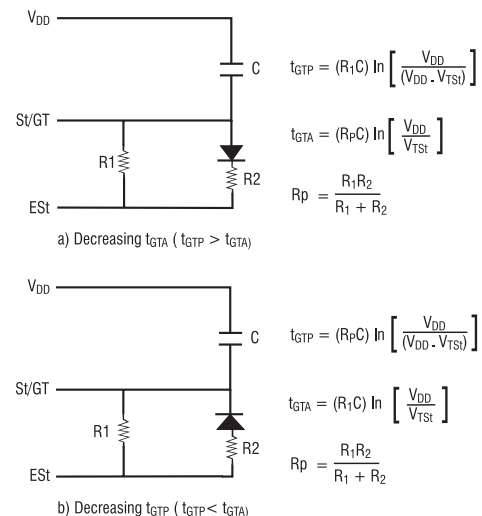
Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing  $t_{REC}$  improves talkoff performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be

registered. On the other hand, a relatively short  $t_{REC}$  with a long  $t_{DO}$  would be appropriate for extremely noisy environments where fast acquisition time and immunity to dropouts would be required. Design information for guard time adjustment is shown in the Guard Time Adjustment below.

## Power-down and Inhibit Mode (-02 only)

A logic high applied to pin 6 (PD) will place the device into standby mode to minimize power consumption. It

**Figure 5 Guard Time Adjustment**



stops the oscillator and the functioning of the filters. On the M-8870-01 models, this pin is tied to ground (logic low).

Inhibit mode is enabled by a logic high input to pin 5 (INH). It inhibits the detection of 1633 Hz. The output code will remain the same as the previous detected code (see Pin functions table on page 4). On the M-8870-01 models, this pin is tied to ground (logic low).

### Input Configuration

The input arrangement of the M-8870 provides a differential input operational amplifier as well as a bias source ( $V_{REF}$ ) to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment.

### Tone Decoding

FLOW	FHIGH	Key (ref.)	OE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	S	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
ANY	ANY	ANY	L	Z	Z	Z	Z

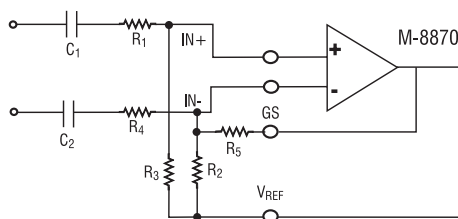
L = logic low, H = logic high, Z = high impedance

In a single-ended configuration, the input pins are connected as shown in the Single - Ended Input Configuration on page 3 with the op-amp connected for unity gain and  $V_{REF}$  biasing the input at  $1/2V_{DD}$ . The Differential Input Configuration below permits gain adjustment with the feedback resistor  $R_5$ .

### DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. The crystal can be connected to a single M-8870 as shown in the Single - Ended Input Configuration on page 3, or to a series of M-8870s. As illustrated in the Common Crystal Connection below, a single crystal can be used to connect a series of M-8870s by coupling the oscillator output of each M-8870 through a 30 pF capacitor to the oscillator input of the next M-8870.

### Differential Input Configuration



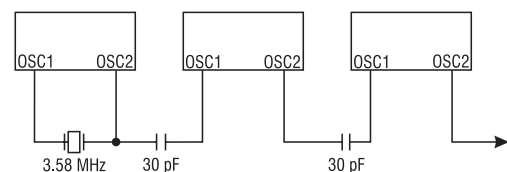
Differential Input Amplifier  
 $C_1 = C_2 = 10 \text{ nF}$   
 $R_1 = R_4 = R_5 = 100 \text{ K}\Omega$   
 $R_2 = 60 \text{ K}\Omega, R_3 = 37.5 \text{ K}\Omega$   
 $R_3 = \frac{R_2 R_5}{R_2 + R_5}$   
 Voltage Gain ( $A_v \text{ diff}$ ) =  $\frac{R_5}{R_1}$

All resistors are  $\pm 1\%$  tolerance.  
 All capacitors are  $\pm 5\%$  tolerance.

Input Impedance

$$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

### Common Crystal Connection





## AC Characteristics

Parameter	Symbol	Min	Typ*	Max	Units	Notes
Valid input signal levels (each tone of composite signal)	-	-29	-	+1	dBm	1,2,3,4,5,8
	-	27.5	-	869	mVRMS	
Positive twist accept	-	-	-	10	dB	2,3,4,8
Negative twist accept	-	-	-	10	dB	
Frequency deviation accept limit	-	-	-	$\pm 1.5\% + 2 \text{ Hz}$	Nom.	2,3,5,8,10
Frequency deviation reject limit	-	$\pm 3.5\%$	-	-	Nom.	2,3,5
Third tone tolerance	-	-25	-16	-	dB	2,3,4,5,8,9,13,14
Noise tolerance	-	-	-12	-	dB	2,3,4,5,6,8,9
Dial tone tolerance	-	+18	+22	-	dB	2,3,4,5,7,8,9
Tone present detection time	$t_{DP}$	5	8	14	ms	See Timing Diagram on page 7
Tone absent detection time	$t_{DA}$	0.5	3	8.5	ms	
Minimum tone duration accept	$t_{REC}$	-	-	40	ms	User adjustable (see Basic Steering Circuit and Guard Time Adjustment on pages 3 and 4.)
Maximum tone duration reject	$t_{\overline{REC}}$	20	-	-	ms	
Minimum interdigit pause accept	$t_{ID}$	-	-	40	ms	
Maximum interdigit pause reject	$t_{DO}$	20	-	-	ms	
Propagation delay (St to Q)	$t_{PQ}$	-	6	11	$\mu\text{s}$	OE = VDD
Propagation delay (St to StD)	$t_{PSID}$	-	9	16	$\mu\text{s}$	
Output data setup (Q to StD)	$t_{OSID}$	-	4.0	-	$\mu\text{s}$	
Propagation delay (OE to Q), enable	$t_{PTE}$	-	50	60	ns	$R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF}$
Propagation delay (OE to Q), disable	$t_{PTD}$	-	300	-	ns	
Crystal clock frequency	$f_{CLK}$	3.5759	3.5795	3.5831	MHz	-
Clock output (OSC2), capacitive load	$C_{LO}$	-	-	30	pF	-

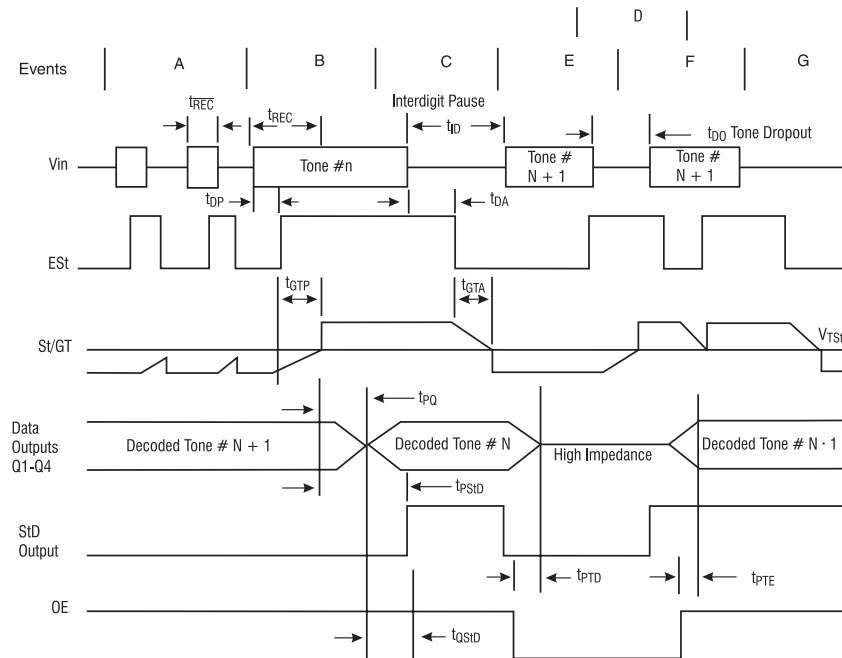
All voltages referenced to  $V_{SS}$  unless otherwise noted. For typical values  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{CLK} = 3.579545 \text{ MHz}$ .

\*Typical figures are at  $25^\circ\text{C}$  and are for design aid only; not guaranteed and not subject to production testing.

## Notes:

1. dBm = decibels above or below a reference power of 1 mW into a 600 $\Omega$  load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used, measured at GS.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 kHz) Gaussian noise.
7. The precise dial tone frequencies are (350 and 440 Hz)  $\pm 2\%$ .
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and OE.
12. External voltage source used to bias  $V_{REF}$ .
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Single - Ended Input Configuration on page 3. Input DTMF tone level at -28 dBm.

## Timing Diagram



### Explanation of Events

- (A) Tone bursts detected, tone duration invalid, outputs not updated.
- (B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
- (C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
- (D) Outputs switched to high impedance state.
- (E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
- (F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
- (G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

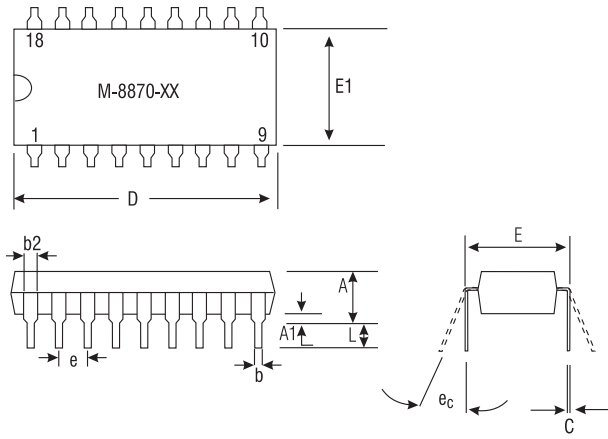
### Explanation of Symbols

VIN	DTMF composite input signal.
Est	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1 - Q4	4-bit decoded tone output.
StD	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guardtime, thus constituting a valid signal.
OE	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
$t_{REC}$	Minimum DTMF signal duration required for valid recognition.
$t_{ID}$	Minimum time between valid DTMF signals.
$t_{DO}$	Maximum allowable dropout during valid DTMF signal.
$t_{DP}$	Time to detect the presence of valid DTMF signals.
$t_{DA}$	Time to detect the absence of valid DTMF signals.
$T_{GTP}$	Guard time, tone present.
$T_{GTA}$	Guard time, tone absent.



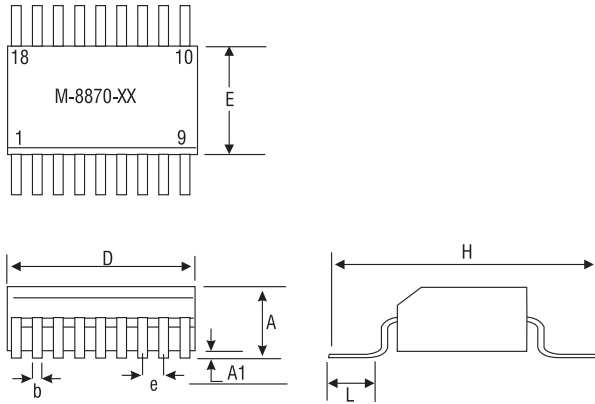
Figure 9 Mechanical Dimensions

18-Pin DIP



Tolerances for 18 - pin Dip				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	-	.210	-	5.33
A1	.015	-	.38	-
b	.014	.022	.36	.56
b2	.045	.070	1.1	1.7
C	.008	.014	.20	.36
D	.880	.920	23.35	23.37
E	.300	.325	7.62	8.26
E1	.240	.280	6.10	7.11
e	.100 BSC		2.54 BSC	
ec	0°	15°	0°	15°
L	.115	.150	2.92	3.81

18-Pin SOIC



Tolerances for 18 - pin Dip				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	.0926	.1043	2.35	2.65
A1	.0040	.0118	.10	.30
b	.013	.020	.33	.51
D	.4469	.4625	11.35	11.75
E	.2914	.2992	7.4	7.6
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	.40	1.27

Drawing not to scale.  
Does not reflect actual part marking.

Dimensions  
mm  
(inches)



### CLARE LOCATIONS

Clare Headquarters  
78 Cherry Hill Drive  
Beverly, MA 01915  
Tel: 1-978-524-6700  
Fax: 1-978-524-4900  
Toll Free: 1-800-27-CLARE

Clare Switch Division  
4315 N. Earth City Expressway  
Earth City, MO 63045  
Tel: 1-314-770-1832  
Fax: 1-314-770-1812

Clare Micronix Division  
145 Columbia  
Aliso Viejo, CA 92656-1490  
Tel: 1-949-831-4622  
Fax: 1-949-831-4628

### SALES OFFICES

#### AMERICAS

##### Americas Headquarters

Clare  
78 Cherry Hill Drive  
Beverly, MA 01915  
Tel: 1-978-524-6700  
Fax: 1-978-524-4900  
Toll Free: 1-800-27-CLARE

##### Eastern Region

Clare  
603 Apache Court  
Mahwah, NJ 07430  
Tel: 1-201-236-0101  
Fax: 1-201-236-8685  
Toll Free: 1-800-27-CLARE

##### Central Region

Clare Canada Ltd.  
3425 Harvester Road, Suite 202  
Burlington, Ontario L7N 3N1  
Tel: 1-905-333-9066  
Fax: 1-905-333-1824

##### Western Region

Clare  
1852 West 11th Street, #348  
Tracy, CA 95376  
Tel: 1-209-832-4367  
Fax: 1-209-832-4732  
Toll Free: 1-800-27-CLARE

##### Canada

Clare Canada Ltd.  
3425 Harvester Road, Suite 202  
Burlington, Ontario L7N 3N1  
Tel: 1-905-333-9066  
Fax: 1-905-333-1824

### EUROPE

#### European Headquarters

CP Clare nv  
Bampslaan 17  
B-3500 Hasselt (Belgium)  
Tel: 32-11-300868  
Fax: 32-11-300890

#### France

Clare France Sales  
Lead Rep  
99 route de Versailles  
91160 Champlan  
France  
Tel: 33 1 69 79 93 50  
Fax: 33 1 69 79 93 59

#### Germany

Clare Germany Sales  
ActiveComp Electronic GmbH  
Mitterstrasse 12  
85077 Manching  
Germany  
Tel: 49 8459 3214 10  
Fax: 49 8459 3214 29

#### Italy

C.L.A.R.E.s.a.s.  
Via C. Colombo 10/A  
I-20066 Melzo (Milano)  
Tel: 39-02-95737160  
Fax: 39-02-95738829

#### Sweden

Clare Sales  
Comptronic AB  
Box 167  
S-16329 Spånga  
Tel: 46-862-10370  
Fax: 46-862-10371

#### United Kingdom

Clare UK Sales  
Marco Polo House  
Cook Way  
Bindon Road  
Taunton  
UK-Somerset TA2 6BG  
Tel: 44-1-823 352541  
Fax: 44-1-823 352797

### ASIA/PACIFIC

#### Asian Headquarters

Clare  
Room N1016, Chia-Hsin, Bldg II,  
10F, No. 96, Sec. 2  
Chung Shan North Road  
Taipei, Taiwan R.O.C.  
Tel: 886-2-2523-6368  
Fax: 886-2-2523-6369

<http://www.clare.com>

---

*Clare, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses nor indemnity are expressed or implied. Except as set forth in Clare's Standard Terms and Conditions of Sale, Clare, Inc. assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.*

*The products described in this document are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of Clare's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. Clare, Inc. reserves the right to discontinue or make changes to its products at any time without notice.*

---

Specification: DS-M-8870-R3  
©Copyright 2001, Clare, Inc.  
All rights reserved. Printed in USA.  
7/25/01