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ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
M0519 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® M0519 Series 32-bit microcontroller is embedded with the newest ARM® Cortex®-M0 core at a cost equivalent to traditional 8-bit microcontroller for industrial control and applications which need high performance.

The NuMicro® M0519 Series embedded with the Cortex®-M0 core runs up to 72 MHz and supports a variety of industrial control and applications which need high CPU performance. The NuMicro® M0519 Series provides 128K/64K bytes embedded flash, 4 Kbytes data flash, 8 Kbytes flash for the ISP, and 16K bytes embedded SRAM. This MCU includes advanced PWM function and input capture timer which are specially designed for motor driving application. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, UART, SPI, I2C, PWM Timer, GPIO, 12-bit ADC, Low Voltage Detector and Brown-out detector. These useful functions make the NuMicro® M0519 Series powerful for a wide range of applications.

In addition, the NuMicro® M0519 Series is equipped with ISP (In-System Programming), ICP (In-Circuit Programming) functions and IAP (In-Application Programming) which allow user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Memory
  - 128K/64K bytes Flash for program memory (APROM)
  - 4KB Flash for data memory (Data Flash)
  - 8KB Flash for loader (LDROM)
  - Supports In-system program (ISP) and In-application program (IAP) application code update
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
  - 16K bytes embedded SRAM
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Supports one PLL up to 72 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock output
- Hardware divider
  - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
  - Four I/O modes:
  - TTL/Schmitt trigger input selectable
  - Bit control available
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high driver and high sink current I/O (up to 16 mA at 5V)
  - INT0 and INT1 pins with individual interrupt vectors
  - Supports up to 82/51/38 GPIOs for LQFP100/64/48 respectively
- Timers
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
  - Supports event counting function to count the event from external pin
- Watchdog Timer
  - Supports multiple clock sources from LIRC(default selection) and HCLK/2048
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Time-out reset delay period time can be selected
- Window Watchdog Timer

- Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
- Window set by 6-bit counter with 11-bit prescale
- Able to wake up from Power-down or Idle mode

- Basic PWM
  - 1 unit of 16-bit basic PWM, up to 2ch output
  - Alternative function as input capture timer
- Enhanced PWM
  - 2 units of 16-bit enhanced PWM, up to 6ch output with dead-zone control, brake and polarity control for motor drive
  - Default tri-state during any reset
- Enhanced Input Capture
  - Up to 2 units of 24-bit input capture
  - Each unit has 3 inputs: ECAPx_IC0, ECAPx_IC1 and ECAPx_IC2
- UART
  - Up to two 16550 compatible UART devices
  - Programmable baud-rate generator
  - Buffered receiving and transmitting, each with 16 bytes FIFO
  - Supports flow control (TX, RX, CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS-485
- SPI
  - Up to three sets of SPI device
  - Supports SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Supports Byte Suspend mode in 32-bit transmission
- I^2C
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters
  - Programmable clocks allow versatile rate control
  - Multiple address recognition (four slave address with mask option)
- ADC
  - Two A/D converters
  - Each ADC with up to 8 channel, 12-bit resolution with 10-bit accuracy
  - 16 result registers
  - Sampling rate up to 800ksps
  - Two operating modes:
    - Single Sampling mode: Only one specified channel can be sampled at one time.
    - Simultaneous Sampling mode: Allowing two ADC channels to be sampled simultaneously.
  - Two converting result digital comparators
  - Conversion start by software, external pins, or linked with Timer 0~3 or PWM module
- Up to three Analog Comparators
- Up to two OPA (operational amplifier)

- Brown-out detector
  - 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Optional brown-out interrupt or reset
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Low Voltage Reset
- 96-bit unique ID
- Operating Temperature: -40℃~105℃
- Develop tools: parallel writer or In-Circuit Programming (ICP) writer
- Packages:
  - All Green package (RoHS)
  - LQFP 100/64/48-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® M0519 Selection Guide

4.1.1 NuMicro® M0519 Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	LDROM (KB)	I/O	Timer (32-Bit)	Connectivity				QEI	Capture	PWM	ADC (12-Bit)	OPA	Comp.	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN								
M0519LD3AE	64	16	4	8	38	4	2	1	1	2	-	-	6	16	-	2	v	LQFP48
M0519LE3AE	128	16	Config.	8	38	4	2	1	1	2	-	-	6	16	-	2	v	LQFP48
M0519SD3AE	64	16	4	8	51	4	2	2	1	2	-	-	10	16	1	2	v	LQFP64
M0519SE3AE	128	16	Config.	8	51	4	2	2	1	2	-	-	10	16	1	2	v	LQFP64
M0519VE3AE	128	16	Config.	8	82	4	2	3	1	2	-	6	14	16	2	3	v	LQFP100

4.1.2 NuMicro® M0519 Naming Rule

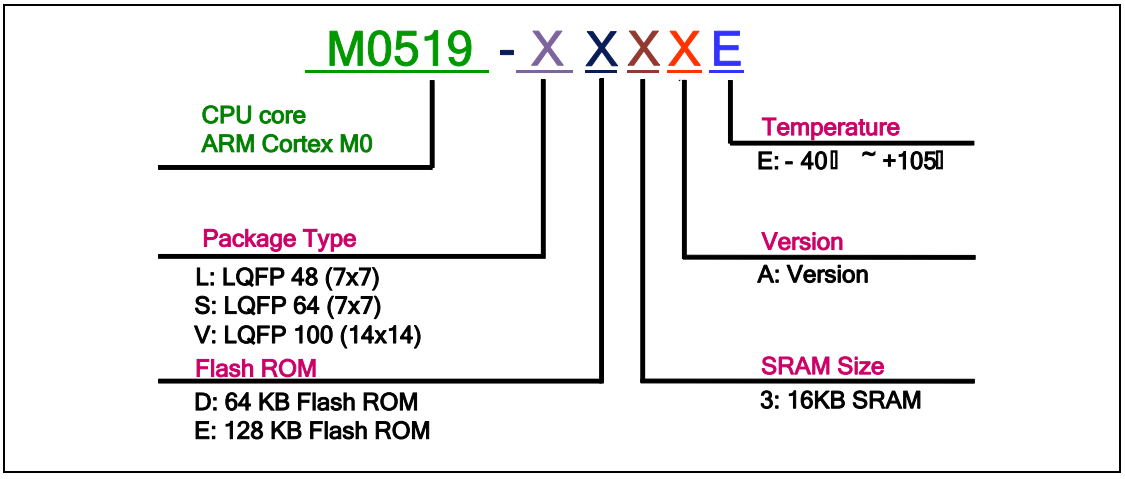

Figure 4-1 NuMicro® M0519 Selection Code

4.2 Pin Configuration

4.2.1 LQFP 100-pin

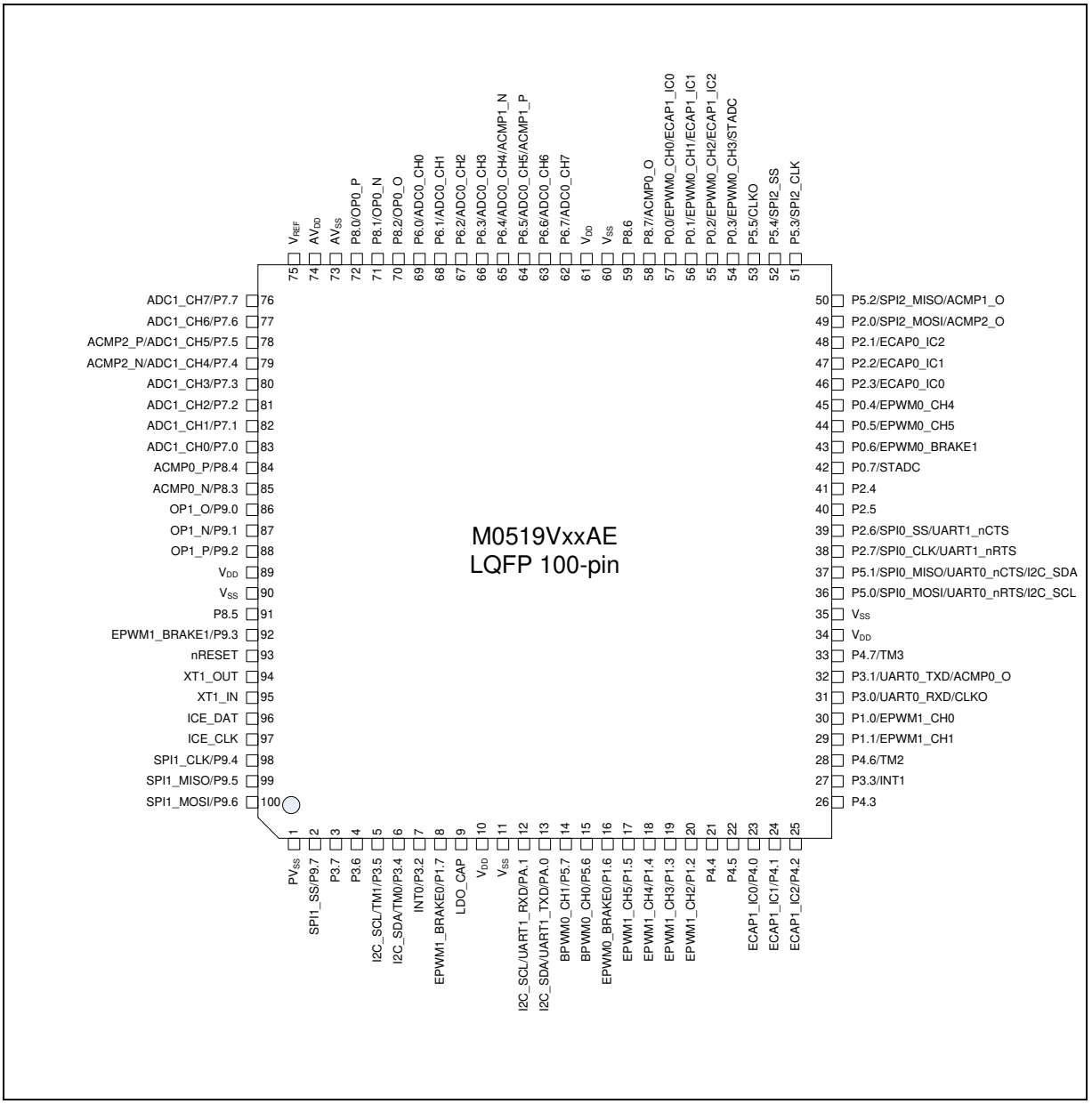

Figure 4-2 NuMicro® M0519VxxAE Series LQFP-100 Pin Diagram

4.2.2 LQFP 64-pin

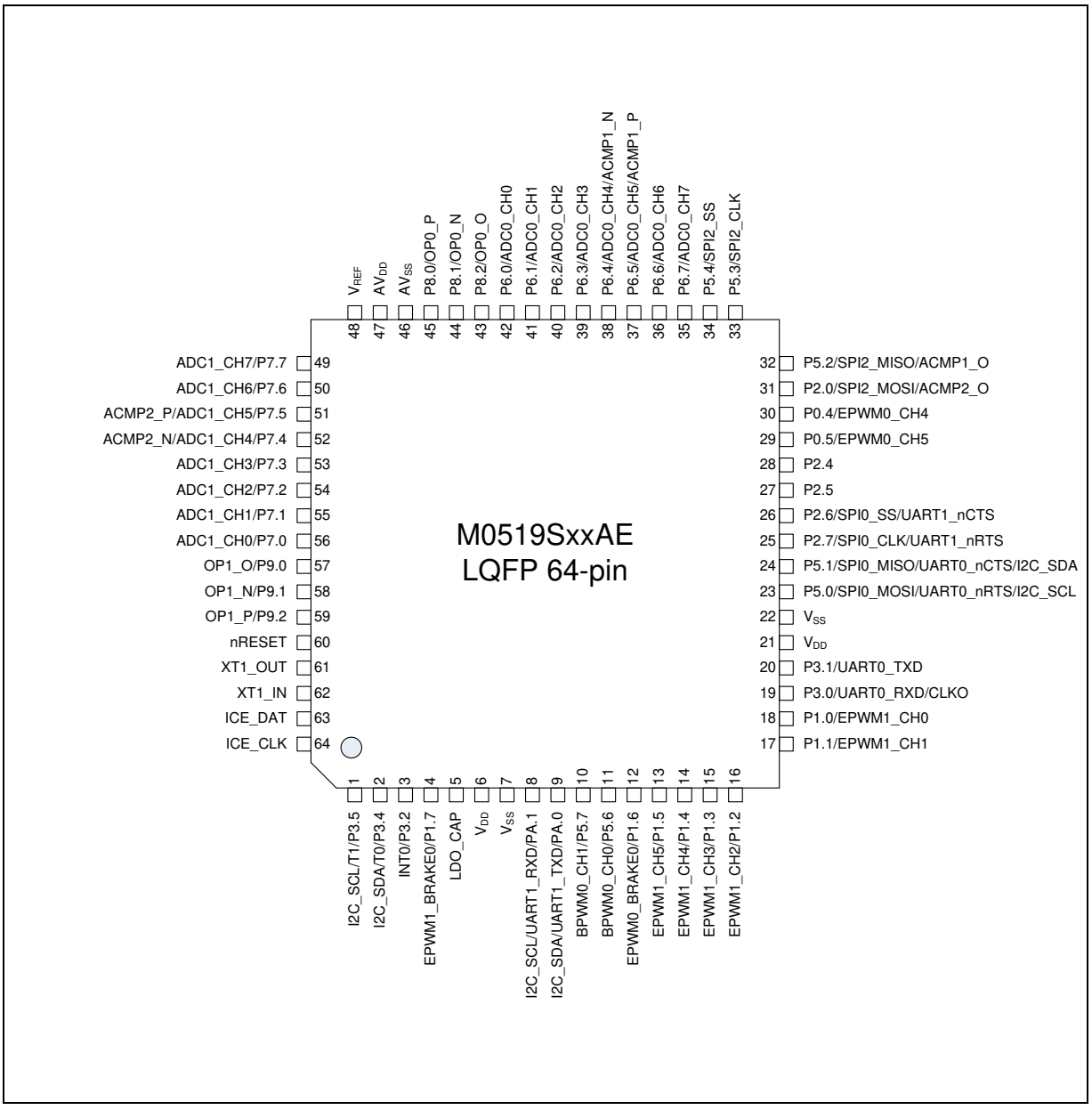

Figure 4-3 NuMicro® M0519SxxAE Series LQFP-64 Pin Diagram

4.2.3 LQFP 48-pin

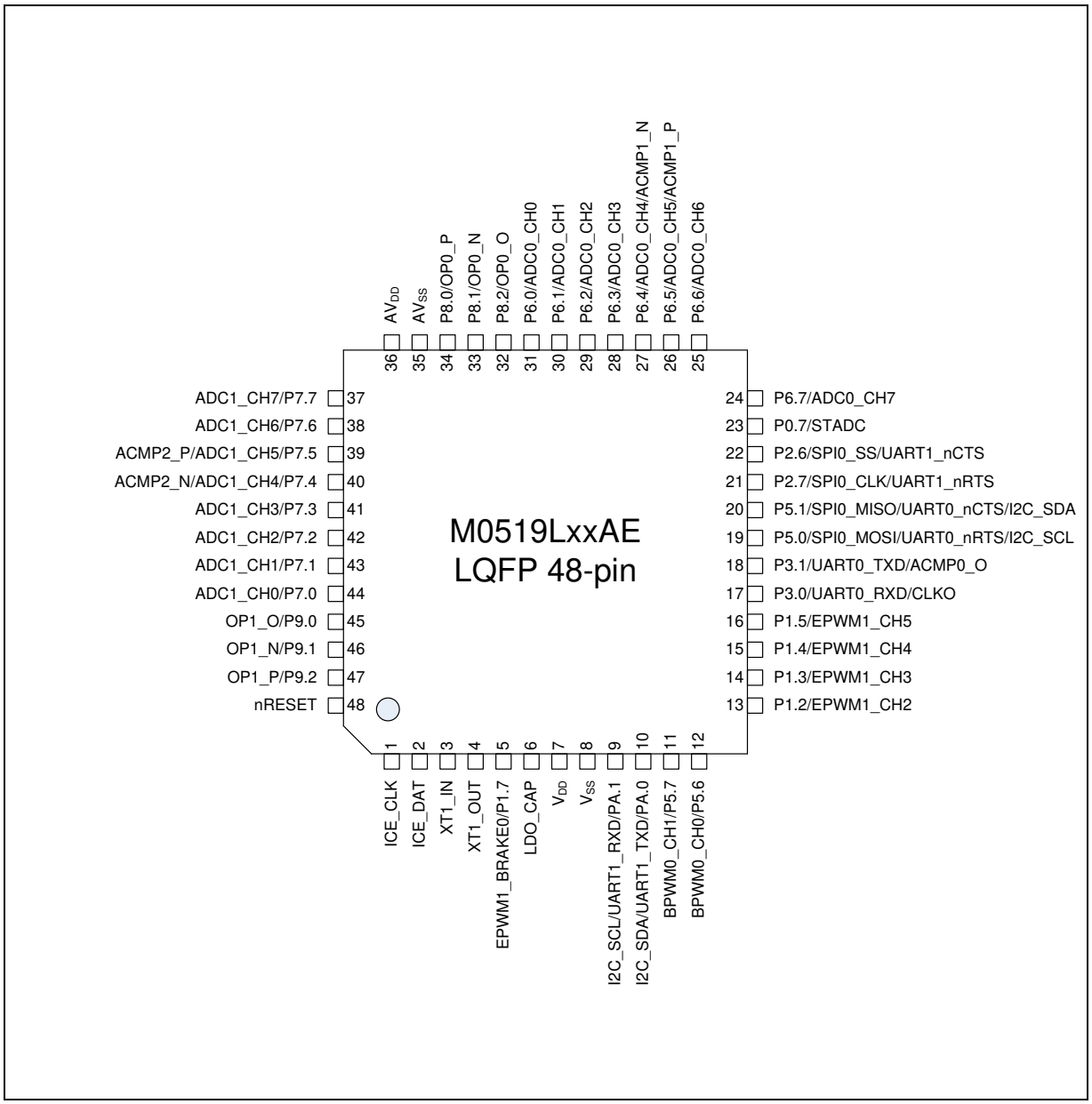

Figure 4-4 NuMicro® M0519LxxAE Series LQFP-48 Pin Diagram

4.3 Pin Description

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
10	6	7	V_{DD}	**P**	**POWER SUPPLY:** Supply voltage **Digital** V_{DD} for operation.
34					
61	21				
89					
11	7	8	V_{SS}	**P**	**GROUND:** Digital Ground potential.
35					
60	22				
90					
9	5	6	LDO_CAP	**P**	**LDO:** LDO output pin **Note: It needs to be connected with a 1uF capacitor.**
1	-	-	PV_{SS}	**P**	**PLL GROUND: PLL** Ground potential.
74	47	36	AV_{DD}	**AP**	Power supply for internal analog circuit
73	46	35	AV_{SS}	**AP**	Ground Pin for analog circuit
75	48	-	V_{REF}	**AP**	Voltage reference input for ADC **Note: It needs to be connected with a 1uF capacitor.**
93	60	48	nRESET	**I (ST)**	**RESET:** nRESET pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
94	61	4	XT1_OUT	**O**	**CRYSTAL OUT:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XT1_IN.
95	62	3	XT1_IN	**I (ST)**	**CRYSTAL IN:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
96	63	2	ICE_DAT	**I/O**	Serial Wired Debugger Data pin
97	64	1	ICE_CLK	**I**	Serial Wired Debugger Clock pin
57	-	-	P0.0	**I/O**	General purpose digital I/O pin
			PWM0_CH0	**O**	PWM0 output of PWM Unit 0
			ECAP1_IC0	**I**	Input 0 of Enhanced Input Capture Unit 1
56	-	-	P0.1	**I/O**	General purpose digital I/O pin
			PWM0_CH1	**O**	PWM1 output of PWM Unit 0
			ECAP1_IC1	**I**	Input 1 of Enhanced Input Capture Unit 1
55	-	-	P0.2	**I/O**	General purpose digital I/O pin
			PWM0_CH2	**O**	PWM2 output of PWM Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
54	-	-	P0.3	I/O	General purpose digital I/O pin
			PWM0_CH3	O	PWM3 output of PWM Unit 0
			STADC	I	ADC external trigger input
45	30	-	P0.4	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM Unit 0
44	29	-	P0.5	I/O	General purpose digital I/O pin
			PWM0_CH5	O	PWM5 output of PWM Unit 0
43	-	-	P0.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE1	I	Brake input pin 1 of PWM Unit 0
42	-	23	P0.7	I/O	General purpose digital I/O pin
			STADC	I	ADC external trigger input
30	18	-	P1.0	I/O	General purpose digital I/O pin
			PWM1_CH0	O	PWM0 output of PWM Unit 1
29	17	-	P1.1	I/O	General purpose digital I/O pin
			PWM1_CH1	O	PWM1 output of PWM Unit 1
20	16	13	P1.2	I/O	General purpose digital I/O pin
			PWM1_CH2	O	PWM2 output of PWM Unit 1
19	15	14	P1.3	I/O	General purpose digital I/O pin
			PWM1_CH3	O	PWM3 output of PWM Unit 1
18	14	15	P1.4	I/O	General purpose digital I/O pin
			PWM1_CH4	O	PWM4 output of PWM Unit 1
17	13	16	P1.5	I/O	General purpose digital I/O pin
			PWM1_CH5	O	PWM5 output of PWM Unit 1
16	12	-	P1.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE0	I	Brake input pin 0 of PWM Unit 0
8	4	5	P1.7	I/O	General purpose digital I/O pin
			PWM1_BRAKE0	I	Brake input pin0 of PWM Unit 1
49	31	-	P2.0	I/O	General purpose digital I/O pin
			SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin
			ACMP2_O	AO	Analog comparator 2 output pin
48	-	-	P2.1	I/O	General purpose digital I/O pin
			ECAP0_IC2	I	Input 2 of Enhanced Input Capture Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
47	-	-	P2.2	I/O	General purpose digital I/O pin
			ECAP0_IC1	I	Input 1 of Enhanced Input Capture Unit 0
46	-	-	P2.3	I/O	General purpose digital I/O pin
			ECAP0_IC0	I	Input 0 of Enhanced Input Capture Unit 0
41	28	-	P2.4	I/O	General purpose digital I/O pin
40	27	-	P2.5	I/O	General purpose digital I/O pin
39	26	22	P2.6	I/O	General purpose digital I/O pin
			SPI0_SS	I/O	SPI0 slave select pin
			UART1_nCTS	I	UART1 CTS pin
38	25	21	P2.7	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI0 serial clock pin
			UART1_nRTS	O	UART1 RTS pin
31	19	17	P3.0	I/O	General purpose digital I/O pin
			UART0_RXD	I	Data Receiver input pin for UART0
32	20	18	P3.1	I/O	General purpose digital I/O pin
			UART0_TXD	O	Data transmitter output pin for UART0
			ACMP0_O	AO	Analog comparator 0 output
7	3	-	P3.2	I/O	General purpose digital I/O pin
			INT0	I	External Interrupt 0 input pin
27	-	-	P3.3	I/O	General purpose digital I/O pin
			INT1	I	External Interrupt 1 input pin
6	2	-	P3.4	I/O	General purpose digital I/O pin
			TM0	I/O	Timer0 external clock
			I2C0_SDA	I/O	I2C0 data input/output pin
5	1	-	P3.5	I/O	General purpose digital I/O pin
			TM1	I/O	Timer1 external clock
			I2C0_SCL	I/O	I2C0 clock output pin
4	-	-	P3.6	I/O	General purpose digital I/O pin
3	-	-	P3.7	I/O	General purpose digital I/O pin
23	-	-	P4.0	I/O	General purpose digital I/O pin
			ECAP1_IC0	I	Input 0 of Enhanced Input Capture Unit 1
24	-	-	P4.1	I/O	General purpose digital I/O pin
			ECAP1_IC1	I	Input 1 of Enhanced Input Capture Unit 1

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
25	-	-	P4.2	I/O	General purpose digital I/O pin
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
26	-	-	P4.3	I/O	General purpose digital I/O pin
21	-	-	P4.4	I/O	General purpose digital I/O pin
22	-	-	P4.5	I/O	General purpose digital I/O pin
28	-	-	P4.6	I/O	General purpose digital I/O pin
			TM2	I/O	Timer2 external clock
33	-	-	P4.7	I/O	General purpose digital I/O pin
			TM3	I/O	Timer3 external clock
36	23	19	P5.0	I/O	General purpose digital I/O pin
			SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin
			UART0_nRTS	O	UART0 RTS pin
37	24	20	P5.1	I/O	General purpose digital I/O pin
			SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin
			UART0_nCTS	I	UART0 CTS pin
50	32	-	P5.2	I/O	General purpose digital I/O pin
			SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin
			ACMP1_O	AO	Analog comparator 1 output pin
51	33	-	P5.3	I/O	General purpose digital I/O pin
			SPI2_CLK	I/O	SPI2 serial clock pin
52	34	-	P5.4	I/O	General purpose digital I/O pin
			SPI2_SS	I/O	SPI2 slave select pin
53	-	-	P5.5	I/O	General purpose digital I/O pin
			CLKO	O	Frequency Divider output pin
15	11	12	P5.6	I/O	General purpose digital I/O pin
			PWM2_CH0	I/O	PWM0 output of PWM unit 2
14	10	11	P5.7	I/O	General purpose digital I/O pin
			PWM2_CH1	I/O	PWM1 output of PWM unit 2
69	42	31	P6.0	I/O	General purpose digital I/O pin
			ADC0_CH0	AI	ADC analog input 0 for sample-and-hold A
68	41	30	P6.1	I/O	General purpose digital I/O pin
			ADC0_CH1	AI	ADC analog input 1 for sample-and-hold A
67	40	29	P6.2	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ADC0_CH2	AI	ADC analog input 2 for sample-and-hold A
66	39	28	P6.3	I/O	General purpose digital I/O pin
			ADC0_CH3	AI	ADC analog input 3 for sample-and-hold A
65	38	27	P6.4	I/O	General purpose digital I/O pin
			ADC0_CH4	AI	ADC analog input 4 for sample-and-hold A
			ACMP1_N	AI	Analog comparator 1 negative input
64	37	26	P6.5	I/O	General purpose digital I/O pin
			ADC0_CH5	AI	ADC analog input 5 for sample-and-hold A
			ACMP1_P	AI	Analog comparator 1 positive input
63	36	25	P6.6	I/O	General purpose digital I/O pin
			ADC0_CH6	AI	ADC analog input 6 for sample-and-hold A
62	35	24	P6.7	I/O	General purpose digital I/O pin
			ADC0_CH7	AI	ADC analog input 7 for sample-and-hold A
83	56	44	P7.0	I/O	General purpose digital I/O pin
			ADC1_CH0	AI	ADC analog input 0 for sample-and-hold B
82	55	43	P7.1	I/O	General purpose digital I/O pin
			ADC1_CH1	AI	ADC analog input 1 for sample-and-hold B
81	54	42	P7.2	I/O	General purpose digital I/O pin
			ADC1_CH2	AI	ADC analog input 2 for sample-and-hold B
80	53	41	P7.3	I/O	General purpose digital I/O pin
			ADC1_CH3	AI	ADC analog input 3 for sample-and-hold B
79	52	40	P7.4	I/O	General purpose digital I/O pin
			ADC1_CH4	AI	ADC analog input 4 for sample-and-hold B
			ACMP2_N	AI	Analog comparator 2 negative input
78	51	39	P7.5	I/O	General purpose digital I/O pin
			ADC1_CH5	AI	ADC analog input 5 for sample-and-hold B
			ACMP2_P	AI	Analog comparator 2 positive input
77	50	38	P7.6	I/O	General purpose digital I/O pin
			ADC1_CH6	AI	ADC analog input 6 for sample-and-hold B
76	49	37	P7.7	I/O	General purpose digital I/O pin
			ADC1_CH7	AI	ADC analog input 7 for sample-and-hold B
72	45	34	P8.0	I/O	General purpose digital I/O pin
			OP0_P	AI	OP Amplifier 0 positive input

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
71	44	33	P8.1	I/O	General purpose digital I/O pin
			OP0_N	AI	OP Amplifier 0 negative input
70	43	32	P8.2	I/O	General purpose digital I/O pin
			OP0_O	AO	OP Amplifier 0 output
85	-	-	P8.3	I/O	General purpose digital I/O pin
			ACMP0_N	AI	Analog comparator negative input pin
84	-	-	P8.4	I/O	General purpose digital I/O pin
			ACMP0_P	AI	Analog comparator positive input pin
91	-	-	P8.5	I/O	General purpose digital I/O pin
59	-	-	P8.6	I/O	General purpose digital I/O pin
58	-	-	P8.7	I/O	General purpose digital I/O pin
			ACMP0_O	O	Analog comparator output pin
86	57	45	P9.0	I/O	General purpose digital I/O pin
			OP1_O	AO	OP Amplifier 1 output
87	58	46	P9.1	I/O	General purpose digital I/O pin
			OP1_N	AI	OP Amplifier 1 negative input
88	59	47	P9.2	I/O	General purpose digital I/O pin
			OP1_P	AI	OP Amplifier 1 positive input
92	-	-	P9.3	I/O	General purpose digital I/O pin
			PWM1_BRAKE1	I	Brake input pin 1 of PWM Unit 1
98	-	-	P9.4	I/O	General purpose digital I/O pin
			SPI1_CLK	I/O	SPI1 serial clock pin
99	-	-	P9.5	I/O	General purpose digital I/O pin
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin
100	-	-	P9.6	I/O	General purpose digital I/O pin
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin
2	-	-	P9.7	I/O	General purpose digital I/O pin
			SPI1_SS	I/O	SPI1 slave select pin
13	9	10	PA.0	I/O	General purpose digital I/O pin
			UART1_TXD	O	Data transmitter output pin for UART1
			I2C0_SDA	I/O	I2C0 data input/output pin
12	8	9	PA.1	I/O	General purpose digital I/O pin
			UART1_RXD	I	Data Receiver input pin for UART1

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			I2C0_SCL	I/O	I2C0 clock output pin

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

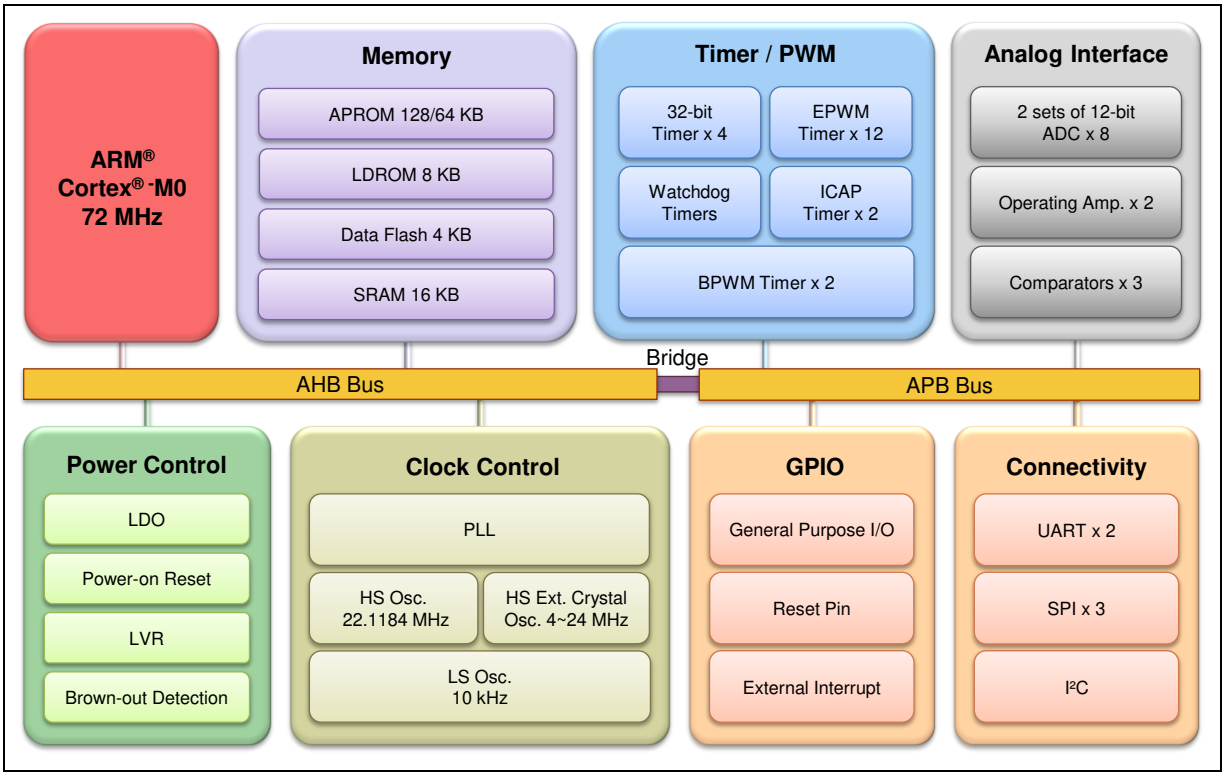

Figure 5-1 NuMicro® M0519 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

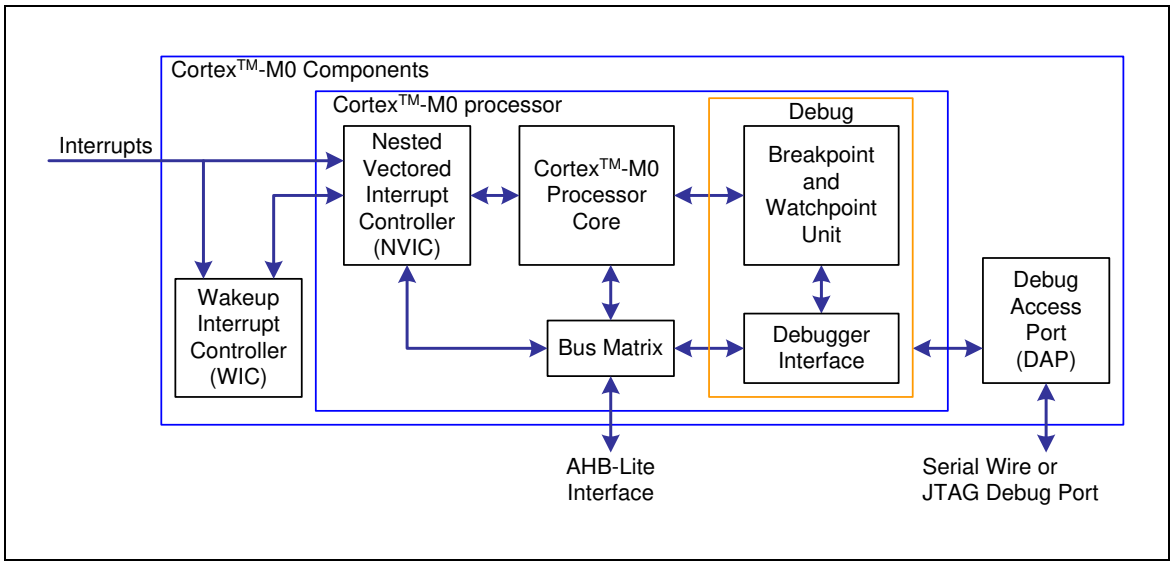

Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)