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ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
M052/M054BN Datasheet

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1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M052/M054 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M052/M054 has 8K/16K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M052/M054 in order to reduce component count, board space and system cost. These useful functions make the M052/M054 powerful for a wide range of applications.

Additionally, the M052/M054 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 8KB/16KB Flash memory for program memory (APROM)
  - 4KB Flash memory for data memory (DataFlash)
  - 4KB Flash memory for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 4~24 MHz external crystal input
  - 22.1184 MHz internal oscillator (trimmed to 3% accuracy)
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
  - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output

- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode

- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function equivalent to 8051 Timer2.
- Watchdog Timer
  - Multiple clock sources
  - Supports wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
- UART

- Up to two sets of UART device
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function

- SPI
  - Up to two sets of SPI device.
  - Supports master/slave mode
  - Full duplex synchronous serial data transfer
  - Provide 3 wire function
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx latching data can be either at rising edge or at falling edge of serial clock
  - Tx sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte suspend mode in 32-bit transmission
- I^2C
  - Supports master/slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC with 760k SPS
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
  - Supports 2' complement/un-signed format in differential mode conversion result
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion can be started either by software trigger or external pin trigger
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal band gap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Supports 8-bit/16-bit data width
  - Supports byte-write in 16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- One built-in temperature sensor with 1°C resolution
- Brown-Out Detector
  - With 4 levels: 4.3V/3.7V/2.7V/2.2V

- Supports Brown-Out interrupt and reset option

- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP, 33-pin QFN

3 BLOCK DIAGRAM

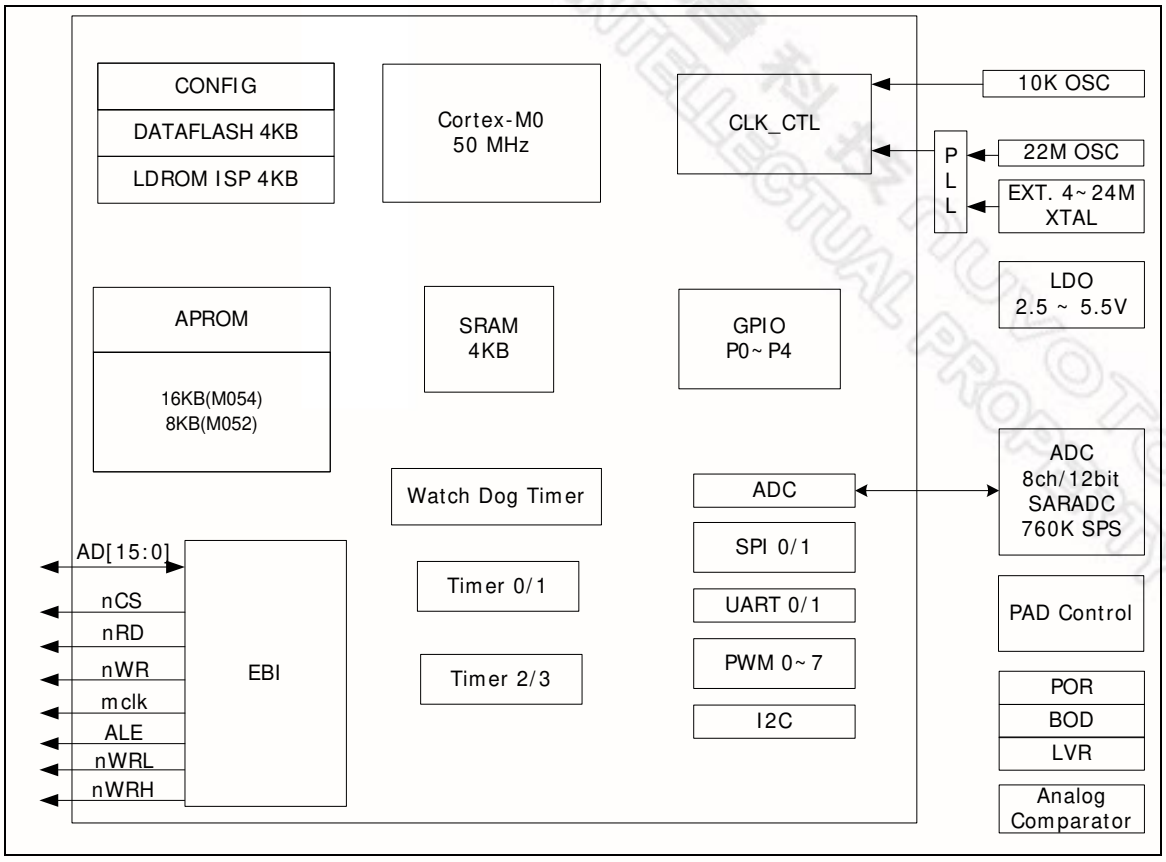

Figure 3-1 NuMicro™ M051 Series Block Diagram

4 SELECTION TABLE

NuMicro M051™ Series Selection Guide

Part number	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			COMP	PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C						
M052LBN	8KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M052ZBN	8KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33
M054LBN	16KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M054ZBN	16KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33

Table 4-1 NuMicro™ M051 Series Product Selection Guide

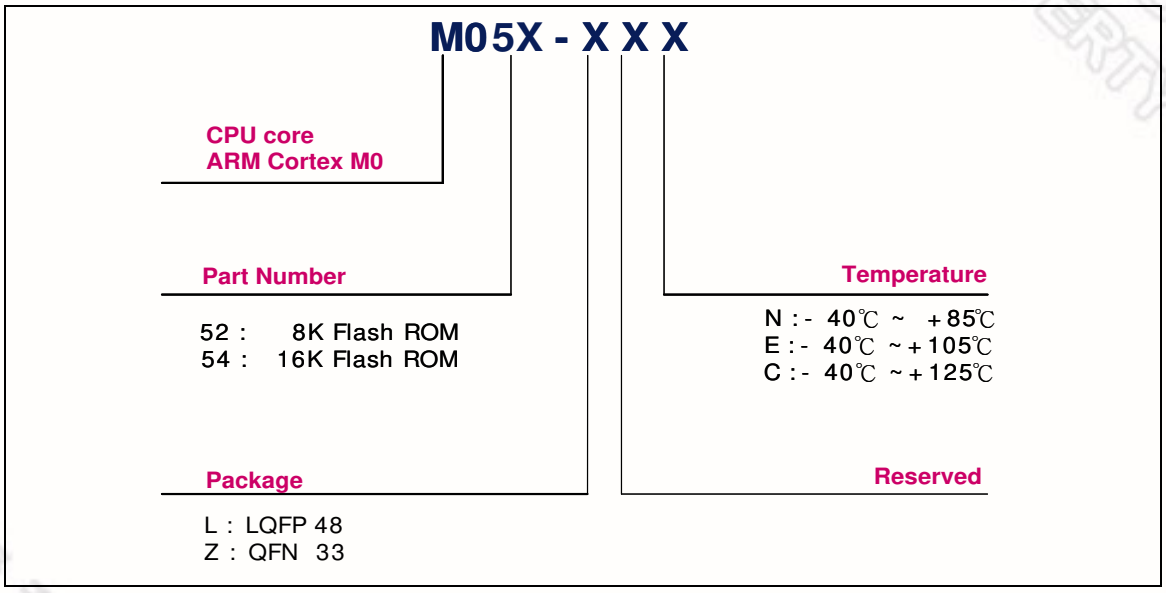

Figure 4-1 NuMicro™ Naming Rule

5 PIN CONFIGURATION

5.1 QFN 33 pin

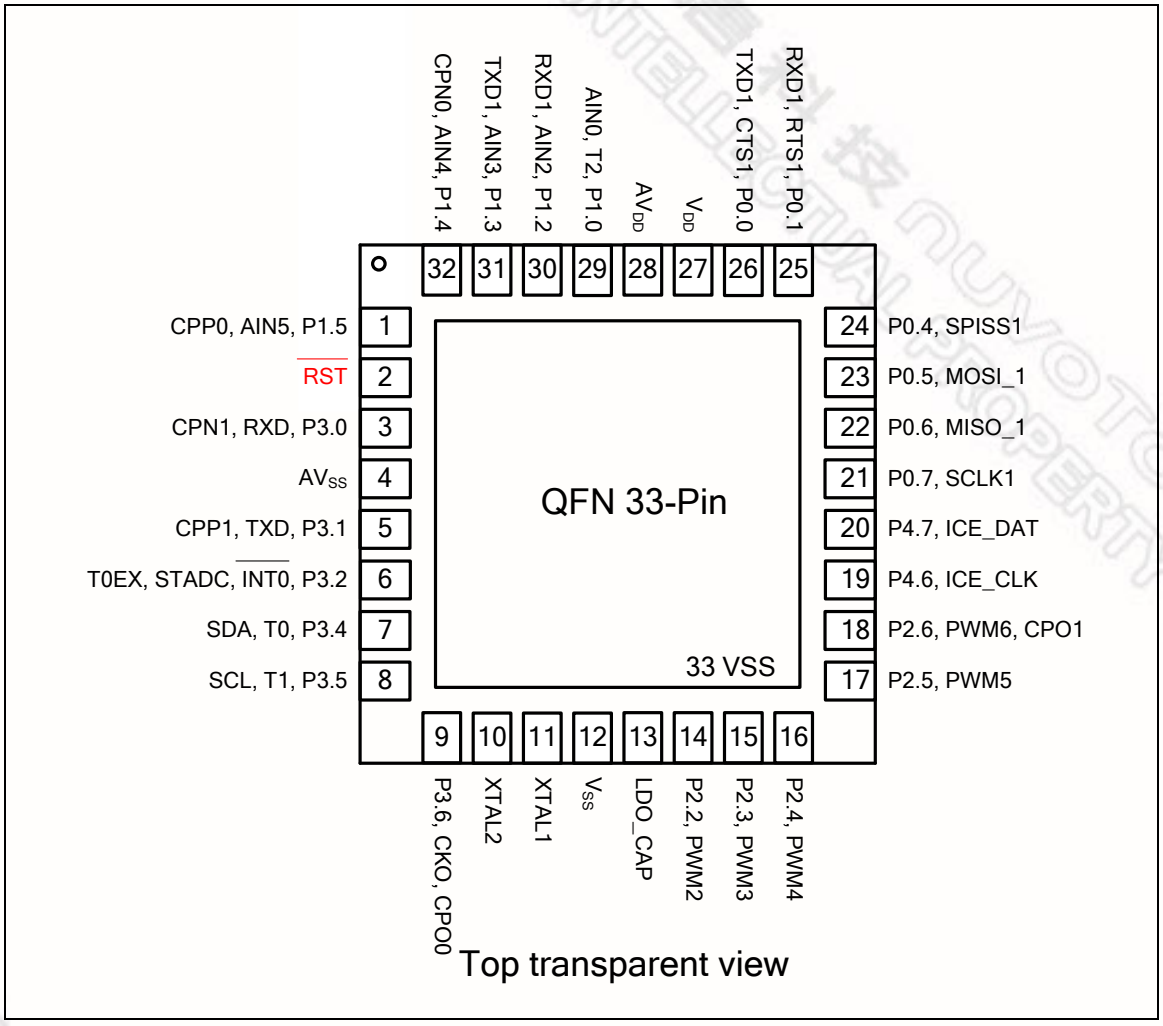

Figure 5-1 NuMicro™ M051 Series QFN33 Pin Diagram

5.2 LQFP 48 pin

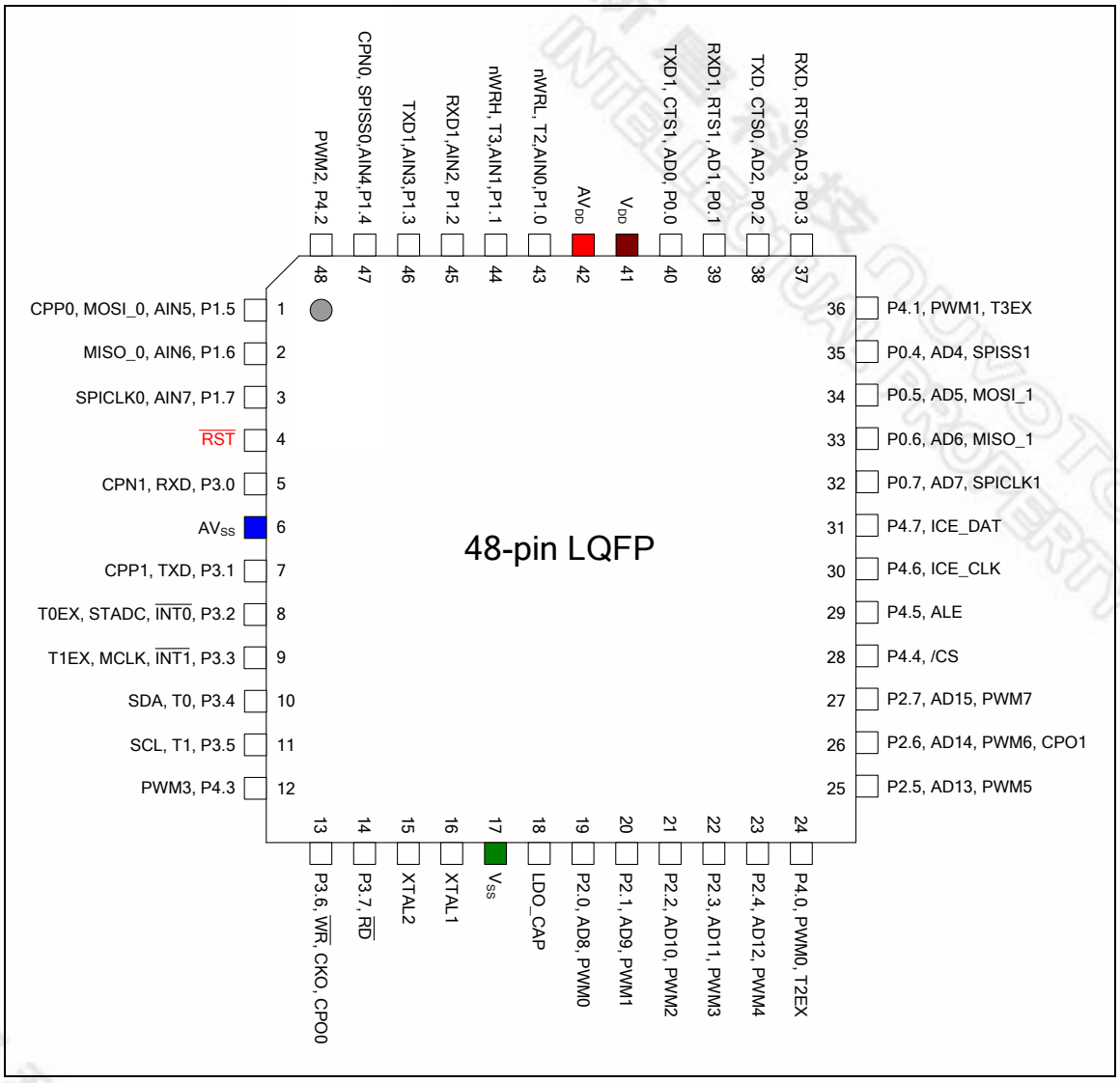

Figure 5-2 NuMicro™ M051 Series LQFP-48 Pin Diagram

5.3 Pin Description

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
11	16	XTAL1				I (ST)	**CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
10	15	XTAL2				O	**CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
27	41	V_{DD}				P	**POWER SUPPLY:** Power supply to I/O ports and LDO source for internal PLL and digital circuit.
12 33	17	V_{SS}				P	**GROUND: Digital** Ground potential.
28	42	AV_{DD}				P	**POWER SUPPLY:** Power supply to internal analog circuit.
4	6	AV_{SS}				P	**GROUND: Analog** Ground potential.
13	18	LDO_CAP				P	**LDO:** LDO output pin **Note: It needs to be connected with a 1uF capacitor.**
2	4	$\overline{RST}$				I (ST)	**RESET:** /RST pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	40	P0.0	CTS1	AD0	TXD1[2]	D, I/O	**PORT0:** Port 0 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, and SPICLK1. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte
25	39	P0.1	RTS1	AD1	RXD1[2]	D, I/O	
NC	38	P0.2	CTS0	AD2	TXD[2]	D, I/O	

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
NC	37	P0.3	RTS0	AD3	RXD[2]	D, I/O	address for external devices. These pins which are SPISS1, MOSI_1, MISO_1, and SPICLK1 for the SPI function used. CTS0/1: Clear to Send input pin for UART0/1 RTS0/1: Request to Send output pin for UART0/1 The RXD/TXD pins are for UART0 function used. The RXD1/TXD1 pins are for UART1 function used.
24	35	P0.4	SPISS1	AD4		D, I/O	
23	34	P0.5	MOSI_1	AD5		D, I/O	
22	33	P0.6	MISO_1	AD6		D, I/O	
21	32	P0.7	SPICLK1	AD7		D, I/O	
29	43	P1.0	T2	AIN0	$\overline{WRL}$	I/O	**PORT1:** Port 1 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, and SPICLK0. These pins which are SPISS0, MOSI_0, MISO_0, and SCLK0 for the SPI function used. These pins which are AIN0~AIN7for the 12 bits ADC function used. The RXD1/TXD1 pins are for UART1 function used. The $\overline{WRL}$ / $\overline{WRH}$ pins are for low/high byte write enable output in 16-bit data width of EBI. The CPN0/CPP0 pins are for Comparator0 negative/positive inputs. The T2/T3 pins are for Timer2/3 external even counter input.
NC	44	P1.1	T3	AIN1	$\overline{WRH}$	I/O	
30	45	P1.2	RXD1[3]	AIN2		I/O	
31	46	P1.3	TXD1[3]	AIN3		I/O	
32	47	P1.4	SPISS0	AIN4	CPN0	I/O	
1	1	P1.5	MOSI_0	AIN5	CPP0	I/O	
NC	2	P1.6	MISO_0	AIN6		I/O	
NC	3	P1.7	SPICLK0	AIN7		I/O	
NC	19	P2.0	PWM0[2]	AD8		D, I/O	**PORT2:** Port 2 is an 8-bit four mode output pin and two mode input. It has an alternative function P2 has an alternative function as AD[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices. These pins which are PWM0~PWM7 for the PWM function used in the LQFP48 package.
NC	20	P2.1	PWM1[2]	AD9		D, I/O	
14	21	P2.2	PWM2[2]	AD10		D, I/O	
15	22	P2.3	PWM3[2]	AD11		D, I/O	

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
16	23	P2.4	PWM4[2]	AD12		D, I/O	The CPO1 pin is the output of Comparator1.
17	25	P2.5	PWM5[2]	AD13		D, I/O	
18	26	P2.6	PWM6[2]	AD14	CPO1	D, I/O	
NC	27	P2.7	PWM7[2]	AD15		D, I/O	
3	5	P3.0	RXD[2]		CPN1	I/O	**PORT3:** Port 3 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for RXD, TXD, $\overline{INT0}$, $\overline{INT1}$, T0, T1, $\overline{WR}$, and $\overline{RD}$. The RXD/TXD pins are for UART0 function used. The SDA/SCK pins are for I^2C function used. MCLK: EBI clock output pin. CKO: HCLK clock output The STADC pin is for ADC external trigger input. The CPN1/CPP1 pins are for Comparator1 negative/positive inputs. The CPO0 pin is the output of Comparator0. The T0/T1 pins are for Timer0/1 external even counter input. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1.
5	7	P3.1	TXD[2]		CPP1	I/O	
6	8	P3.2	$\overline{INT0}$	STADC	T0EX	I/O	
NC	9	P3.3	$\overline{INT1}$	MCLK	T1EX	I/O	
7	10	P3.4	T0	SDA		I/O	
8	11	P3.5	T1	SCL		I/O	
9	13	P3.6	$\overline{WR}$	CKO	CPO0	I/O	
NC	14	P3.7	$\overline{RD}$			I/O	
NC	24	P4.0	PWM0[2]		T2EX	I/O	**PORT4:** Port 4 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for /CS, ALE, ICE_CLK and ICE_DAT. $\overline{CS}$ for EBI (External Bus Interface) used. ALE (Address Latch Enable) is used to enable the address latch that separates the address from the data on Port 0 and Port 2.
NC	36	P4.1	PWM1[2]		T3EX	I/O	
NC	48	P4.2	PWM2[2]			I/O	
NC	12	P4.3	PWM3[2]			I/O	

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
NC	28	P4.4	$\overline{CS}$			I/O	The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used. PWM0-3 can be used from P4.0-P4.3 when EBI is active. The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3.
NC	29	P4.5	ALE			I/O	
19	30	P4.6	ICE_CLK			I/O	
20	31	P4.7	ICE_DAT			I/O	

Table 5-1 NuMicro™ M051 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

[2] The pins features which are set by S/W. Only one-set pin can be used while S/W to set it.

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

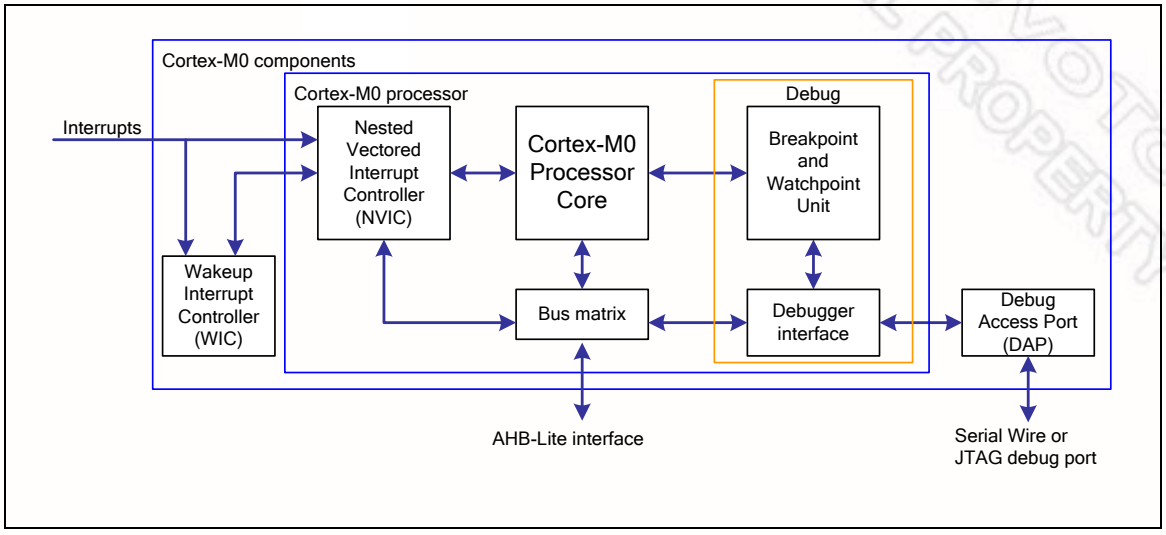

Figure 6-1 Functional Block Diagram

The implemented device provides:

A low gate count processor the features:

- The ARMv6-M Thumb® instruction set.
- Thumb-2 technology.
- ARMv6-M compliant 24-bit SysTick timer.
- A 32-bit hardware multiplier.
- The system interface supports little-endian data accesses.
- The ability to have deterministic, fixed-latency, interrupt handling.

- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
- C Application Binary Interface compliant exception model.
  This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

NVIC features:

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

Debug support:

- Four hardware breakpoints.
- Two watchpoints.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

Bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2 System Manager

6.2.1 Overview

The following functions are included in system manager section

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip module reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset (POR)
- The low level on the /RESET pin
- Watchdog Time Out Reset (WDT)
- Low Voltage Reset (LVR)
- Brown-Out Detected Reset (BOD)
- CPU Reset
- Software one shot Reset

6.2.3 System Power Architecture

In this device, the power architecture is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog module operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.

The outputs of internal voltage regulator, which is LDO, require an external capacitor which should be located close to the corresponding pin. The Figure 6-2 shows the power architecture of this device.

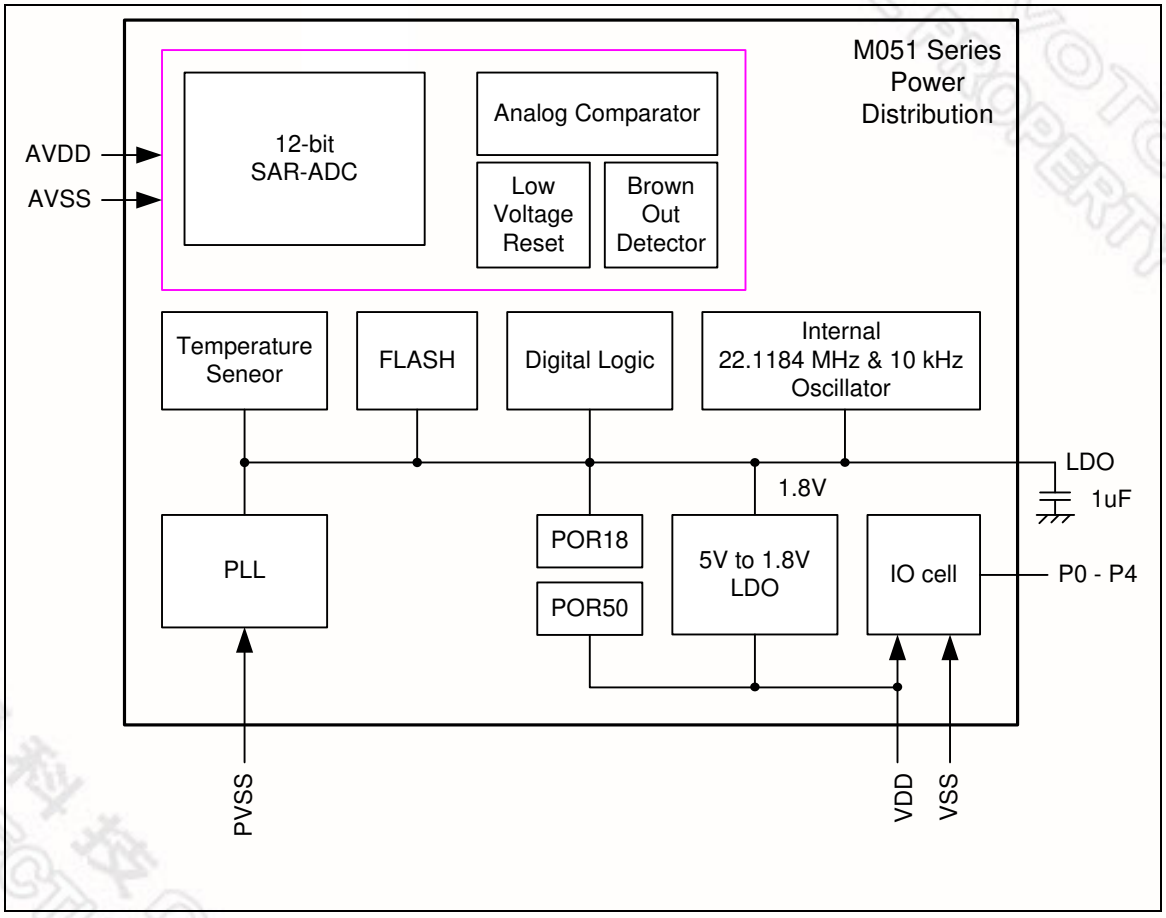

Figure 6-2 NuMicro M051™ Series Power Architecture Diagram

6.2.4 Whole System Memory Map

NuMicro M051™ series provides a 4G-byte address space. The memory locations assigned to each on-chip modules are shown in Table 6-1. The detailed register memory addressing and programming will be described in the following sections for1 individual on-chip peripherals. NuMicro M051™ series only supports little-endian data format.

Address Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4KB)
EBI Space (0x6000_0000 ~ 0x6001_FFFF)		
0x6000_0000 – 0x6001_FFFF	EBI_BA	External Memory Space (128KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO (P0~P4) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_CTL_BA	EBI Control Registers (128KB)
APB Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watch-Dog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers