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ARM CORTEX[®]-M 32-BIT MICROCONTROLLER

NuMicro[®] Family M0564 Series Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® M0564 series microcontroller based on the ARM® Cortex®-M0 core operates at up to 72 MHz. It features adjustable V_{DDIO} pins for specific I/O pins with a wide range of voltage from 1.8V to 5.5V for various operating voltages of external components, a unique high-speed PWM with clock frequency up to 144 MHz for precision control, and an integrated hardware divider to speed up the calculation for the control algorithms. Apart from that, the M0564 also integrates SPROM (Security Protection ROM) which provides a secure code execution area to protect the intelligent property of developers. The M0564 series is ideal for industrial control, motor control and metering applications.

The M0564 series supports the wide voltage range from 2.5V to 5.5V and temperature ranging from -40°C to 105°C, up to 256 Kbytes of Flash memory, 20 Kbytes of SRAM, 4 Kbytes of ISP (In-System Programming) ROM as well as ICP (In-Circuit Programming) ROM and IAP (In-Application Programming) ROM in 48-, 64- or 100-pin packages. It also supports high immunity of 8KV ESD (HBM)/4KV EFT. It is also equipped with plenty of peripherals such as Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card Interface, SPI, I²S, I²C, GPIO, up to 12 channels of 16-bit PWM, up to 20 channels of 12-bit ADC, analog comparator, temperature sensor, LVR (Low Voltage Reset), BOD (Brown-out Detector), 96-bit UID (Unique Identification), and 128-bit UCID (Unique Customer Identification).

1.1 Key Features Support Table

Product Line	USB	USCI	UART	I ² C	SPI/I ² S	ISO 7816	PWM	EBI	PDMA	ADC	ACMP	RTC V _{BAT}	1.8V IO
M0564	-	3	3	2	2	2	12	Y	5	20	2	Y	Y

Table 1.1-1 Key Features Support Table

The NuMicro[®] M0564 series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- Smart Card Reader
- Printer
- Bar Code Scanner
- Motor Control
- Digital Power

2 FEATURES

2.1 NuMicro® M0564 Features

- Core
 - ARM® Cortex®-M0 core running up to 72 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Supports programmable mask-able interrupts
 - Serial Wire Debug supports with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
 - Supports 256/128 KB application ROM (APROM)
 - Supports 4 KB Flash for loader (LDROM)
 - Supports 2 KB Security Protection Rom (SPROM)
 - Supports 12 bytes User Configuration block to control system initiation
 - Supports Data Flash with configurable memory size
 - Supports 2 KB page erase for all embedded flash
 - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
 - Supports CRC-32 checksum calculation function
 - Supports flash all one verification function
 - Hardware external read protection of whole flash memory by Security Lock Bit
 - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
 - 20 KB embedded SRAM
 - Supports byte-, half-word- and word-access
 - Supports PDMA mode
- Hardware Divider
 - Signed (two's complement) integer calculation
 - 32-bit dividend with 16-bit divisor calculation capacity
 - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
 - Divided by zero warning flag
 - 6 HCLK clocks taken for one cycle calculation
 - Write divisor to trigger calculation
 - Waiting for calculation ready automatically when reading quotient and remainder
- PDMA (Peripheral DMA)
 - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
 - Supports single and burst transfer type
 - Supports Normal and Scatter-Gather Transfer modes
 - Supports two types of priorities modes: Fixed-priority and Round-robin modes
 - Supports byte-, half-word- and word-access
 - Supports incrementing mode for the source and destination address for each channel
 - Supports time-out function for channel 0 and channel 1
 - Supports software and SPI/I2S, UART, USCI, ADC, PWM and TIMER request
- Clock Control

- Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 48 MHz internal high speed RC oscillator (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
- Built-in 4~24 MHz high speed crystal oscillator for precise timing operation
- Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
- Supports PLL up to 144 MHz for high resolution PWM operation
- Supports dynamically calibrating the HIRC48 to 48 MHz $\pm 0.25\%$ by external 32.768K crystal oscillator (LXT)
- Supports dynamically calibrating the HIRC to 22.1184Mhz by external 32.768K crystal oscillator (LXT)
- Supports clock on-the-fly switch
- Supports clock failure detection for system clock
- Supports auto clock switch once clock failure detected
- Supports exception (NMI) generated once a clock failure detected
- Supports divided clock output
- GPIO
 - Four I/O modes
 - TTL/Schmitt trigger input selectable
 - I/O pin configured as interrupt source with edge/level trigger setting
 - Supports high driver and high sink current I/O (up to 20 mA at 5V)
 - Supports software selectable slew rate control
 - Supports up to 81/49/35 GPIOs for LQFP100/64/48 respectively
- Timer/PWM
 - Supports 4 sets of Timers/PWM

Timer Mode	PWM Mode
TM_CNT_OUT	PWM_CH0
TM_EXT	PWM_CH1 (Complementary)

- Timer Mode
 - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
 - Independent clock source for each timer
 - Provides one-shot, periodic, toggle and continuous counting operation modes
 - Supports event counting function to count the event from external pin
 - Supports input capture function to capture or reset counter value
 - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
 - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
 - Supports Inter-Timer trigger mode
- PWM Mode
 - Supports maximum clock frequency up to 50MHz
 - Supports independent mode for 4 sets of independent PWM output channel
 - Supports complementary mode for 4 sets of complementary paired PWM output channel with 12-bit Dead-time generator
 - Supports 12-bit pre-scalar from 1 to 4096

- Supports 16-bit resolution PWM counter, each timer provides 1 PWM counter
 - Supports up, down and up/down counter operation type
 - Supports one-shot or Auto-reload counter operation mode
 - Supports mask function and tri-state enable for each PWM pin
 - Supports brake function
 - Supports interrupt when PWM counter match zero, period value or compared value, and brake condition happened
 - Supports trigger ADC when PWM counter match zero, period value or compared value
- Watchdog Timer
 - Supports multiple clock sources from LIRC(default selection), HCLK/2048 and LXT
 - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
 - Able to wake up from Power-down or Idle mode
 - Interrupt or reset selectable on watchdog time-out
 - Window Watchdog Timer
 - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
 - Window set by 6-bit counter with 11-bit prescale
 - Interrupt or reset selectable on time-out
 - RTC
 - Supports separate battery power pin VBAT
 - Supports software compensation by setting frequency compensate register (FCR)
 - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Supports Alarm registers (second, minute, hour, day, month, year)
 - Supports Alarm mask registers
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Supports wake-up function
 - PWM
 - Supports maximum clock frequency up to 144MHz
 - Supports up to two PWM modules, each module provides 6 output channels.
 - Supports independent mode for PWM output/Capture input channel
 - Supports complementary mode for 2 complementary paired PWM output channel
 - Dead-time insertion with 12-bit resolution
 - Two compared values during one period
 - Supports 12-bit pre-scalar from 1 to 4096
 - Supports 16-bit resolution PWM counter
 - Up, down and up/down counter operation type
 - Supports mask function and tri-state enable for each PWM pin
 - Supports brake function
 - Brake source from pin and system safety events: clock failed, Brown-out detection and CPU lockup.
 - Noise filter for brake source from pin
 - Edge detect brake source to control brake state until brake interrupt cleared
 - Level detect brake source to auto recover function after brake condition removed
 - Supports interrupt on the following events:
 - PWM counter match zero, period value or compared value
 - Brake condition happened
 - Supports trigger ADC on the following events:

- PWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- USCI
 - Supports up to 3 sets of USCI

USCI	UART Mode	SPI Mode	I ² C Mode
USCI_CLK	-	SPI_CLK	SCL
USCI_CTL0	nCTS	SPI_SS	-
USCI_CTL1	nRTS	-	-
USCI_DAT0	Rx	SPI_MOSI	SDA
USCI_DAT1	Tx	SPI_MISO	-

- UART Mode
 - Supports one transmit buffer and two receive buffer for data payload
 - Supports hardware auto flow control function
 - Supports programmable baud-rate generator
 - Support 9-Bit Data Transfer (Support 9-Bit RS-485)
 - Baud rate detection possible by built-in capture event of baud rate generator
 - Supports Wake-up function (Data and nCTS Wakeup Only)
- SPI Mode
 - Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK / 2, Slave = fPCLK / 5)
 - Supports one transmit buffer and two receive buffers for data payload
 - Configurable bit length of a transfer word from 4 to 16-bit
 - Supports MSB first or LSB first transfer sequence
 - Supports Word Suspend function
 - Supports 3-wire, no slave select signal, bi-direction interface
 - Supports wake-up function by slave select signal in Slave mode
 - Supports one data channel half-duplex transfer
- I²C Mode
 - Full master and slave device capability
 - Supports of 7-bit addressing, as well as 10-bit addressing
 - Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
 - Supports multi-master bus
 - Supports one transmit buffer and two receive buffer for data payload
 - Supports 10-bit bus time-out capability
 - Supports bus monitor mode.
 - Supports Power down wake-up by data toggle or address match
 - Supports setup/hold time programmable
 - Supports multiple address recognition (two slave address with mask option)
- UART
 - Supports up to 3 sets of UART
 - Full-duplex asynchronous communications
 - Separates receive and transmit 16/16 bytes entry FIFO for data payloads
 - Supports hardware auto-flow control (RX, TX, CTS and RTS)
 - Programmable receiver buffer trigger level
 - Supports programmable baud rate generator for each channel individually
 - Supports 8-bit receiver buffer time-out detection function
 - Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])

- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
 - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
 - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
 - Supports LIN master/slave mode
 - Supports programmable break generation function for transmitter
 - Supports break detection function for receiver
- Supports RS-485 mode
 - Supports RS-485 9-bit mode
 - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports PDMA transferSmart Card Host (SC)
 - Supports up to two Smart Card Hosts

SC Mode	UART Mode
SC_DATA	Rx
SC_CLK	Tx
SC_CD	-
SC_PWR	-
SC_RST	-

- SC Mode
 - Supports up to two ISO-7816-3 ports
 - Compliant to ISO-7816-3 T=0, T=1
 - Separate receive / transmit 4 bytes entry FIFO for data payloads
 - Programmable transmission clock frequency
 - Programmable receiver buffer trigger level
 - Programmable guard time selection (11 ETU ~ 266 ETU)
 - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
 - Supports auto inverse convention function
 - Supports transmitter and receiver error retry and error limit function
 - Supports hardware activation sequence process
 - Supports hardware warm reset sequence process
 - Supports hardware deactivation sequence process
 - Supports hardware auto deactivation sequence when detecting the card is removal
- UART Mode
 - Full duplex, asynchronous communications
 - Supports receiving / transmitting 4-bytes FIFO
 - Supports programmable baud rate generator for each channel
 - Programmable even, odd or no parity bit generation and detection
 - Programmable stop bit, 1 or 2 stop bit generation
- SPI/I²S
 - Supports up to two SPI/I²S controllers

SPI Mode	I ² S Mode
SPI_CLK	I2S_BCLK
SPI_SS	I2S_LRCLK
SPI_MOSI	I2S_DO
SPI_MISO	I2S_DI
-	I2S_MCLK

- SPI Mode
 - Supports Master or Slave mode operation
 - Configurable bit length of a transfer word from 8 to 32-bit
 - Provides separate 4-/8-level depth transmit and receive FIFO buffers
 - Supports MSB first or LSB first transfer sequence
 - Supports Byte Reorder function
 - Supports PDMA transfer
- I²S Mode
 - Supports Master or Slave mode operation
 - Capable of handling 8-, 16-, 24- and 32-bit word sizes in I2S mode
 - Provides separate 4-level depth transmit and receive FIFO buffers in I2S mode
 - Supports monaural and stereo audio data in I2S mode
 - Supports PCM mode A, PCM mode B, I2S and MSB justified data format in I2S mode
 - Supports PDMA transfer

● I²C

- Supports up to two sets of I2C device
- Supports Master/Slave mode
- Supports bidirectional data transfer between masters and slaves
- Supports multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Supports 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allow versatile rate control
- Supports multiple address recognition, four slave address with mask option
- Supports two-level buffer function
- Supports setup/hold time programmable
- Supports wake-up function

● ADC

- Supports 12-bit SAR ADC
- 12-bit resolution and 10-bit accuracy is guaranteed
- Analog input voltage range: 0~ AV_{DD}
- Supports external VREF pin
- Up to 20 single-end analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Conversion rate up to 800K SPS at 5V
- Configurable ADC internal sampling time
- Supports single-scan, single-cycle-scan, and continuous scan and scan on enabled channels
- Supports individual conversion result register with valid and overrun indicators for each

- channel
 - Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
 - An A/D conversion can be triggered by:
 - Software enable
 - External pin (STADC)
 - Timer 0~3 overflow pulse trigger
 - PWM triggers with optional start delay period
 - Supports 4 internal channels for
 - Operational amplifier output
 - Band-gap VBG input
 - Temperature sensor input
 - VBAT voltage measure
 - Supports internal reference voltage: 2.048V, 2.560V, 3.072V and 4.096V
 - Supports PDMA transfer
- Analog Comparator
 - Supports up to 2 rail-to-rail analog comparators
 - Supports 4 multiplexed I/O pins at positive node.
 - Supports I/O pin and internal voltages at negative node
 - Support selectable internal voltage reference from:
 - Band-gap V_{BG}
 - Voltage divider source from AV_{DD} and internal reference voltage.
 - Supports programmable hysteresis
 - Supports programmable speed and power consumption
 - Interrupts generated when compare results change, interrupt event condition is programmable.
 - Supports power-down wake-up
 - Supports triggers for break events and cycle-by-cycle control for PWM
- Cyclic Redundancy Calculation Unit
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - Programmable initial value
 - Supports programmable order reverse setting for input data and CRC checksum
 - Supports programmable 1's complement setting for input data and CRC checksum.
 - Supports 8/16/32-bit of data width
 - Interrupt generated once checksum error occurs
- User Configurable VDD1=1.8~5.5V IO Interface
 - Supports UART0, SPI0 and I2C0
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1°C resolution
- Brown-out detector
 - With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
 - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage levels: 2.0 V
- Power consumption
 - Chip power down current < 10 uA with RAM data retention.
 - V_{BAT} power domain operating current <1.5 uA
- Operating Temperature: -40°C~105°C

● Packages

- All Green package (RoHS)
- LQFP 100-pin
- LQFP 64-pin(7mmx7mm)
- LQFP 48-pin

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

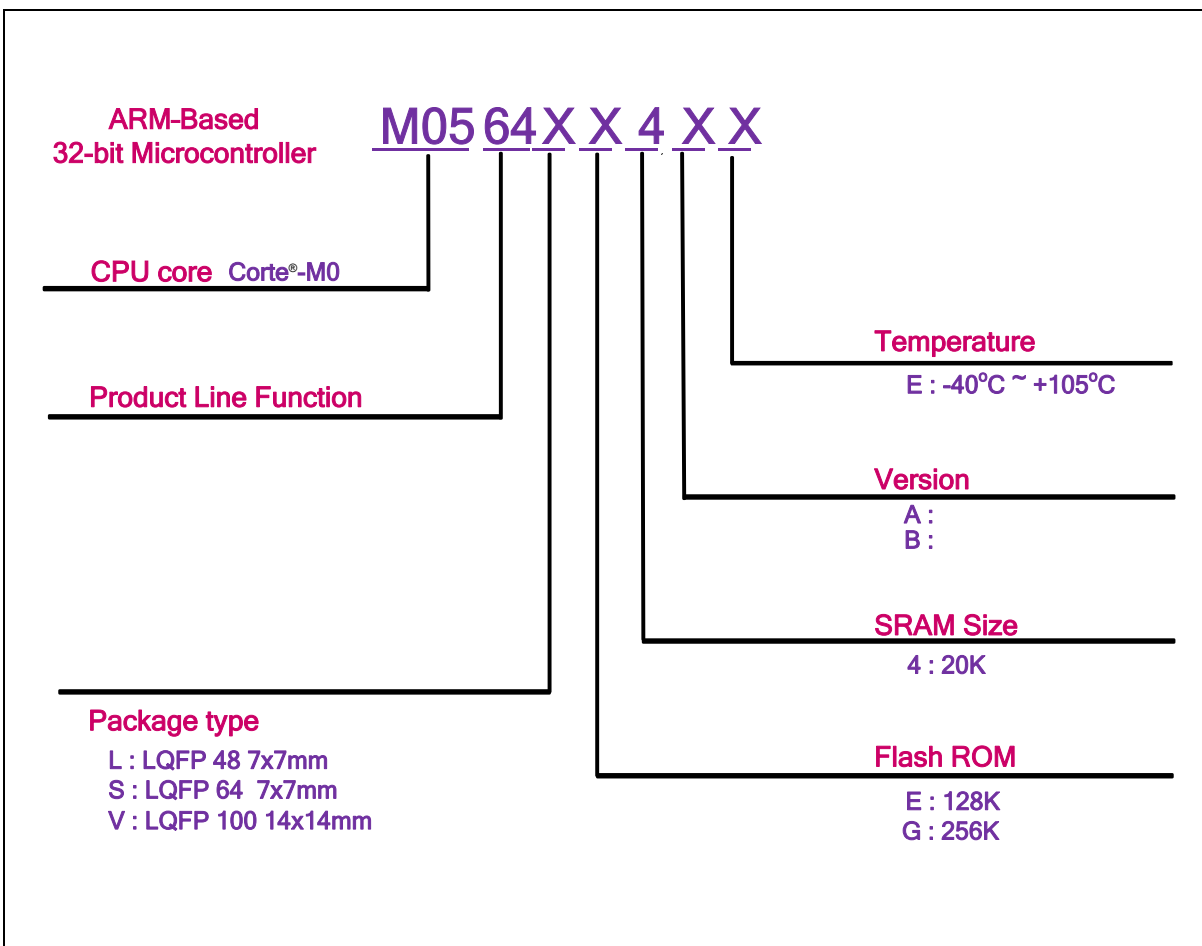
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® M0564 Selection Guide

4.1.1 NuMicro® M0564 Naming Rule



4.1.2 NuMicro® M0564 Base Series (M051 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM	Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	LVIO	EBI	ICP/IAP/ISP	Package
									USCI*	UART	SC/UART	SPI/I ² S	I ² C								
M0564LE4AE	128	20	Conf*	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564LG4AE	256	20	Conf*	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564SE4AE	128	20	Conf*	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564SG4AE	256	20	Conf*	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564VG4AE	256	20	Conf*	2	4	85	4	12	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP100

Conf*: Configurable

USCI*: support UART, SPI or I²C

LQFP64*: 7x7 mm

4.2 Pin Configuration

4.2.1 NuMicro® M0564 Base Series LQFP48 Pin Diagram

Corresponding Part Number: M0564LE4AE, M0564LG4AE

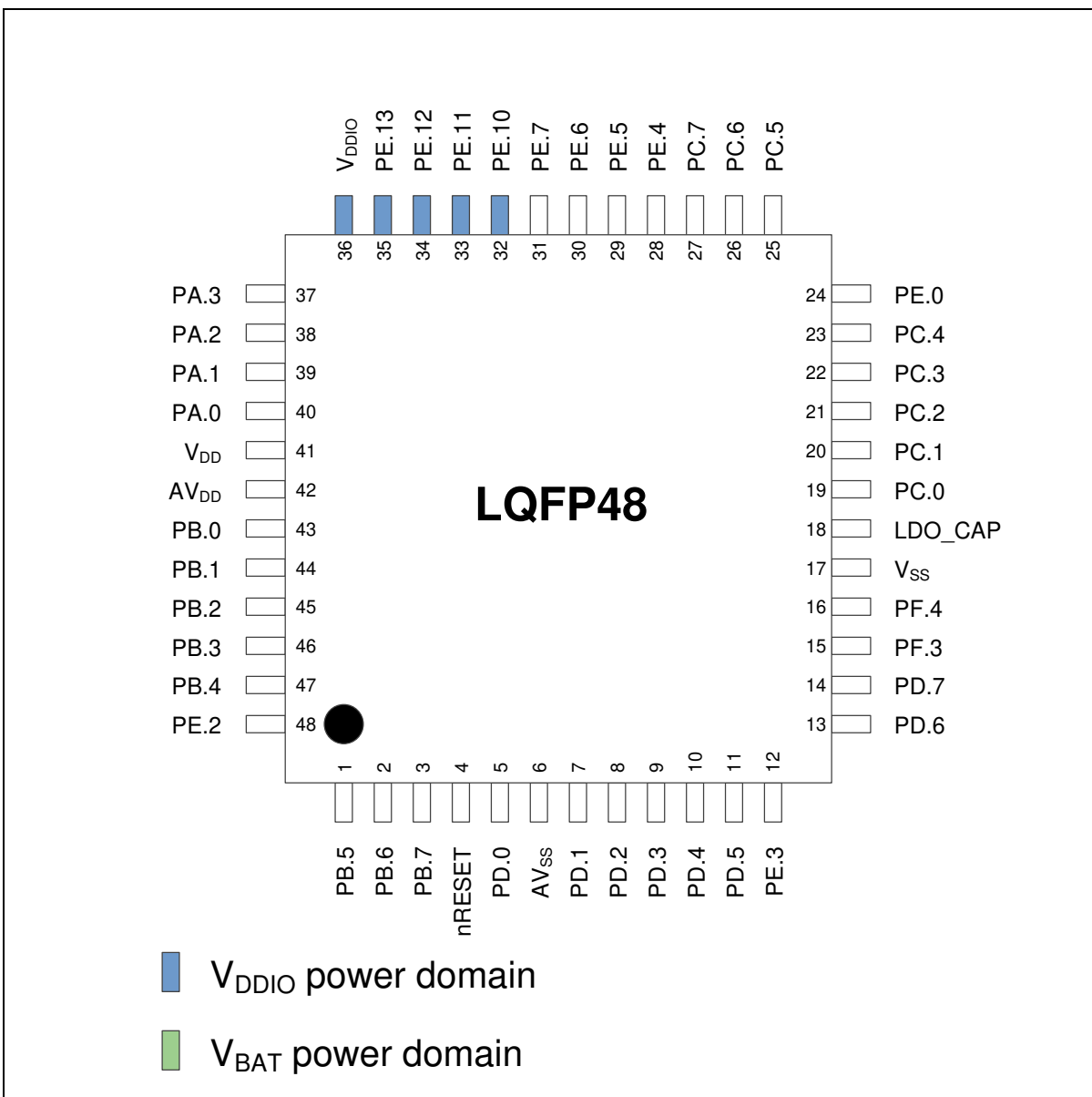


Figure 4.2-1 NuMicro® M0564 Base Series LQFP 48-pin Diagram

4.2.2 NuMicro® M0564 Base Series LQFP64 Pin Diagram

Corresponding Part Number: M0564SE4AE, M0564SG4AE

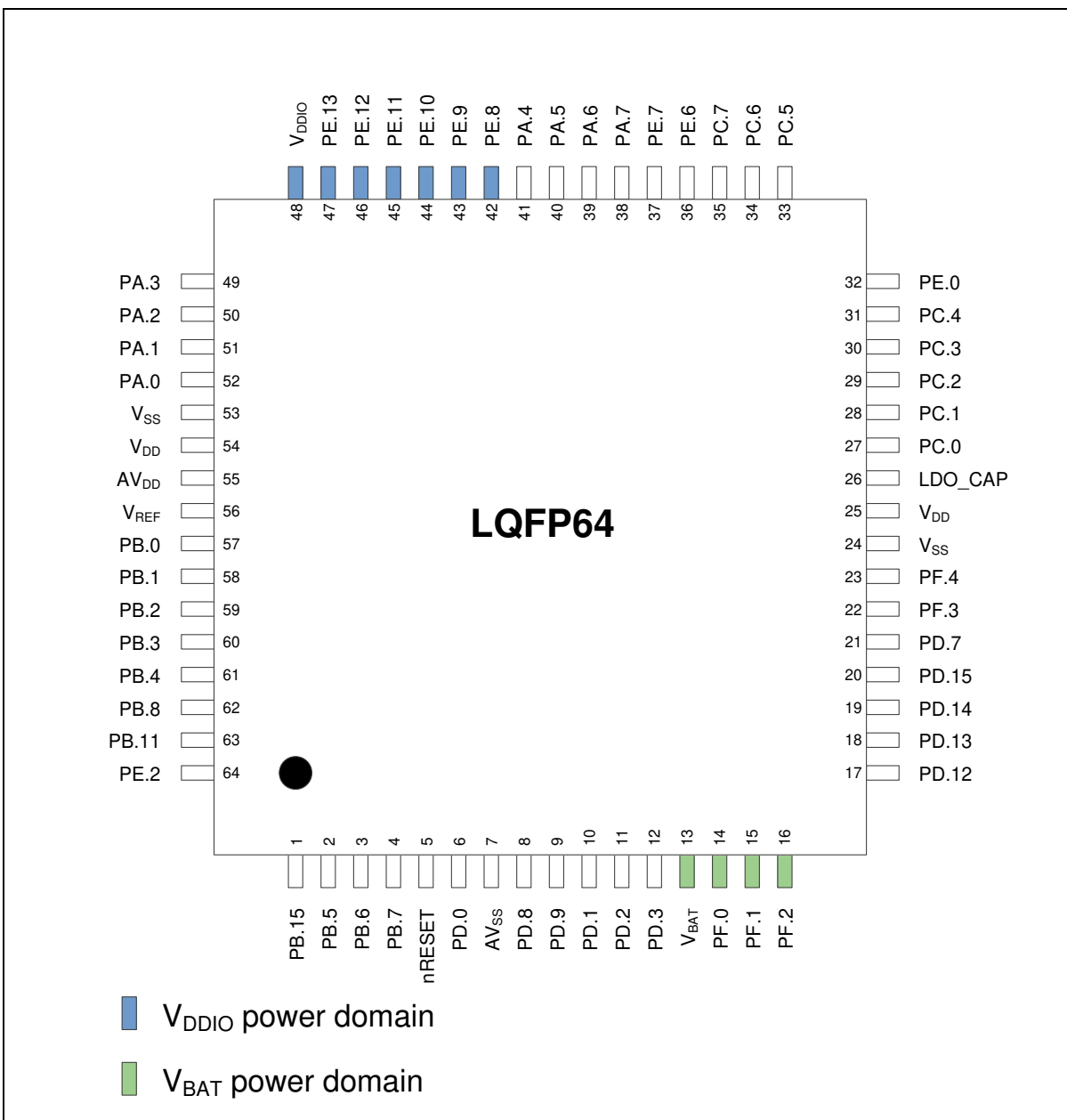


Figure 4.2-2 NuMicro® M0564 Base Series LQFP 64-pin Diagram

4.2.3 NuMicro® M0564 Base Series LQFP100 Pin Diagram

Corresponding Part Number: M0564VG4AE

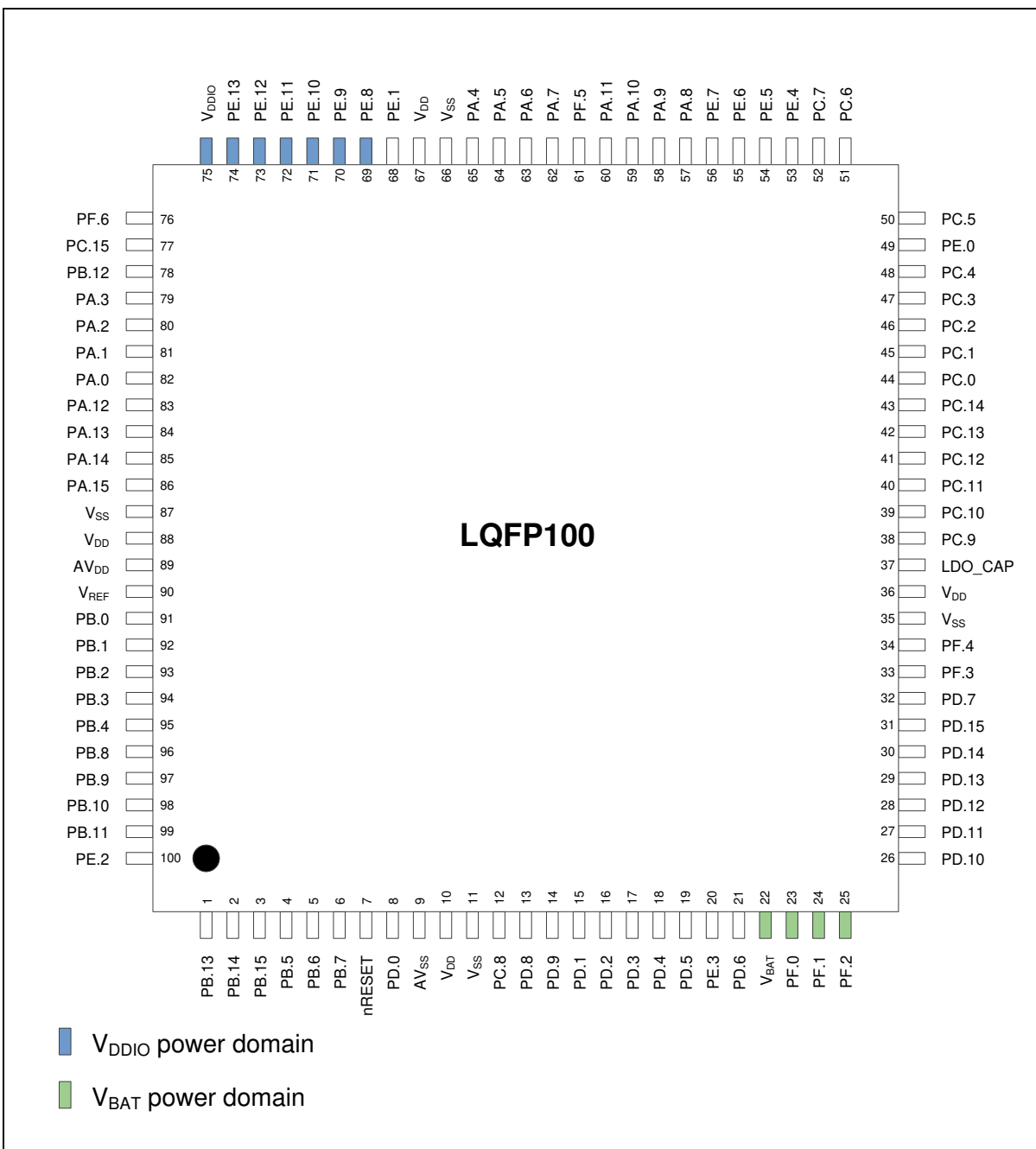


Figure 4.2-3 NuMicro® M0564 Base Series LQFP 100-pin Diagram