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nuvoTon

ARM Cortex®-M0
32-bit Microcontroller

NuMicro™ M058S Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro™ M058S is a 32-bit microcontroller with embedded ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The Cortex®-M0 is ARM embedded processor with 32-bit performance and cost-effective microcontroller.

The NuMicro™ M058S can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro™ M058S has 32 KB flash, 4 KB data flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and Brown-Out Detector, have been incorporated into the NuMicro™ M058S in order to reduce component count, board space and system cost. These useful functions make the NuMicro™ M058S powerful for a wide range of applications.

Additionally, the NuMicro™ M058S is equipped with IAP (In-Application Programming), ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 32 KB Flash for program memory (APROM)
  - 4 KB Flash for data memory (DataFlash)
  - 4 KB Flash for loader (LDROM)
  - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 22.1184 MHz internal oscillator
  - 4~24 MHz external crystal input
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
  - PLL allows CPU operation up to the maximum 50 MHz
- I/O Port
  - Up to 55 general-purpose I/O (GPIO) pins for LQFP-64 package
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Configurable I/O mode after POR
- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function.
  - Additional functions:
    - Two more timer clock sources from external trigger and internal 10 kHz
    - TIMER wake-up function
    - External capture input source selected from TxEX
    - Toggle mode output pins selected from TxEX or TMx
    - Inter-Timer trigger mode
- WDT (Watchdog Timer)

- Multiple clock sources
- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected

- WWDT (Window Watchdog Timer)
  - 6-bit down counter with 11-bit prescale for wide range window selected
- PWM
  - Up to two built-in 16-bit PWM generators, providing four PWM outputs or two complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
  - Additional functions
    - Internal 10 kHz to PWM clock source
    - Polar inverse function
    - Center-aligned type function
    - Timer duty interrupt enable function
    - Two kinds of PWM interrupt period/duty type selection
    - Period/duty trigger ADC function
- UART
  - Programmable baud-rate generator
  - Buffered receiver and transmitter, each with 16 bytes FIFO
  - Optional flow control function (CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS485 function
  - Supports LIN function
- SPI
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Provides 3 wire function
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Supports Byte Suspend mode in 32-bit transmission
  - Additional functions
    - PLL clock source
    - 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode
- I^2C
  - Up to two sets of I2C device
  - Supports master/slave mode
  - Bidirectional data transfer between master and slave
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via

one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
  - Supports 2' complement/un-signed format in differential mode conversion results
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion started either by software trigger or external pin trigger
  - Additional functions
    - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
    - PWM trigger delay function
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1℃ resolution
- BOD (Brown-out Detector)
  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-Out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - 64-pin LQFP, 48-pin LQFP, 33-pin QFN, 20-pin TSSOP

3 ABBREVIATIONS

3.1 List of Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ M058S Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			PWM (16-bit)	ADC (12-bit)	WDT	WWDT	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I²C							
M058SFAN	32	4	4	4	14	4	1	1	1	1	2	√	√	√	TSSOP20	-40 to +85
M058SZAN	32	4	4	4	26	4	1	1	1	2	5	√	√	√	QFN33	-40 to +85
M058SLAN	32	4	4	4	42	4	1	1	2	4	8	√	√	√	LQFP48	-40 to +85
M058SSAN	32	4	4	4	55	4	1	1	2	4	8	√	√	√	LQFP64	-40 to +85

Table 4.1-1 NuMicro™ M058S Series Selection Guide

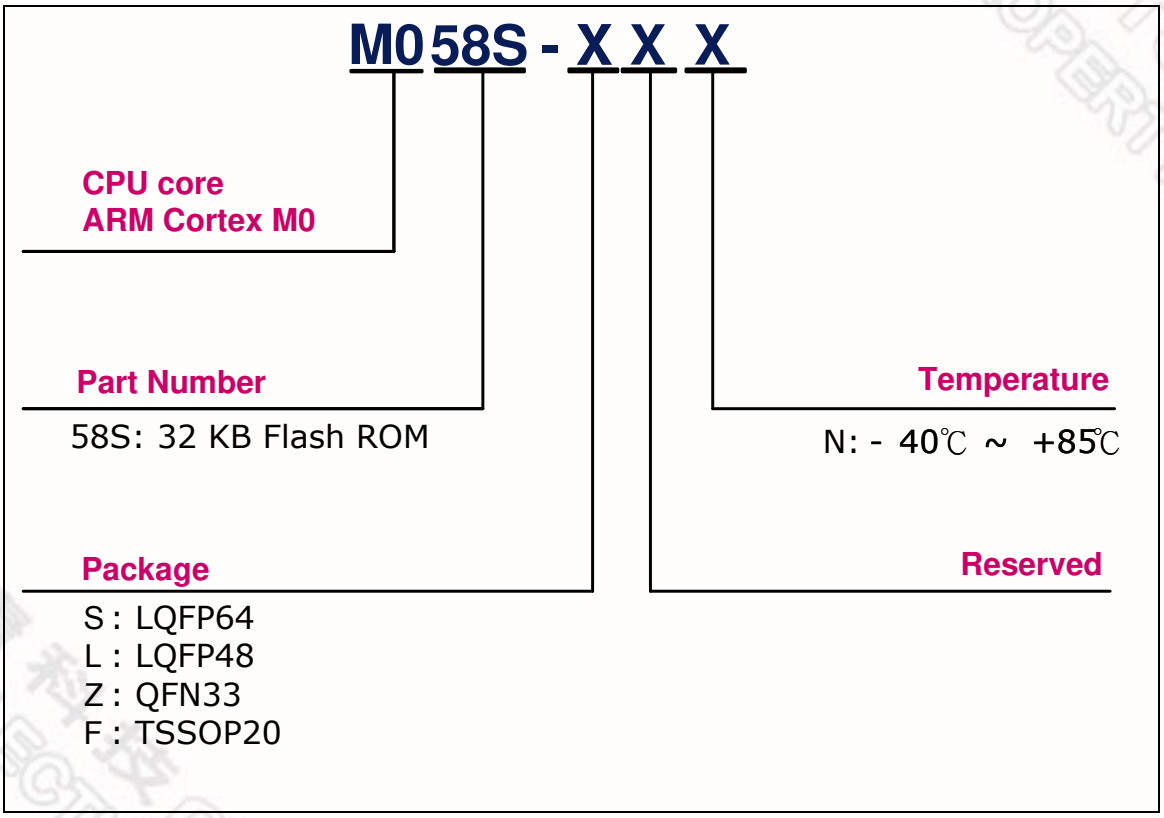

Figure 4.1-1 NuMicro™ M058S Series Selection Code

4.2 Pin Configuration

4.2.1 TSSOP20 pin

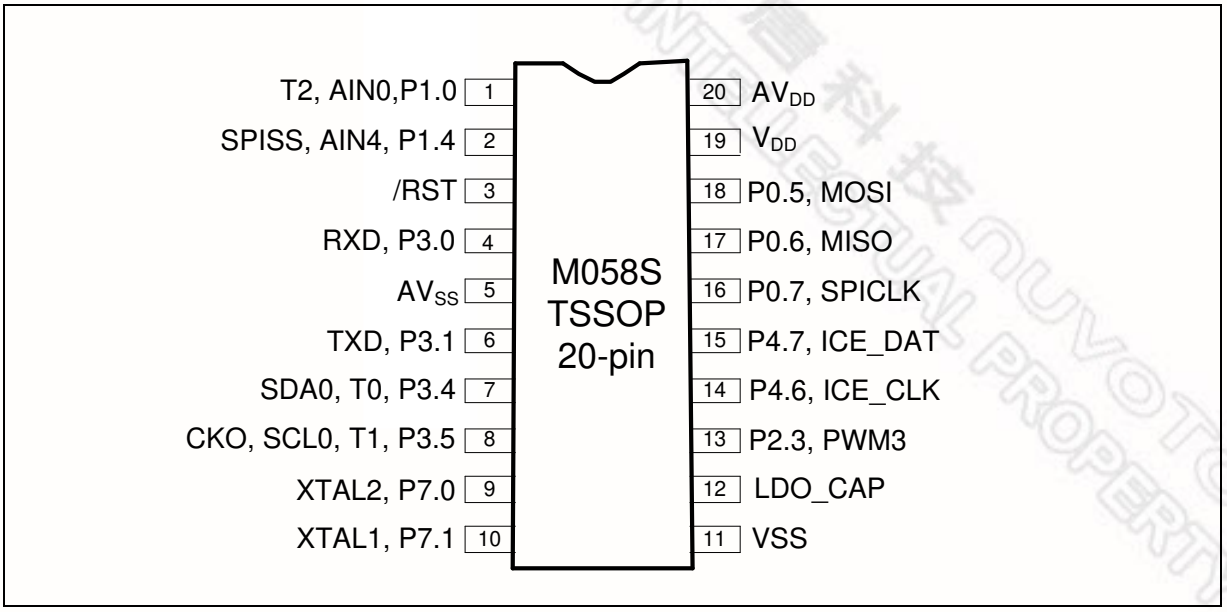

Figure 4.2-1 NuMicro™ M058S TSSOP20 Pin Diagram

4.2.2 QFN 33-pin

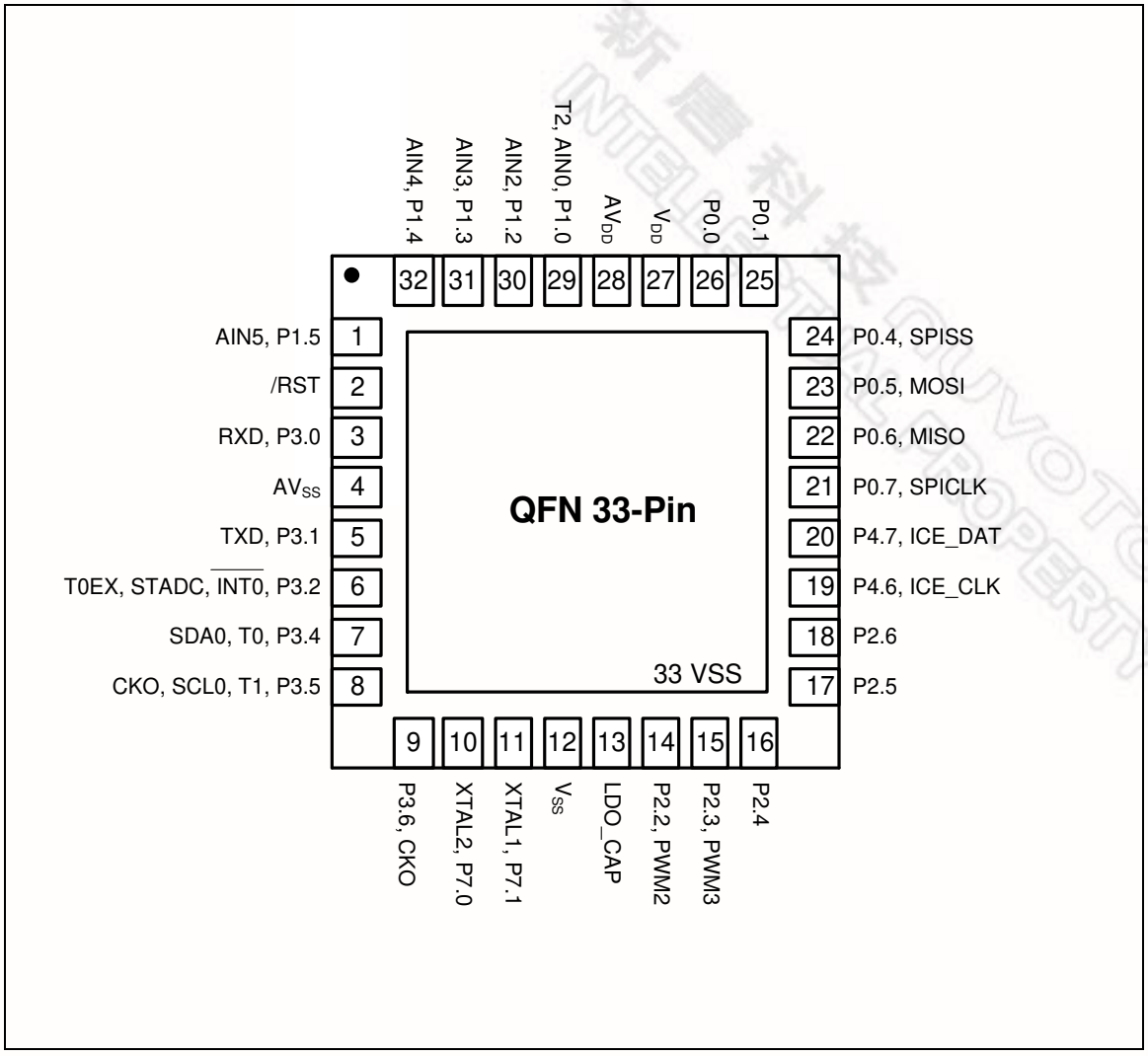

Figure 4.2-2 NuMicro™ M058S Series QFN-33 Pin Diagram

4.2.3 LQFP 48-pin

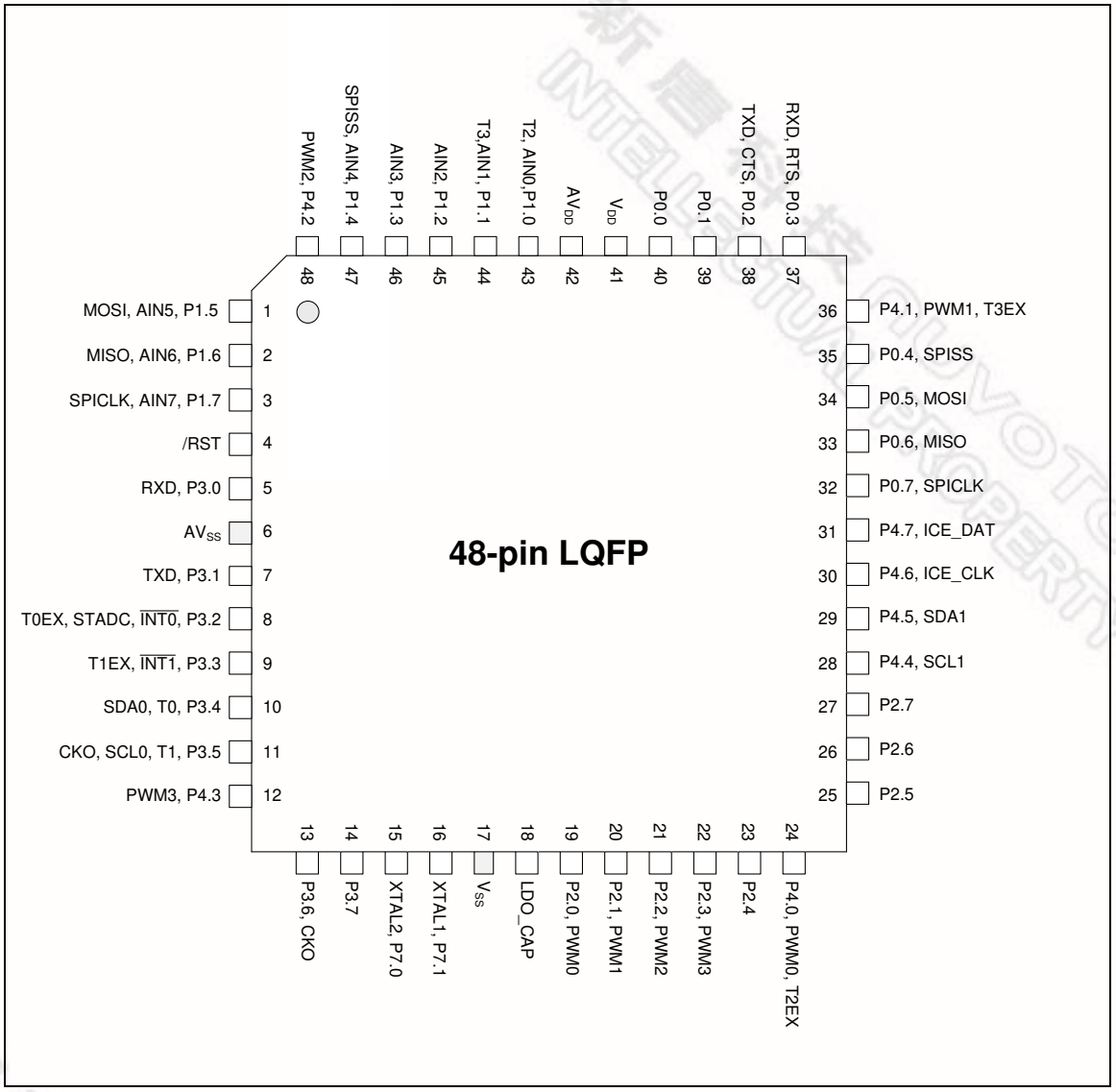

Figure 4.2-3 NuMicro™ M058S Series LQFP-48 Pin Diagram

4.2.4 LQFP 64-pin

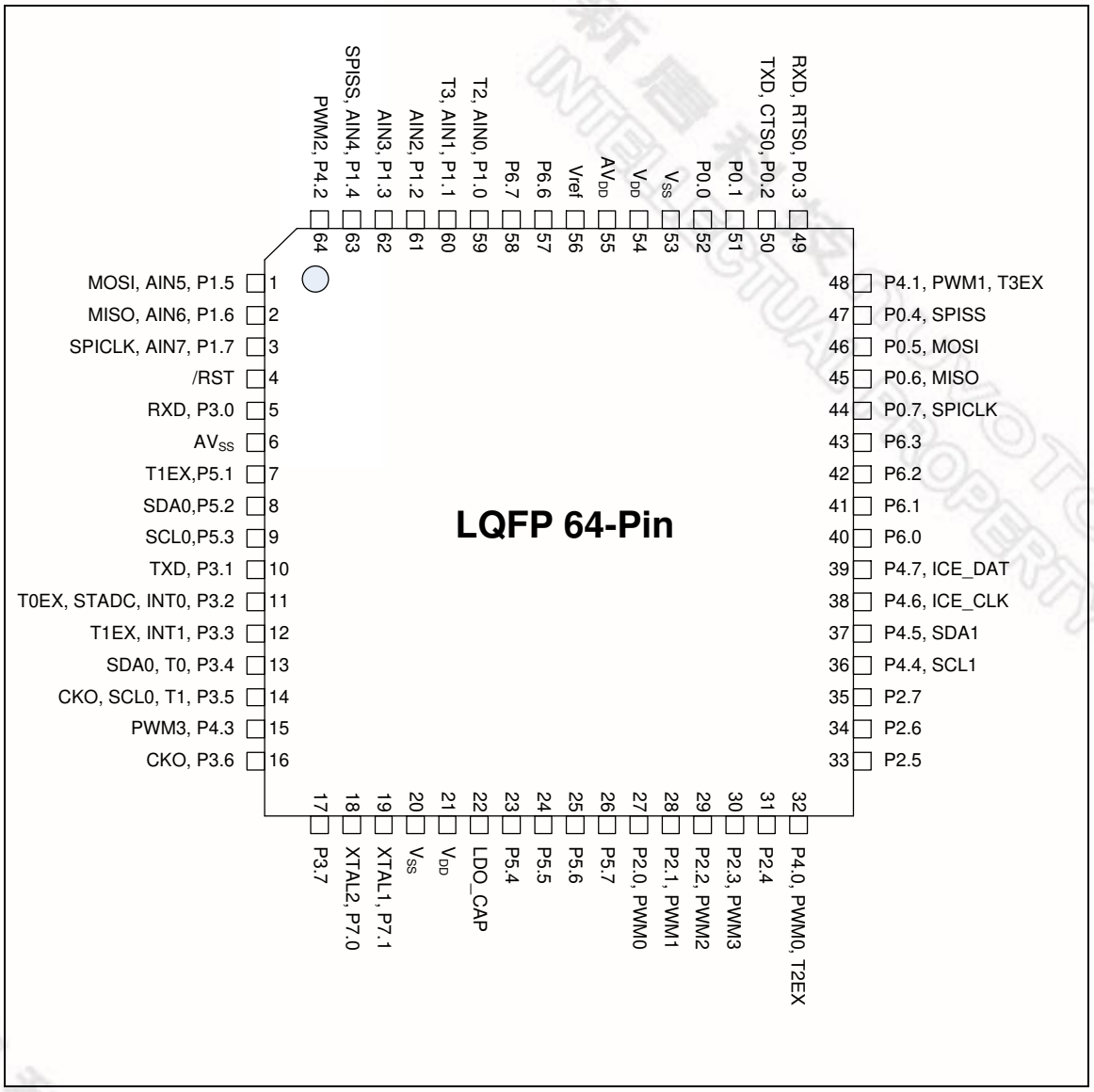

Figure 4.2-4 NuMicro™ M058S Series LQFP-64 Pin Diagram

4.3 Pin Description

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
19	27	41	21 54	V_{DD}				P	Power supply to I/O ports and LDO source for internal PLL and digital circuit.
11	12 33	17	20 53	V_{SS}				P	Ground pin for digital circuit.
20	28	42	55	AV_{DD}				P	Power supply to internal analog circuit.
5	4	6	6	AV_{SS}				P	Analog Ground pin for analog circuit.
	NC	NC	56	V_{ref}				P	Voltage reference input for ADC
12	13	18	22	LDO _CAP				P	LDO output pin **Note:** This pin needs to be connected with a 1uF capacitor.
3	2	4	4	/RST				I (ST)	/RST pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
	26	40	52	P0.0				I/O	**PORT0:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS, MOSI, MISO, and SPICLK. The pins SPISS, MOSI, MISO, and SPICLK are for the SPI function use. CTS: Clear to Send input pin
	25	39	51	P0.1				I/O	
	NC	38	50	P0.2	CTS		TXD[2]	I/O	
	NC	37	49	P0.3	RTS		RXD[2]	I/O	
	24	35	47	P0.4	SPISS[2]			I/O	
18	23	34	46	P0.5	MOSI[2]			I/O	

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
17	22	33	45	P0.6	MISO[2]			I/O	for UART RTS: Request to Send output pin for UART The RXD/TXD pins are for UART function use.
16	21	32	44	P0.7	SPICLK[2]			I/O	
1	29	43	59	P1.0	T2	AIN0		I/O	**PORT1:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T2, T3, SPISS0, MOSI, MISO, and SPICLK. The pins SPISS0, MOSI, MISO, and SCLK are for the SPI function use. The pins AIN0~AIN7 are for the 12 bits ADC function use. The T2/T3 pins are for Timer2/3 external event counter input.
	NC	44	60	P1.1	T3	AIN1		I/O	
	30	45	61	P1.2		AIN2		I/O	
	31	46	62	P1.3		AIN3		I/O	
2	32	47	63	P1.4	SPISS[2]	AIN4		I/O	
	1	1	1	P1.5	MOSI[2]	AIN5		I/O	
	NC	2	2	P1.6	MISO[2]	AIN6		I/O	
	NC	3	3	P1.7	SPICLK[2]	AIN7		I/O	
	NC	19	27	P2.0	PWM0[2]			I/O	**PORT2:** General purpose I/O port, which can be configured by software in four modes. It has an alternative function. The pins PWM0~PWM3 are for the PWM function use.
	NC	20	28	P2.1	PWM1[2]			I/O	
	14	21	29	P2.2	PWM2[2]			I/O	
13	15	22	30	P2.3	PWM3[2]			I/O	
	16	23	31	P2.4				I/O	
	17	25	33	P2.5				I/O	
	18	26	34	P2.6				I/O	
	NC	27	35	P2.7				I/O	
4	3	5	5	P3.0	RXD[2]			I/O	**PORT3:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for RXD, TXD, /INT0, /INT1, T0 and T1. The RXD/TXD pins are for
6	5	7	10	P3.1	TXD[2]			I/O	
	6	8	11	P3.2	/INT0	STADC	T0EX	I/O	
	NC	9	12	P3.3	/INT1		T1EX	I/O	

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
7	7	10	13	P3.4	T0	SDA0		I/O	UART function use. The SDA0/SCL0 pins are for I²C0 function use. CKO: HCLK clock output The STADC pin is for ADC external trigger input. The T0/T1 pins are for Timer0/1 external event counter input. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1.
8	8	11	14	P3.5	T1	SCL0	CKO[2]	I/O	
	9	13	16	P3.6		CKO		I/O	
	NC	14	17	P3.7				I/O	
	NC	24	32	P4.0	PWM0[2]		T2EX	I/O	**PORT4:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for PWM0-3, SCL1, SDA1, ICE_CLK and ICE_DAT. The ICE_CLK/ICE_DAT pins are for JTAG-ICE function use. PWM0-3 can be used from P2.0-P2.3 or P4.0-P4.3. The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3.
	NC	36	48	P4.1	PWM1[2]		T3EX	I/O	
	NC	48	64	P4.2	PWM2[2]			I/O	
	NC	12	15	P4.3	PWM3[2]			I/O	
	NC	28	36	P4.4		SCL1		I/O	
	NC	29	37	P4.5		SDA1		I/O	
14	19	30	38	P4.6	ICE_CLK			I/O	
15	20	31	39	P4.7	ICE_DAT			I/O	
	NC	NC	7	P5.1	T1EX			I/O	**PORT5:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T0EX, T1EX, SDA0 and SCL0. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1. The SDA0/SCL0 pins are for I²C0 function use.
	NC	NC	8	P5.2	SDA0			I/O	
	NC	NC	9	P5.3	SCL0			I/O	
	NC	NC	23	P5.4				I/O	
	NC	NC	24	P5.5				I/O	
	NC	NC	25	P5.6				I/O	
	NC	NC	26	P5.7				I/O	
	NC	NC	40	P6.0				I/O	**PORT6:** General purpose I/O

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
	NC	NC	41	P6.1				I/O	port, which can be configured by software in four modes.
	NC	NC	42	P6.2				I/O	
	NC	NC	43	P6.3				I/O	
	NC	NC	57	P6.6				I/O	
	NC	NC	58	P6.7				I/O	
9	10	15	18	P7.0	XTAL2			I/O, O	PORT7: General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for XTAL
10	11	16	19	P7.1	XTAL1			I/O, I(ST)	XTAL: External 4~24 MHz (high speed) crystal pin.

Note 1: I/O type description. I: Input, O: Output, I/O: Quasi-bidirectional, D: Open-drain, P: Power pins, ST: Schmitt trigger.

Note 2: The PWM0 ~ PWM3, RXD, TXD, RXD1, TXD1, SCL1, SDA1 and CKO can be assigned to different pins. However, a pin function can only be assigned to a pin at the same time, i.e. software cannot assign RXD to P0.3 and P3.0 at the same time.

5 BLOCK DIAGRAM

5.1 NuMicro™ M058S Block Diagram

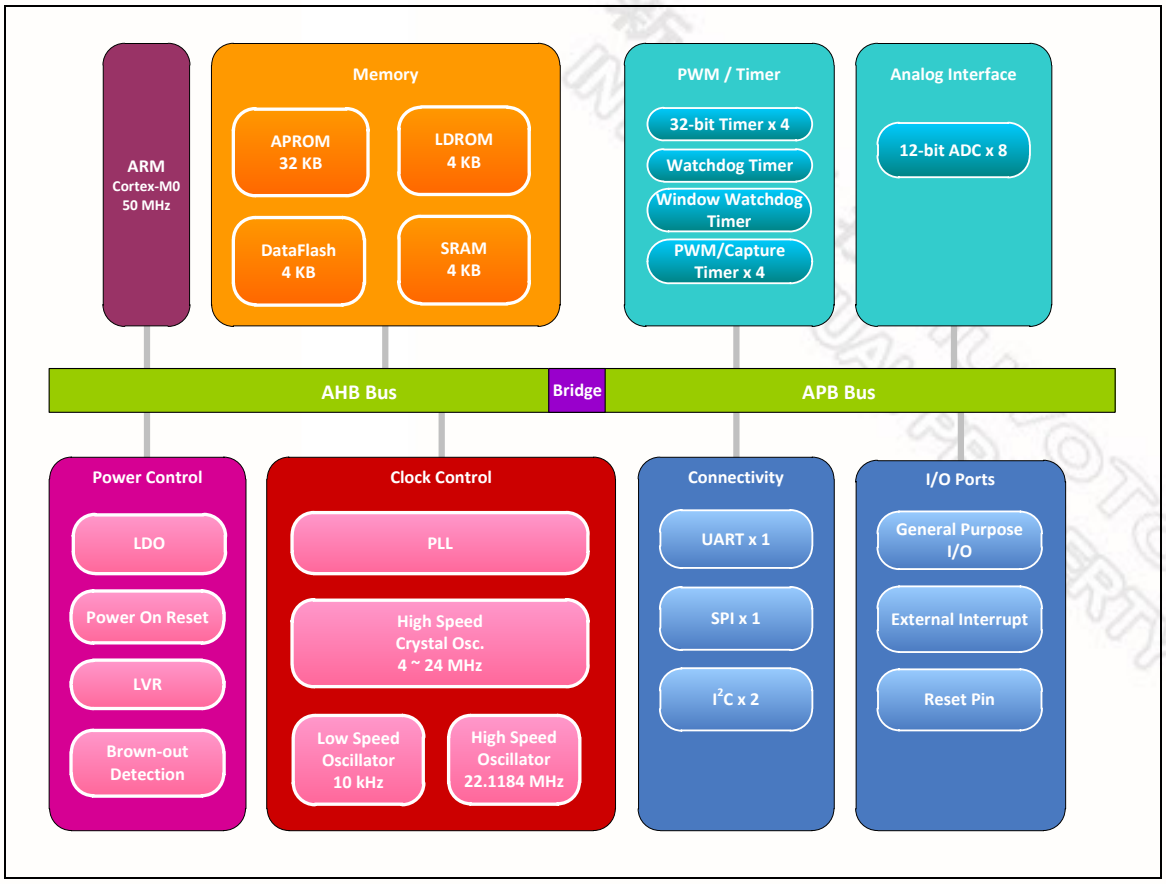

Figure 5.1-1 NuMicro™ M058S Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

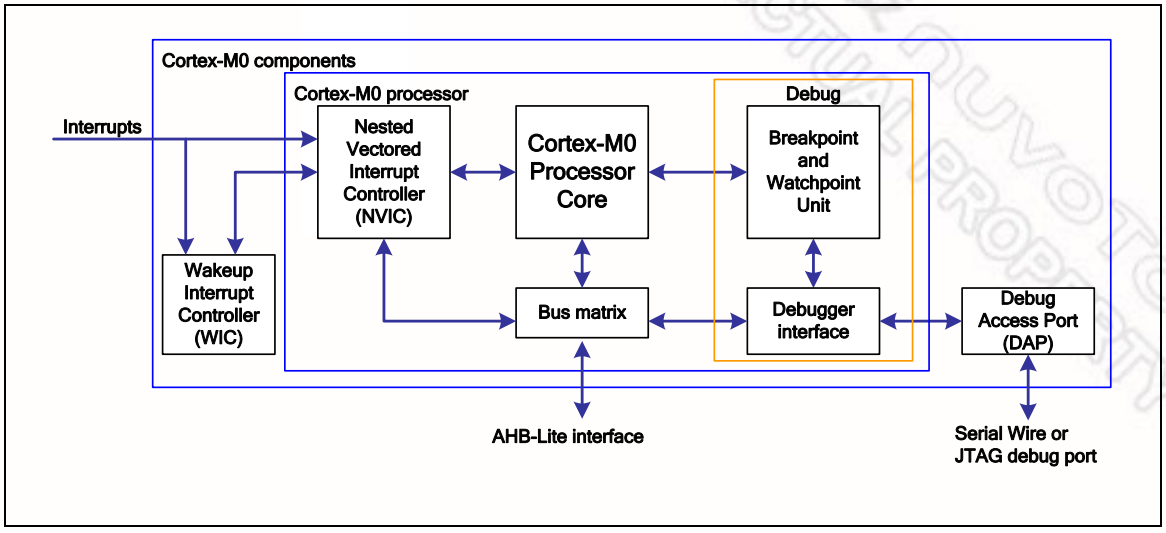

Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- **A low gate count processor the features:**
  - The ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - ARMv6-M compliant 24-bit SysTick timer.
  - A 32-bit hardware multiplier.
  - The system interface supports little-endian data accesses.
  - The ability to have deterministic, fixed-latency, interrupt handling.
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
  - C Application Binary Interface compliant exception model.
    This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.

- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

- **NVIC features:**
  - 32 external interrupt inputs, each with four levels of priority.
  - Dedicated non-Maskable Interrupt (NMI) input.
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and provides Ultra-low Power Sleep mode
- **Debug support:**
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- **Bus interfaces:**
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset Pin (nRST)
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.3 System Power Architecture

In this device, the power architecture is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8 V power for digital operation.

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the M058S series.

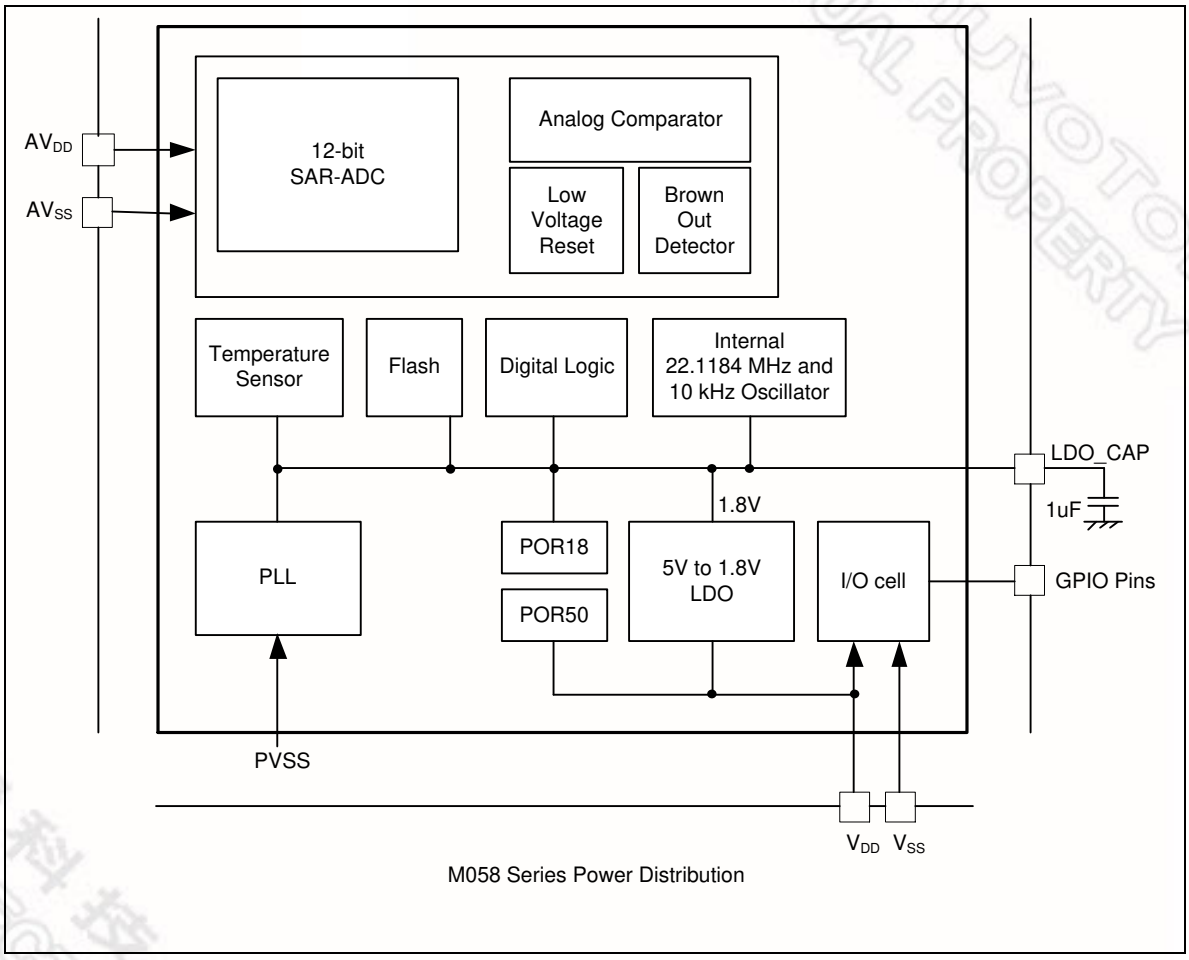

Figure 6.2-1 NuMicro™ M058S Power Architecture Diagram