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GPS RADIONOVA ® RF Antenna Module

Part No. M10478-A1

Product Specification

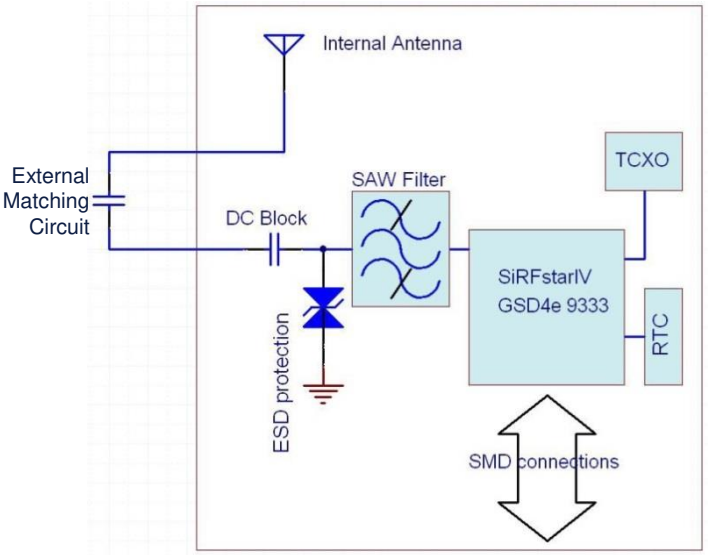
Applications

- **Personal Navigation Devices (PNDs)**
- **Portable Media Players (PMPs)**
- **Personal Digital Assistants (PDAs)**
- **Feature phones / Smart phones**
- **Tablet PCs / eReaders**
- **Asset Tracking / Personal Safety**

Features

- Easy to use, low cost single package GPS RF antenna module
- SiRFstarIV™ 9333 GPS chipset
- Ultra small SMT package; 13.8 x 9.5 x 1.8mm
- Low current consumption <10mW required for TricklePower™ mode
- Novel external matching ensure easy tuning for each platform
- Anti Jammer Remover
- SiRF Instant Fix - SGEE (Server Generated EE) & CGEE Client Generated EE usage (SiRF Instant Fix)

Functional Block Diagram



Description

Antenova M2M's GPS RADIONOVA® M10478-A1 RF Antenna Module is an ultra compact single package solution to combine RF and antenna on the same module. The M10478-A1 is a highly integrated GPS RF Antenna Module suitable for L1-band GPS and A-GPS systems. The device is based on the high performance CSR SiRFstarIV™ GPS architecture combined with Antenova's high efficiency antenna technology, and is designed to provide an optimal radiation pattern for GPS reception.

All front-end and receiver components are contained in a single package laminate base module, providing a complete GPS receiver for optimum performance. The M10478-A1 operates on a single 1.8V positive supply with low power consumption and several low power modes for further power savings. An accurate 0.5ppm TCXO ensures a short TTFF. The M10478-A1 is supported by SiRF stand-alone software and is compatible with UART, SPI, I2C host processor interfaces.

Providing a true drop in solution with the antenna and RF in a single SMT package, GPS RADIONOVA® M10478-A1 offers ease of integration and shorter design cycles for faster time to market.

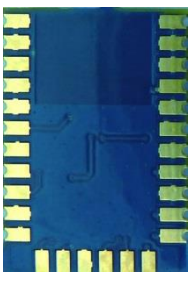
Package Style

SMD Castellated pads enable SMT placement and reflow as well as hand soldering.

13.8 x 9.5 x 1.8mm RF Antenna Module

Top View

Bottom View



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Main Supply Voltage	-0.2	2.2	V
V_{IO}	Supply voltage I/O ring	-0.2	3.6	V
ESD	Electrostatic Discharge Immunity (HBM)	-2.0	2.0	kV
RF_{IN}	Maximum RF Input Power	N/A	+10	dBm
T_{STG}	Storage Temperature	-40	+85	°C
$V_{ON/OFF}$	ON/OFF Pin Voltage	-0.2	+2.2	V

* Exposure to absolute ratings may adversely affect reliability and may cause permanent damage.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Main Supply Voltage	1.71	1.8	1.89	V
V_{IH}	High Level Input Voltage	0.7xVDD	-	3.6	V
T_{OP}	Operating Temperature	-40	-	+85	°C

DC Electrical Characteristics

Conditions: V_{CC} = 1.8V, T_{OP} = 25 °C

Symbol	Parameter	Typ	Unit
$I_{CC(PK)}$	Peak Acquisition Current	47	mA
$I_{CC(AVG)}$	Average Tracking Supply Current	31	mA
$I_{CC(HIB)}$	Hibernate (Sleep) Power Supply Mode	20	µA
$I_{CC(MPM)}$	Micro Power Mode Average Current	500	µA

RF Specifications

Conditions: V_{CC} = 1.8V, T_A = 1.8V, Freq = 1575.420MHz

Symbol	Parameter	Typ	Unit
P1dB	1dB Compression Point	-62	dBm
NF_{LNA}	LNA Noise Figure	2	dB
ANT_{RL}	Antenna Return Loss	-15	dB
ANT_{BW}	Antenna Bandwidth at -10dB return loss	30	MHz
ANT_{EFF}	Antenna Total Efficiency	>40	%
ANT_{EFF_RHCP}	Antenna RHCP Efficiency	%	%

Band Rejection*

Frequency	Standard	Typ*	Unit
698-798	LTE700	45	dB
824-849	Cellular CDMA	45	dB
869-894	GSM850	45	dB
880-915	GSM900	45	dB
1710-1785	GSM1800/DCS	54	dB
1850-1910	GSM1900/PCS	54	dB
1920-1980	WCDMA	50	dB
2400-2492	WLAN, BT and WiMAX	44	dB
2500-2690	LTE2600	42	dB

*Does not include antenna rejection.

Mechanical Specifications

Parameter	Typ	Unit
Module exterior dimensions (L x W x H)	13.8 (+0.1/-0.1) x 9.5 (+0.1 / -0.1) x 1.8 (+0.2 / - 0.0)	mm
Module support and connection	Suface mounted (SMD)	-
Module mass	<1	g

System Specifications

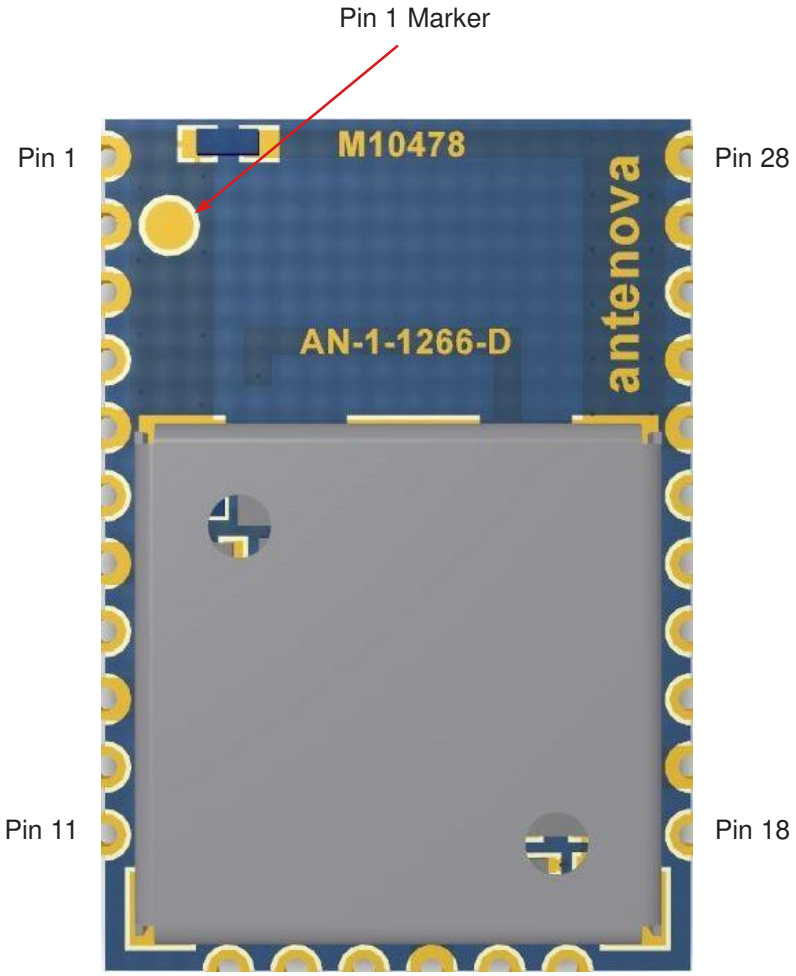
Communication	Specification
Data Output Protocol	NMEA 0183 or OSP (SiRF Binary)
Host Interfaces	UART
	SPI (slave)
	I²C
Default data rate on UART	1200 baud to 1.2288 Mbaud
GPS Engine	
Chip	SiRFstarIV GSD4e-9333 WLSCP
Channels	48 Track Verification Channels
TCXO	0.5ppm
Accuracy	
Horizontal Position Accuracy[1]	<2.5m CEP
Maximum Position Update Rate	1 Hz
Sensitivity	
Autonomous Acquisition	-147dBm
Navigation	-160dBm
Tracking	-163dBm
TTFF	
Hot Start	<1s
Warm Start	<35s (typical)
Cold Start	<35s (typical)
General	
Maximum Altitude	<18.288 km
Maximum Speed	<514 m/s
Active Jammer Remover	Removes in-band jammers up to 80dB-Hz Tracks up to 8 CW jammers
Additional Features	SBAS, WAAS, EGNOS, QRZZ, GAGAN Support
CGEE	Client Generated Extended Ephemeris

[1] 50% CEP, Open-Sky, 24hr Static, -130dBm, good view of the sky

Pin out Description

Table shows the designation and function of each pin on the M10478-A1 module. Please note that several pins have multiple functions.

Pin	Designator	Description
1	GND	Ground connection
2	GND	Ground connection
3	GND	Ground connection
4	ANT_OUT	RF from internal antenna to external matching circuit
5	GND	Ground connection
6	ANT_IN	RF from external matching circuit back into module
7	GND	Ground connection
8	VCC	Main DC supply, 1.8V
9	GND	Ground connection
10	EXT_RST	External Reset - Leave floating and GND to reset
11	TM	1PPS Tim Mark Out
12	EIT	• GPIO4 • SPI_MOSI Serial flash data output
13	DR_I2C_DIO	• GPIO0 • Dead reckoning I²C bus data (SDA) • SPI_MISO serial flash data input pin
14	DR_I2C_CLK	• GPIO1 • Dead reckoning I²C bus data (SCL) • SPI_CLK serial flash SPI clock
15	GND	Ground connection
16	ECLK	• GPIO3 • SPI_CS# serial flash chip select for SPI
17	TSYNC	• GPIO2 • Time aiding input strobe
18	WAKUP	Wakeup output control of external memory or power supply; active high unless chip is in low power state.
19	GND	Ground connection
20	TX	UART Transmit data line
21	RX	UART Receive data line
22	CS_RTS	UART Request to send. Used for host port strap
23	CLK_CTS	UART Clear to send. Used for host port strap
24	GND	Ground connection
25	GND	Ground connection
26	ON_OFF	Run/Sleep hardware control line. Host controlled. Cannot be left floating
27	GND	Ground connection
28	GND	Ground connection

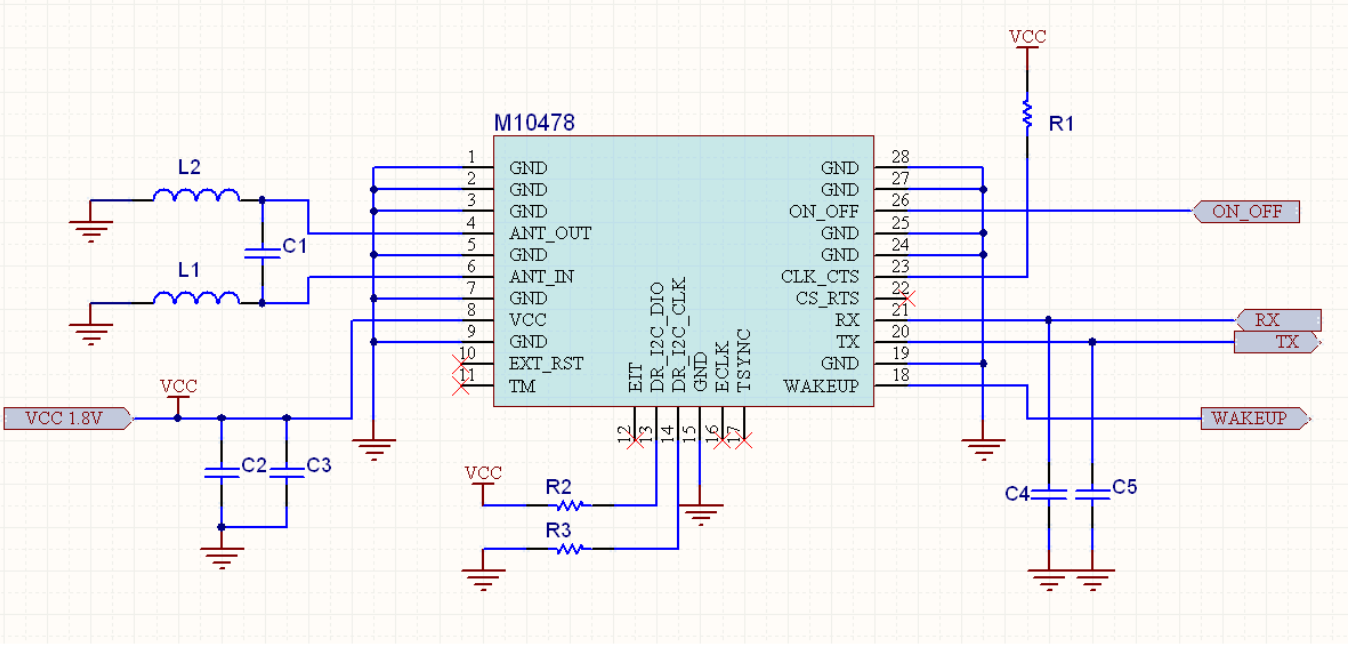

Pin 1 Marker
Pin 1
Pin 28
Pin 11
Pin 18
M10478
AN-1-1266-D
antenova

Application Schematic Example for M10478-A1: UART - 9600 Baud

The circuit below shows a basic design for use with the UART interface and configuring the default baud rate to 9600.

Host Interface = UART

Baud Rate = 9600 (Hardware configured)



Bill of Material

Designator	Value	Description/Comments	Quantity
C1, L1, L2	TBD	Depending on device antenna matching circuit	TBD
C3, C4, C5	22pF capacitor	Decoupling capacitor. Place close to corresponding pin	3
C2	2.2uF capacitor	Decoupling capacitor. Place close to corresponding pin	1
R1, R2, R3	10K resistor	Used for Pull up/Down	3

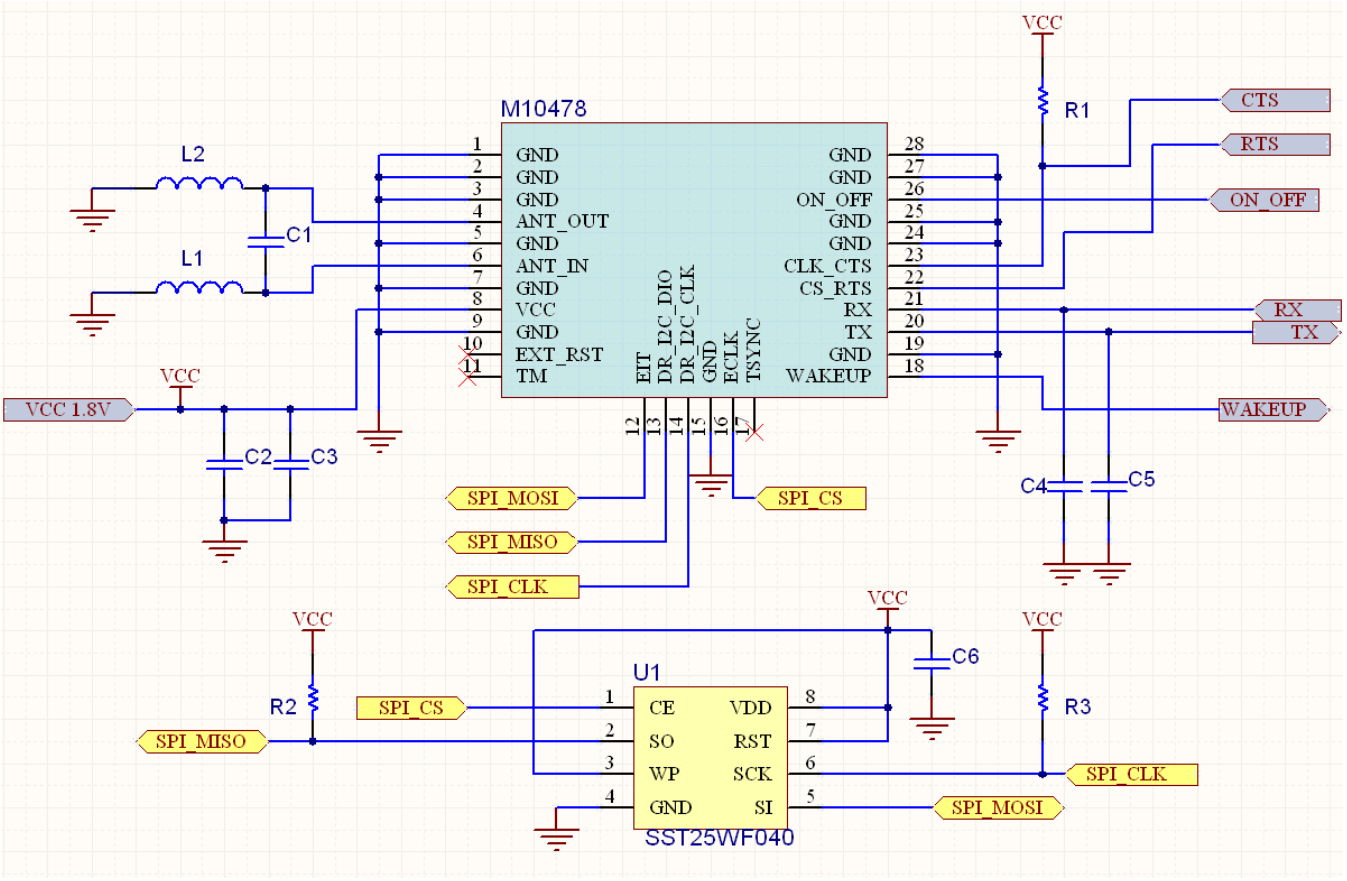
Application Schematic Example for M10478-A1: UART with External SPI Serial Flash

This example shows the module with an external SPI serial flash. This allows simultaneous storage for SGEE and CGEE (up to 31 days in length), and ROM patch storage.

Host Interface = UART

Baud Rate = 4800 (Default)

External Memory Interface = SPI bus



Bill of Material

Designator	Value	Description/Comments	Quantity
U1	SST25WF040-40-51-QAE	SST serial flash memory 4MB	1
C1, L1, L2	TBD	Dependant on device matching circuit	TBD
C3, C4, C5	22pF capacitor	Decoupling capacitor. Place close to corresponding pin	3
C2	2.2uF capacitor	Decoupling capacitor. Place close to corresponding pin	1
C6	0.1uF capacitor	Decoupling capacitor. Place close to corresponding pin	1
R1, R2, R3	10K resistor	Used for Pull up/Down	3

Host Port Selection Straps

The host interface is selected with hardware setup. The table below shows the configuration that determines the interface used. The interface cannot be changed dynamically after start-up.

Interface	Pin 23 (CLK_CTS)	Pin 22 (CS_RTS)
SPI	Leave Floating	Leave Floating
UART	PU	Leave Floating
I²C	Leave Floating	PU

Host Baud Rate/Protocol Selection

With the GSD4e 9333 chip the default baud rate and output protocol is user configurable at start-up with a hardware configuration. This is limited to the values in the following table.*

*If using the I²C interface for external sensor or external memory, then these pins cannot be used for configuration of the Baud rate or protocol. This means that the module will return to a default setting for UART of 4800 baud.

The baud rate and output protocol can be changed dynamically after start up using the relevant commands. Please contact Antenova for more information about protocol messages.

Hardware Baud Rate Selection Table

Baud Rate	Pin13 (DR_I2C_DIO)	Pin 14 (DR_I2C_CLK)
4800	PU	PU
9600	PU	PD
38400	PD	PU
115200 (OSP)	PD	PD

PU = Pull up resistor to VCC (10K Ω)
PD = Pull down resistor to GND (10K Ω)

Host Interface Overview

UART Interface

The default UART communication setting for the M10478-A1 is NMEA-0183 protocol at 4800 Baud, 8 data bits, 1 stop bit, no flow control.

- TX: Output from the GSD4e
- RX: Input to the GSD4e
- RTS (optional): hardware flow control, high when ready to transmit
- CTS (optional): hardware flow control input, high when host allows transmission

While RX and CTS inputs are 3.3V compatible, if RX is driven from a source higher than 1.8V, current may flow from the driver in reverse through the GSD4e's ~80kΩ internal pull-up resistor. TX has maximum 1.8 V logic high output level and may require an external level shifter to interface with a 3.3V input on a host.

UART Interface Logic Levels

Symbol	Description	Min	Max	Unit
V_{IL}	Low Level Input Voltage	-0.4	0.45	V
V_{IH}	High Level Input Voltage	0.7 x V_{CC}	3.6	V
V_{OL}	Low Level Output Voltage	-	0.4	V
V_{OH}	High Level Output Voltage	0.75 x V_{CC}	-	V

Configuration 1:

- RX and TX data lines only, no hardware or software flow control

Configuration 2:

- RX and TX lines for data transmissions
- RTS and CTS for hardware flow control under standard hardware flow control principles
- Transmission stops at the end of the current character and restarts when CTS goes high.

GSD4e may lose or garble serial messages if host flow control throttling is too severe. GSD4e design expects unrestricted outflow of serial messages.

The UART interface can be run at baud rates from 1200 to 1.8432 MBaud. The default protocol is determined by hardware configuration (see Hardware Baud Rate Selection Table above).

Host SPI Interface (Slave)

The host interface SPI is a slave mode SPI.

The 4 SPI pins are:

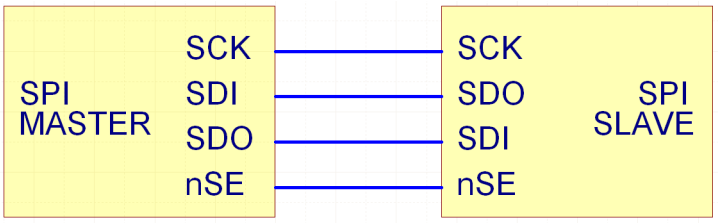
- Pin 13: slave SPI data output (MISO)
- Pin 12: slave SPI data input (MOSI)
- Pin 14: slave SPI clock input (CLK)
- Piin 16: slave SPI chip select (CS#) active low

The maximum clock frequency supported is 6.8MHz.

To allow the module to awaken or signal the host that messages are ready within the GSD4e, the GSD4e software can be programmed or configured to generate a “Message Waiting” signal on a pre-assigned GPIO.

While the Host SPI serial Input and Host SPI clock Input are 3.3V compatible, if Host SPI serial Input is driven from a source higher than 1.8V, excess leakage current may flow through the ~80kΩ internal pull-up resistor.

Host SPI serial Output has maximum 1.8V logic high output level and may require an external level shifter to interface with a 3.3V input.



The following internal operation details are provided to assist with implentation troubleshooting:

- TX and RX each have independent 1024 byte FIFO buffers
- RX and TX each have independent software-specified two byte idle patterns
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled
- RX FIFO detects a software specific number of idle pattern repeats and then disables FIFO input until the idle pattern is broken
- FIFO buffers can generate an interrupt at any fill level
- SPI detects synchronization errors and can be reset by software.

Host I²C Interface

The GSD4e supports two-wire I²C operation in multi-master mode only, with behavior comparable to UART mode operation.

- Address format is 7-bit (default) or 10-bit. I²C supports multiple masters and multiple slaves. The GSD4e address as master (when sending) is 0x62 and as slave (when receiving) is 0x60
- Current I²C Data rates: bit clock rates are 400 kbps (default – fast mode) and 100 kbps (standard mode). High speed mode is not supported. Data rate can be changed using OSP message ID 178
- Internal FIFOs for RX and TX are 64 bytes.

For proper operation, external pull-ups are required to ensure proper rise times with stray shunt capacitances from attached loads and traces.

SPI and I²C Interface (Master Mode)

The M10478-A1 provides an auxiliary serial interface that can be configured as either a master I²C interface or a master SPI bus. These features are implemented using either 2 or 4 of the GPIO pins on M10478-A1. Only one of these buses may be implemented on a receiver.

At start-up, the receiver automatically detects either an I²C EEPROM or a SPI serial flash memory and sets itself appropriately. If GSD4e WLCSP does not detect memory of either type, the system is configured for an I²C bus for sensor interface.

Master I2C Interface

This mode is the default for the receiver. It can be used to communicate with MEMS sensors such as accelerometers, Magneto-meters and altimeters, and with EEPROM storage devices. Some features of the interface include:

- Support for most common sensor formats (accelerometers, gyros, magnetometers, altimeters)
- Support for multiple data lengths
- Standard I²C bus data rates of 100kbps and 400kbps
- Accepts both 64KB and 128KB EEPROMS
- 128KB EEPROMs can store server-generated EE files up to 7 days in length

Master SPI Interface

Non-volatile memory storage can be provided by either 2Mbit or 4Mbit serial flash memories from either SST or EON. The flash memory can store a ROM patch, both server-generated and client-generated extended ephemeris files (up to 31 days in length if 4MB or greater), satellite almanacs, crystal temperature characterization data and data logs. All of these items can be stored simultaneously on the same flash device. Through the master SPI interface, GSD4e WLCSP reads and writes data at approximately 1.0Mbps, with a maximum of 1.25Mbps

Power Management

Full Power ON mode

In the FULL ON state, the ARM processor in the GSD4e is enabled and clocked and the system is under software control. This is the operating state during all acquisition and tracking modes. All RF/BB domains are powered and clocked. However, the software has control of clocks and bias currents, it removes the clocks and bias currents from digital and RF/analog circuits when these circuits are not in use.

Hibernate

In Hibernate state, only essential areas are powered, RTC, IO, RAMs. Current levels are typically 20µA.

At start-up, the module requires an ON_OFF pulse sent from the host. A second pulse sent from the host will re-enter hibernate mode. The ON_OFF pulse needs to be the rising edge of a low to high pulse, this needs to be longer than 90us.

If the host device does not require the hardware selection of hibernate mode, the wakeup pin can be connected to the ON_OFF pin to automatically wake the module to a full power state.

Trickle Power (TP)

Trickle power enters a duty cycle mode to reduce the average current consumption, but still retaining a high standard of accuracy and performance from the module. This means being able to still track weak signals

Typically under normal conditions TP mode runs in full power for 100-900ms and provides a fix, followed by a 1-10 second interval of a low power standby state. Once in a while (typically every 1800 seconds) the module will return to Full power mode to update the ephemeris data.

When in TP, if the signal conditions are harsh (below 30dB-Hz) the module will automatically switch to Full Power mode to improve the navigation performance. When conditions return to normal, the module will return to TP mode. This results in variable power savings but for a fixed output rate, much more reliable performance. Applications using TP Mode perform similarly to applications using full power, but with significant power savings in strong-signal conditions.

Push to Fix (PTF)

Push to fix is similar to TP except:

- The time in the OFF state is longer
- It uses the hibernate settings
- It has a typical duty-cycle of about 2 hours
- It is prepared to wake any time in response to an edge on the ON_OFF pin

PTF Mode is for applications that require infrequent position reporting. The GPS generally stays in a low-power mode, up to 2 hours. Upon wake-up, GPS data is checked for aging validity versus the position update rate to determine if a refresh of position, time, ephemeris data and RTC calibration is required before the next Hibernate cycle. The PTF Mode puts the receiver into a background duty-cycle mode that provides a periodic refresh of position, GPS time, ephemeris and RTC calibration every 10 seconds to 2 hours.

By default, the PTF Mode period is 30 minutes. It is programmable between 10 seconds and 2 hours. When the PTF Mode is enabled at power on or a new PTF Mode cycle, the receiver stays on FP Mode until a good navigation solution is computed. The Hibernate state follows for the remainder of the period. If it takes 36 seconds to fix position and refresh ephemeris on the default period of 30 minutes, the GPS sleeps for the 29 minutes and 24 seconds.

Upon wakeup, the module will remain in full power mode until a good navigation solution is found.

Micro Power Mode (MPM)

MP Mode is a very low-power maintenance mode. The objective of MP Mode is to remain below a stated average current level while maintaining a low level of uncertainty in time, frequency, position and ephemeris state.

MP Mode operates by capturing a buffer of GPS samples at infrequent intervals and analysing the data to update its time, frequency and position estimates. For satellites needing updated ephemeris data, a data collection is scheduled when strong signals are detected. During the data collection phase, time and frequency calibration operations are also carried out.

When switched on the module updates in cycles, usually 1-10 minutes, or maintenance cycles of 30–60 minutes.

Typical *Capture/Update* frequency varies: about once every ten minutes for 9 seconds. Data collection is twice an hour at ~18 seconds each.

Please contact Antenova for more information for MPM and all other low power states.

SiRF Instant Fix (AGPS)

There are two methods to acquire extended ephemeris data:

- SGEE (Requires network connections)
- CGEE (Module Generated - no network connection needed)

SGEE (Server Generated Extended Ephemeris)

SGEE requires periodically accessing servers to download an extended ephemeris (EE) file and transfer it to GSD4e. GSD4e can store EE data to serial EEPROM, flash or host.

CGEE (Client Generated Extended Ephemeris)

The M10478-A1 supports CGEE (Client Generated Extended Ephemeris). CGEE functionality enables devices without an Internet connection to generate EE information based on BE collected from satellites during normal use. This means the module will collect data automatically to generate a predicted ephemeris file, which can dramatically reduce TTTF. The CGEE is default ON, but only if the module has an external serial flash connected to the SPI bus to be able to store the data. Up to 31 days of predicted data can be stored.

Please contact Antenova for more information on SGEE and CGEE

External Matching

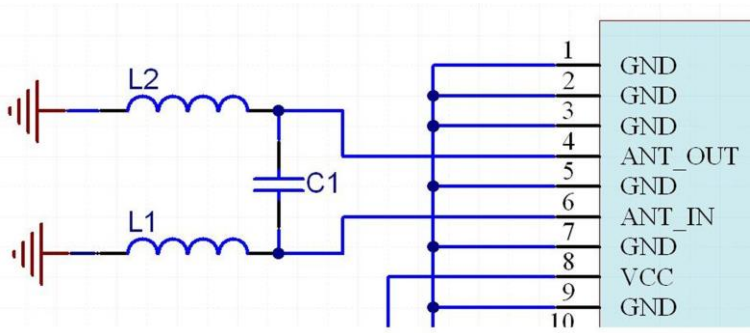
The M10478-A1 module uses a matching circuit on the host PCB in order to fine-tune the on-board antenna to each specific application. This “external matching” allows compensating for the detuning of the antenna caused by various different components that can be close to the M10382 module in the actual application (plastic case, battery, speakers etc).

The external matching must be placed on the host PCB between ANT_OUT (PIN3) and ANT_IN (PIN1). Although 2 components are typically more than enough to match the antenna to the 50Ω impedance required, a Π-network topology with 3 components is recommended for safe proving.

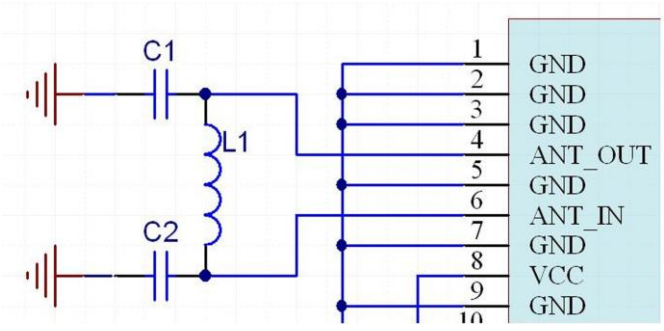
Schematic

Both low-pass and hi-pass topologies for the matching network can be used with similar results. As the same footprint can be used for both topologies, the exact type and value of the components used can be determined during the optimization phase.

- The initial values can be simply chosen as the null-circuit (no impedance matching):
  - Hi-pass:
    - C1 = 18pF
    - L1, L2 = Not Fitted



  - Low-pass:
    - L1 = Jumper (0Ω resistor)
    - C1, C2 = Not Fitted



Type of Matching Components

- Capacitors:
  - Use 0402, COG components
- Inductors:
  - High-Q, wire wound inductors in 0402 size are recommended for maximum performance, e.g. Murata LQW15 series
  - Good quality multi-layer type inductors (e.g. Murata LQG15 series) can also be used as a lower cost alternative

Matching Procedure

The types and values of the matching components must be chosen so that the impedance seen by port ANT_IN (PIN4) is as close as possible as 50Ω. Although it is a relatively simple operation, it requires some RF skills and a VNA (Vector Network Analyzer). **Please contact an Antenova M2M FAE to get support on defining the optimal matching for your specific device.**

External Antenna Support

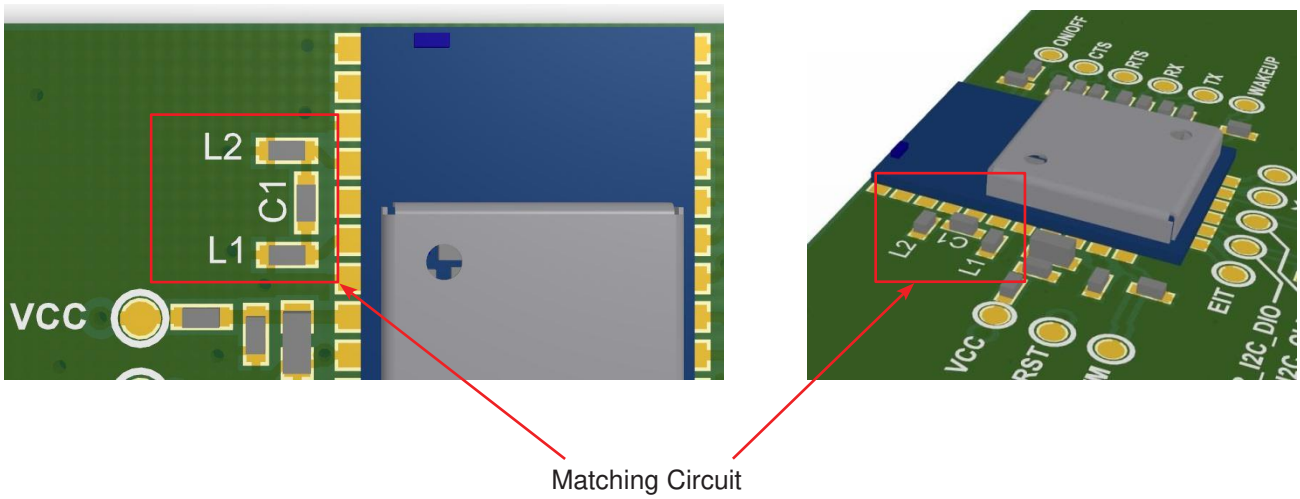
A low cost external circuit can be used to provide external antenna support. Please contact Antenova for more information, and example circuit.

PCB Matching Circuit Layout

The layout of the external matching circuit should be done using the following guidlines:

- Minimize the length of the tracks connecting the ANT_OUT and ANT_IN pads to the matching
- Minimize the length of the tracks between the components
- Use a solid groundplane under the matching circuit area
- Absolutely avoid routing any track under the matching circuit area
- Connect the top ground layer with the ground layer underneath using several vias

Layout drawings (Gerber or other format) are available from Antenova. Please contact your local FAE.

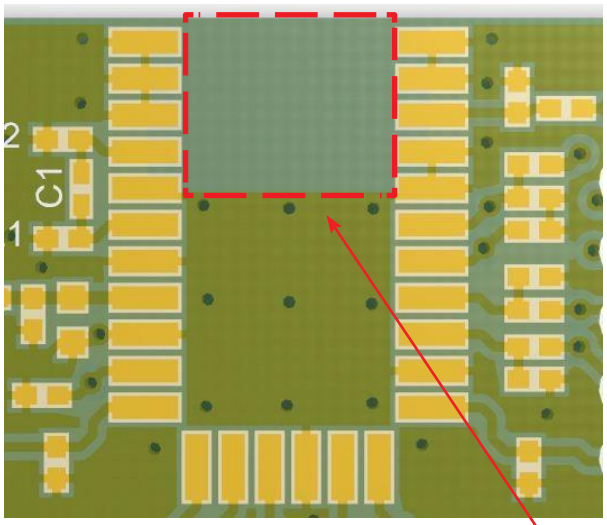


Example of external matching circuit layout

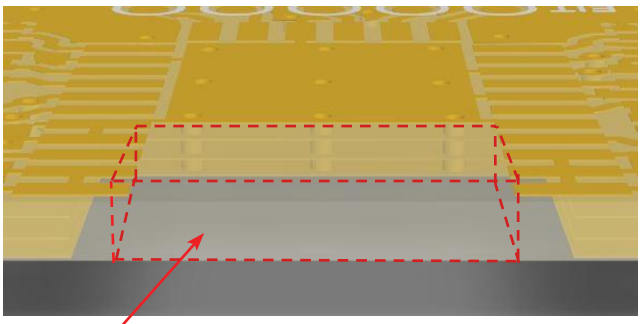
Internal Antenna Clearance

The M10478-A1 module internal antenna requires a small clearance on the host PCB to operate. The clearance means that no Ground or tracks of any kind are allowed to be within this area. This must also be clear through the entire PCB stack up. The minimum area needed clear is 6mm X 4.87mm.

Top view of M10478-A1 Footprint



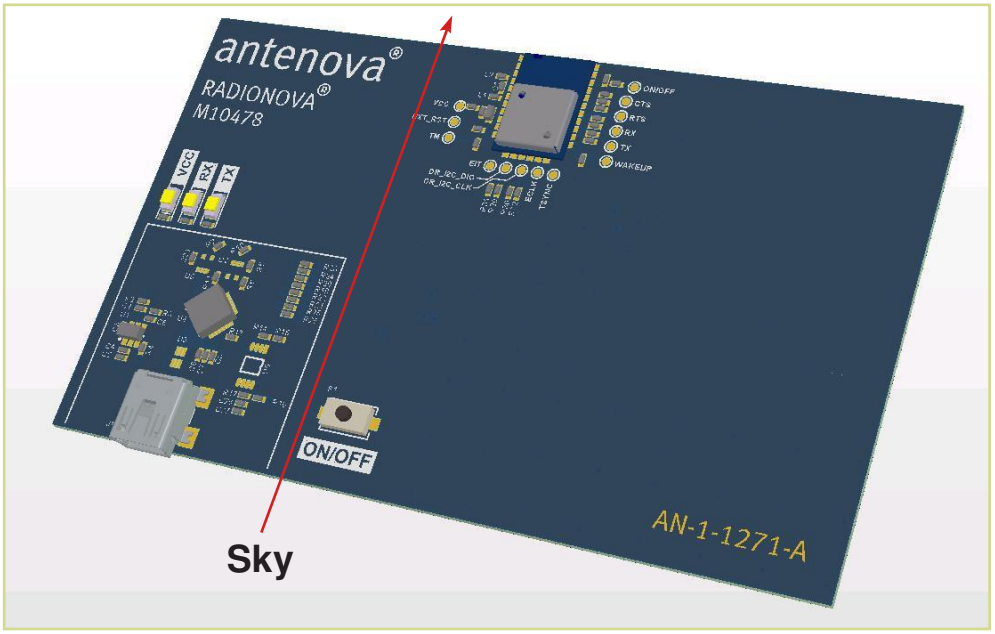
End view - 4 layer PCB stack-up



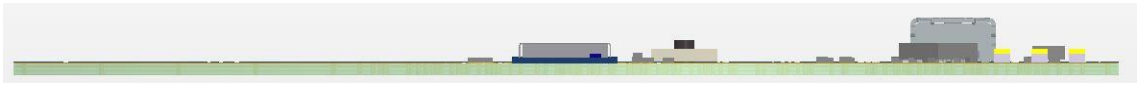
Keep out area

Typical RF Antenna Module Placement

Note: Module placement locations and orientations are critical for achieving optimal system performance. It is strongly recommended to contact Antenova M2M for design recommendations.

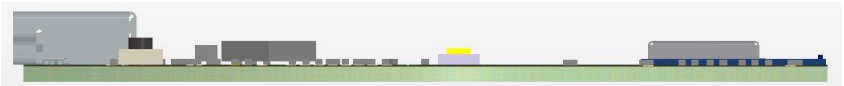


Front View



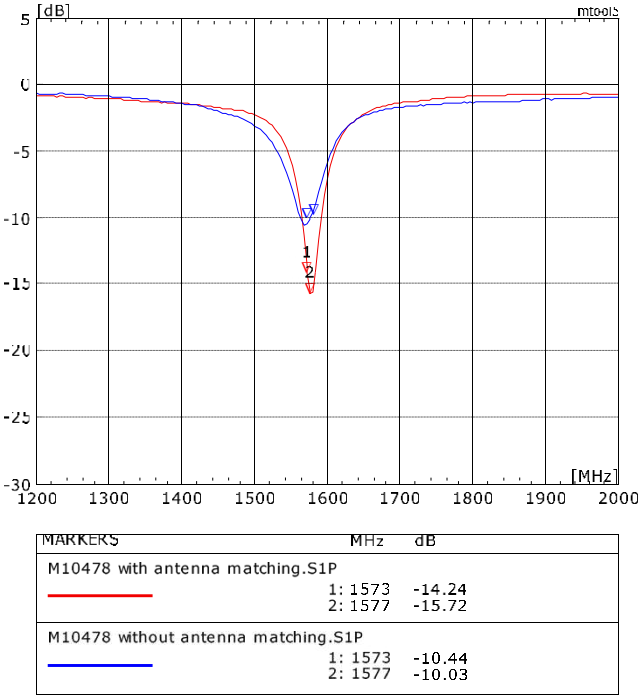
Back View

Side View

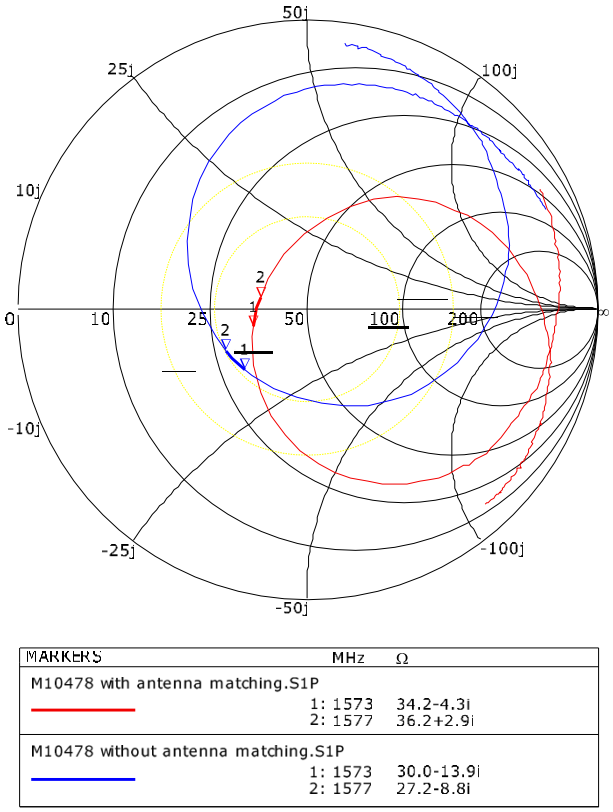


Typical Antenna Matching Results

Typical antenna matching as seen by ANT_IN (Pin 3) is shown in the following plot. The matching bandwidth at -10dB is typically 20MHz. Measured on M10477-U1 test board.



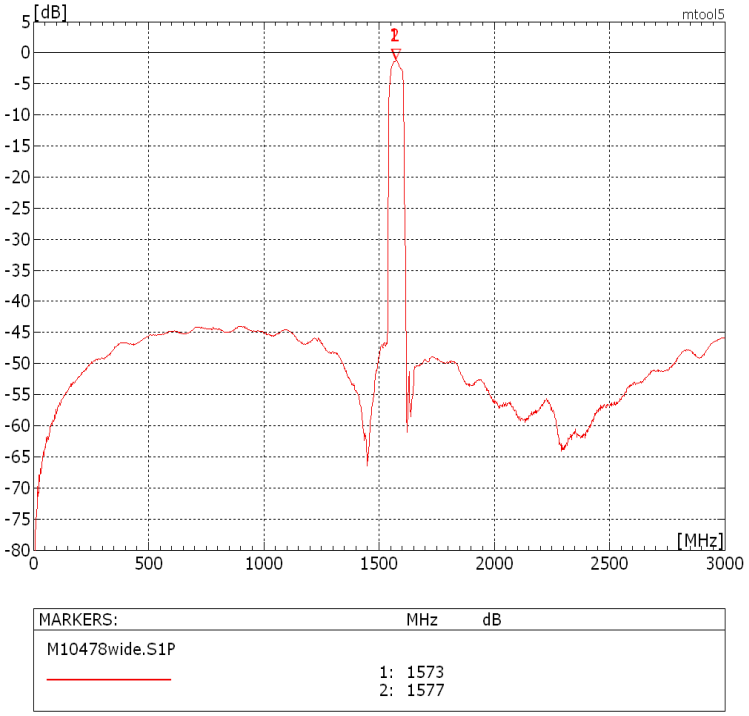
Typical antenna return loss before and after matching



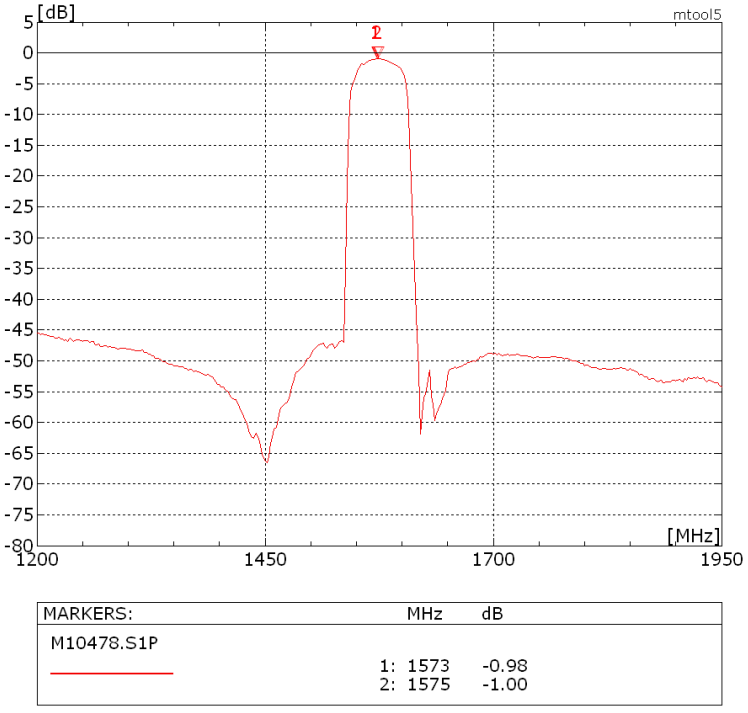
Typical antenna impedance before and after matching

Front-end Rejection

The figure below shows the rejection for the input SAW filter before the RF input, including the effect of pads, tracks, ESD protection and decoupling. The plot can be useful to calculate the isolation required from adjacent transmitters in order to avoid the saturation of the LNA.



Input SAW Rejection - Wideband

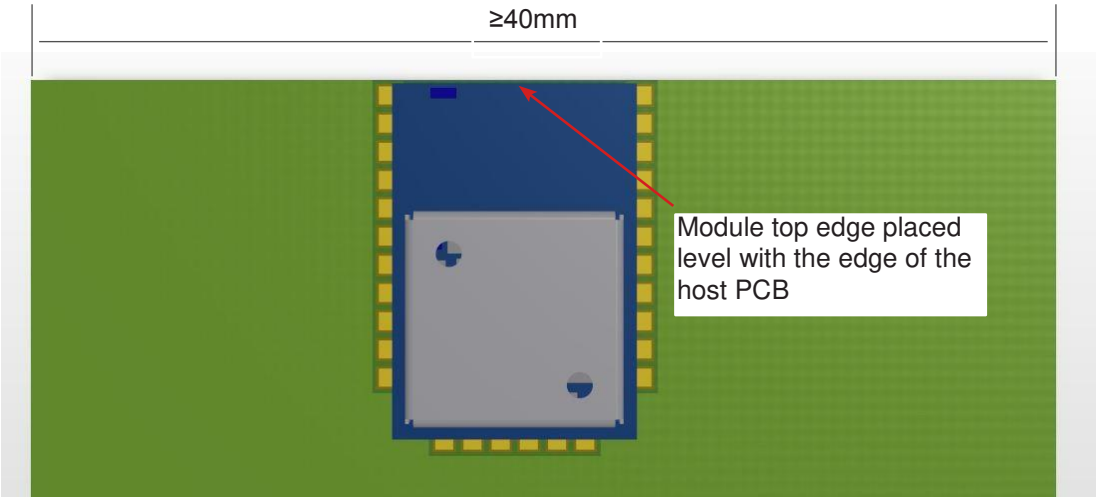


Input SAW Rejection - Narrowband

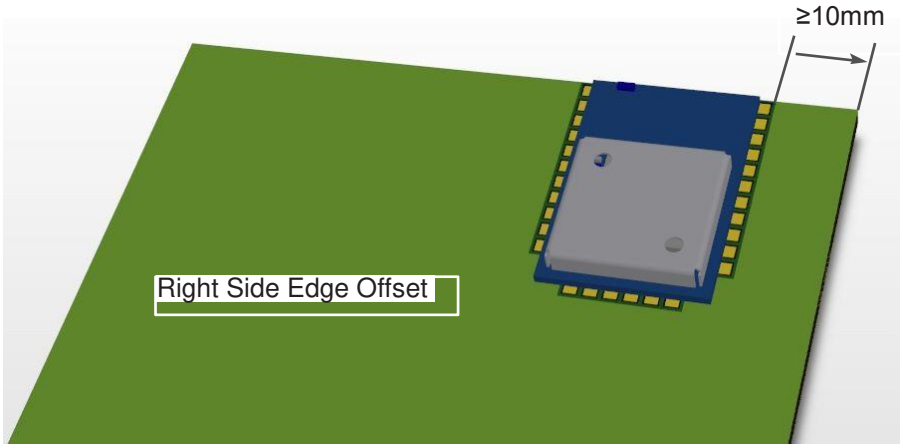
Module Placement Guidelines

Due to the internal antenna, care must be taken when defining the placement of the module on the host PCB. Here are some guidelines that should be used when deciding the position of the module.

- The module top edge must be placed almost level with the edge of the host PCB
- The edge of the host PCB that the module is to be placed at must be a minimum of 40mm in length.



- The central placement of the module is advised. However, an offset placement is also possible.
- For an offset closer to the PCB edge to the right side of the module, a minimum of 10mm distance is required to the edge of the host PCB.



- For an offset closer to the PCB edge on the left side of the module, a minimum of 15mm distance is required to the edge of the host PCB. This additional distance is due to the matching circuit placement.

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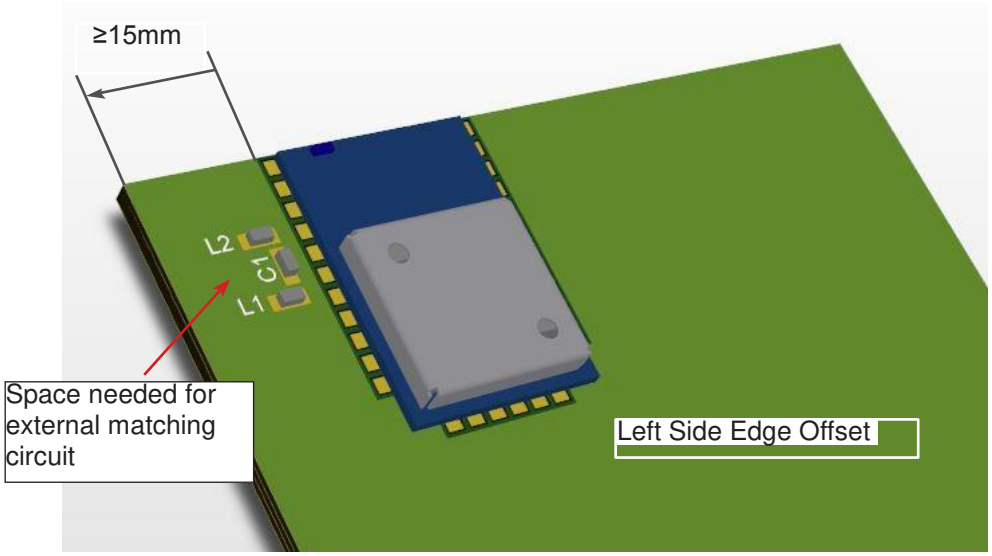
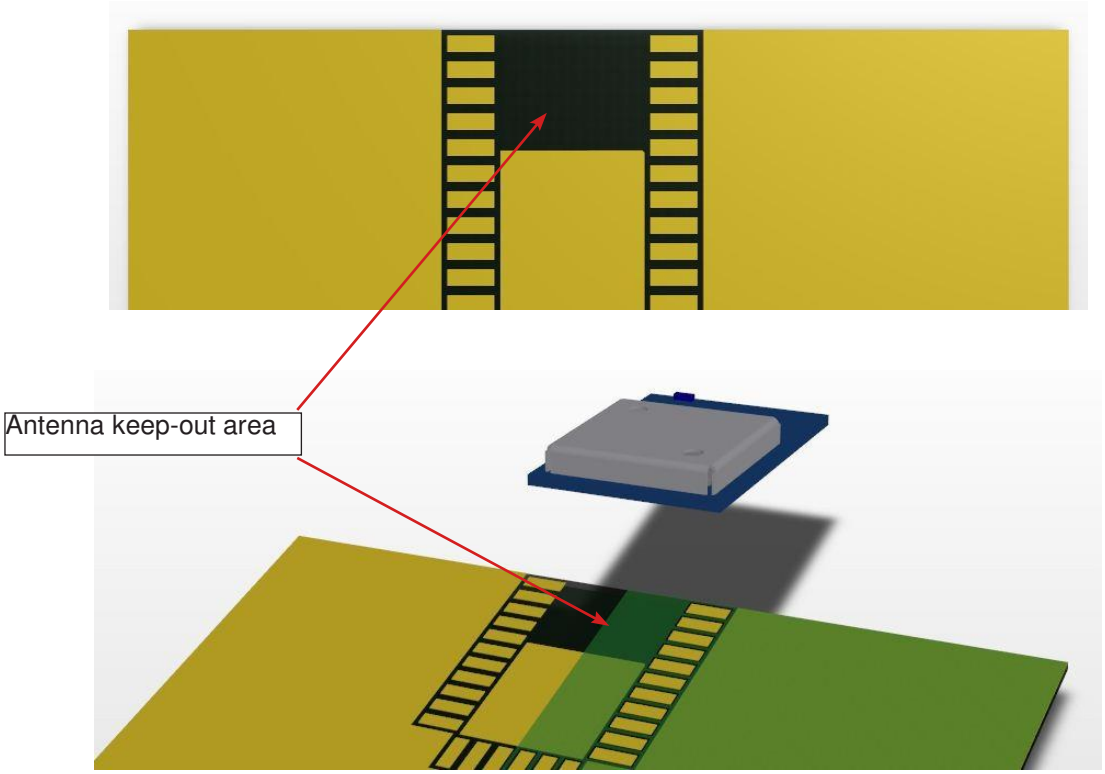
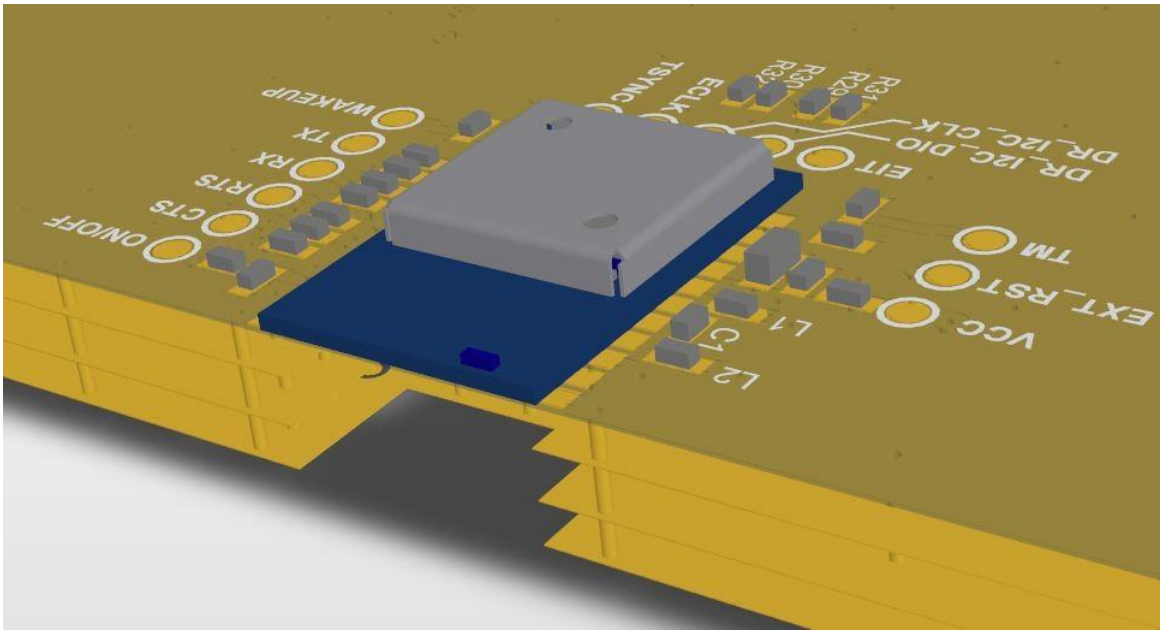


- The antenna uses the host PCB ground to effectively radiate. As such, a GND plane must be placed on the host PCB on at least one layer.
- In the example below, the only area void of GND is the antenna keep-out area.



- An ideal stack-up for a host PCB would be to use the top and bottom layers as GND planes, while using the internal layers for any signal and power planes. This not only helps the GPS antenna to perform effectively, but also helps to reduce any potential noise issues that can be associated with mixed signal PCB's.
- An exaggerated example below shows a 4 layer host PCB, GND flooding all available space not used by signals or components.

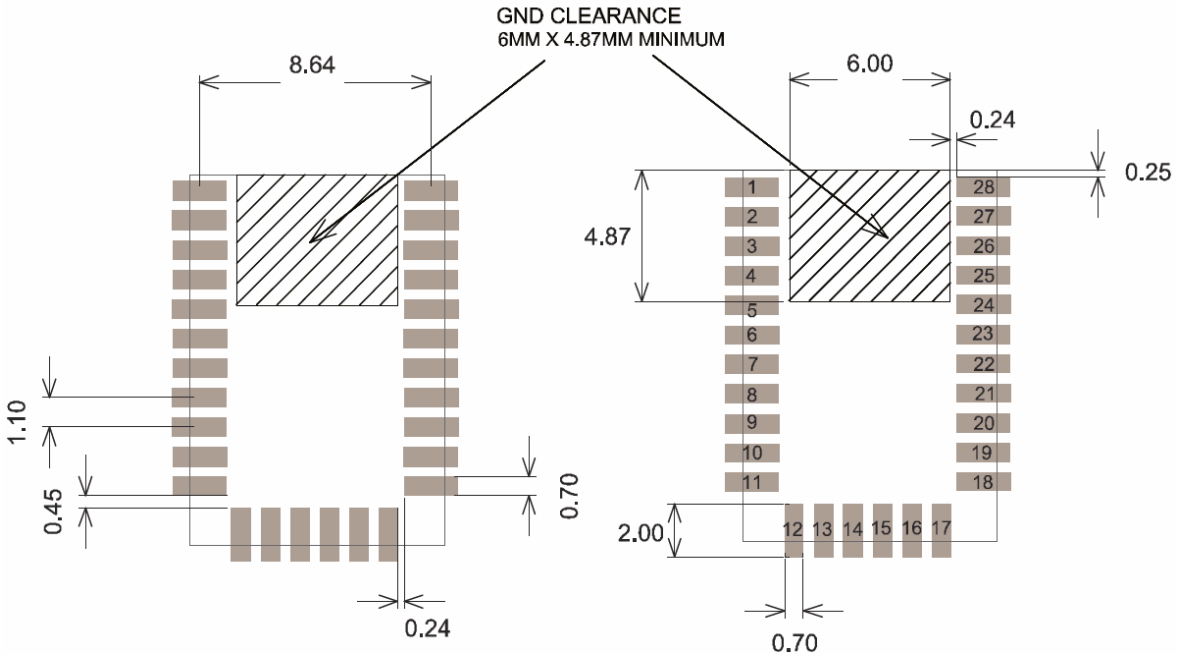


Please contact Antenova M2M for advice on placement.

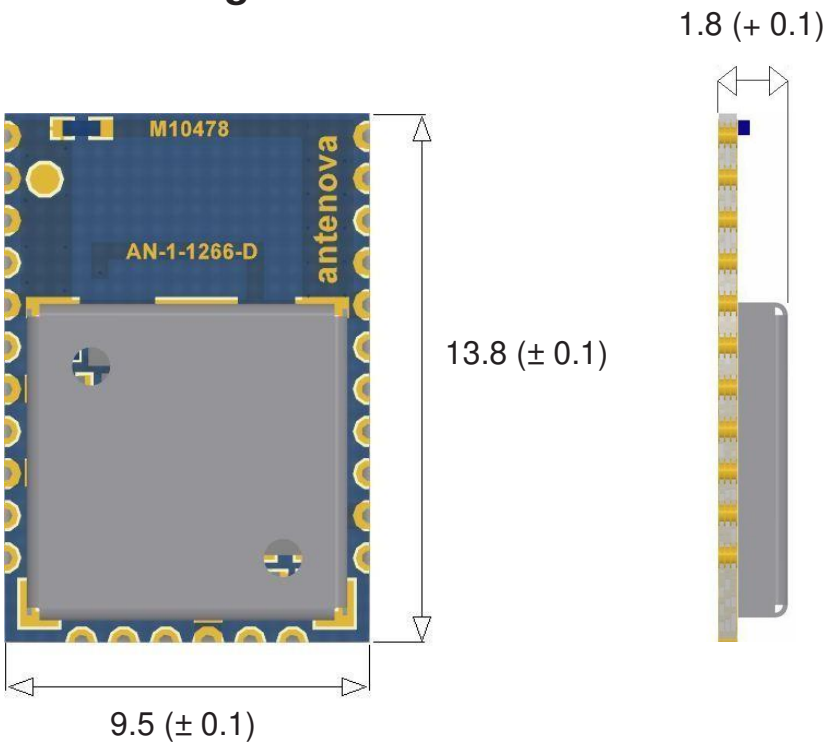
Module Footprint

Below is the recommended footprint for the module. This footprint allows hand soldering.

- All pads are 0.7mm x 2mm
- Pitch is 1.1mm



Mechanical Drawing



All dimensions in mm

Reflow Soldering

Placement

Typical placement systems used for any BGA/LGA package are acceptable. Recommended nozzle diameter for placement: 5mm

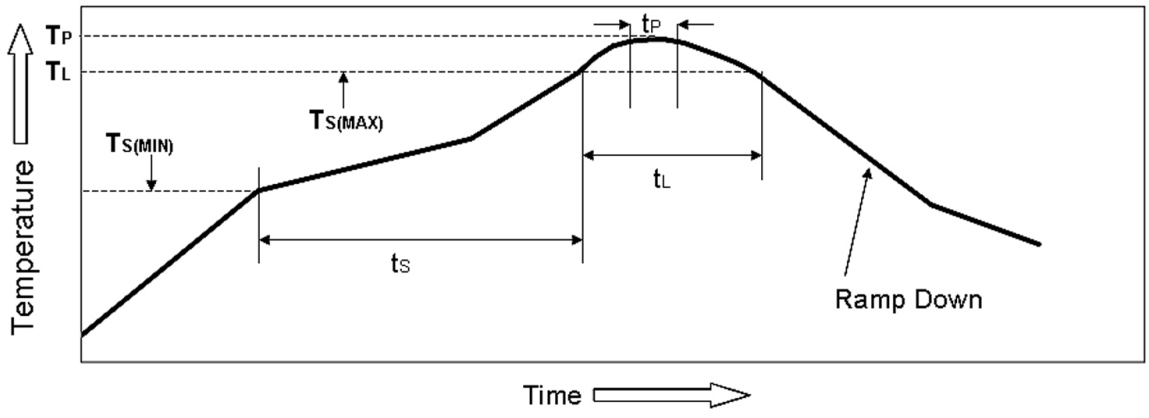
Soldering Paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. An example of suitable soldering paste is Alpha OM350.

Soldering

The recommended soldering profile for M10478-A1 is shown below. However, it is the responsibility of the Contract Manufacturer to determine the exact reflow profile used, taking into consideration the parameters of the host PCB, solder paste used, etc.

Profile Feature		Pb-Free Solder
Pre-Heat	Temperature (T_s) Min	130°C
	Temperature (T_s) Max	220°C
	Time (t_s)	<150s
Reflow	Liquidus Temperature - (T_l)	220°C
	Time (t_l)	45-90s
Peak Package Body Temperature (T_p)		245°C
Time within 5°C of peak temp (t_p)		30s
Average Ramp up rate - T_s(max) to (T_p)		3°C/s
Ramp Down Rate		6°C/s max



Example Reflow profile

The Pb Free Process-Package Peak Reflow Temperature is 260ºC.

Exceeding the maximum soldering temperature could permanently damage the module.