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M2004-01/-11

FREQUENCY TRANSLATION PLL

GENERAL DESCRIPTION

The M2004 variants -01 and -11 are VCSO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation in a high-speed data communications system. The clock multiplication ratio and output divider ratio are pin selectable and also configurable through serial programming. External loop components allow the tailoring of PLL loop response. The M2004-11 adds Hitless Switching with Phase Build-out (HS/PBO) to ensure that reference clock reselection does not disrupt the output clock.

Also read about device variants -21, -31, -41, and -51 in the M2004-x1 Preliminary Information sheet.

FEATURES

- **Ideal for OC-48/192 data clock**
- **Integrated SAW (surface acoustic wave) delay line**
- **VCSO frequency from 300 to 700MHz (Specify VCSO center frequency at time of order)**
- **Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Pin-selectable or serially programmed configuration**
- **The M2004-11 adds Hitless Switching with Phase Build-out (HS/PBO) to ensure SONET/SDH MTIE and TDEV compliance during reference clock reselection**
- **Reference clock inputs support single-ended LVCMOS, LVTTL**
- **Industrial temperature available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

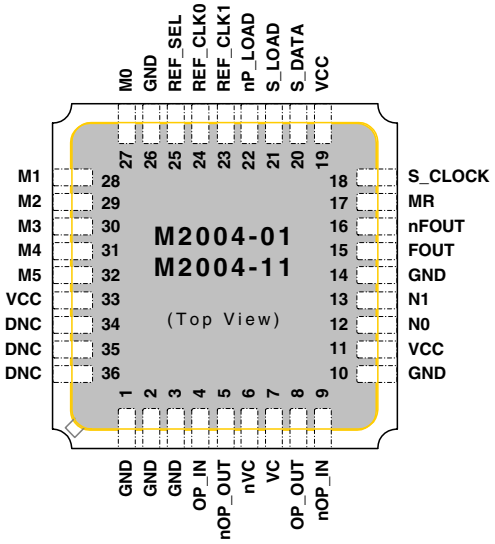


Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input Clock (MHz)	VCSO [1] Freq (MHz)	Output Freq (MHz)	Application
19.44	622.08	77.76	OC-12 / 48 /192
38.80		155.52	
77.76		311.04	
155.52		622.08	
25.00	625.00	156.25	Gigabit Ethernet

Table 1: Example Input / Output Frequency Combinations

Note 1: Specify VCSO center frequency at time of order

SIMPLIFIED BLOCK DIAGRAM

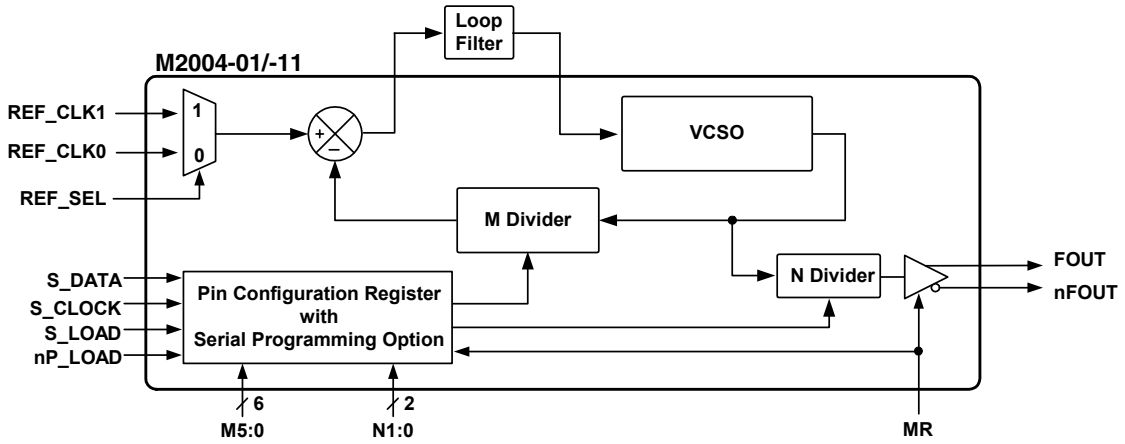


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 6.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	N0 N1	Input	Internal pull-down resistor[1]	N divider (output divider) inputs N1:0. LVCMOS/LVTTL. See Table 5, Pin Selection of N Divider Using N1:0 Pins, on pg. 3.
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.
17	MR	Input	Internal pull-down resistor[1]	Reset: Logic 1 resets M and N dividers and forces FOUT to LOW and nFOUT to HIGH. Logic 0 enables the outputs. LVCMOS/LVTTL. See Table 7, Pin Configuration & Serial Programming Functions, on pg. 5.
18 20 21	S_CLOCK S_DATA S_LOAD	Input	Internal pull-down resistors[1]	Serial programming input pins. LVCMOS/LVTTL. See Table 7, Pin Configuration & Serial Programming Functions, on pg. 5 for how these three pins are used in combination.
22	nP_LOAD	Input	Internal pull-down resistor[1]	Pin-configuration vs. serial programming control. Determines when data present at M5:0 and N1:0 is loaded into M and N dividers vs. when serial programming occurs. LVCMOS/LVTTL. See Table 7, Pin Configuration & Serial Programming Functions, on pg. 5 for how this pin is used.
23	REF_CLK1	Input	Internal pull-down resistor[1]	Reference clock inputs. LVCMOS/LVTTL.
24	REF_CLK0		Internal pull-down resistor[1]	
25	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL. See Table 3, Reference Clock Input Selection, on pg. 3. For the M2004-11, REF_SEL triggers Hitless Switching (HS/PBO) when toggled.
27 28 29 30 31	M0 M1 M2 M3 M4	Input	Internal pull-down resistor[1]	M divider (feedback divider) inputs M5:0. See Table 4, Pin Selection of M Divider Using M5:0 Pins, on pg. 3. See also Table 7, Pin Configuration & Serial Programming Functions, on pg. 5
32	M5		Internal pull-up resistor[1]	
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see DC Characteristics on pg. 7.

DETAILED BLOCK DIAGRAM

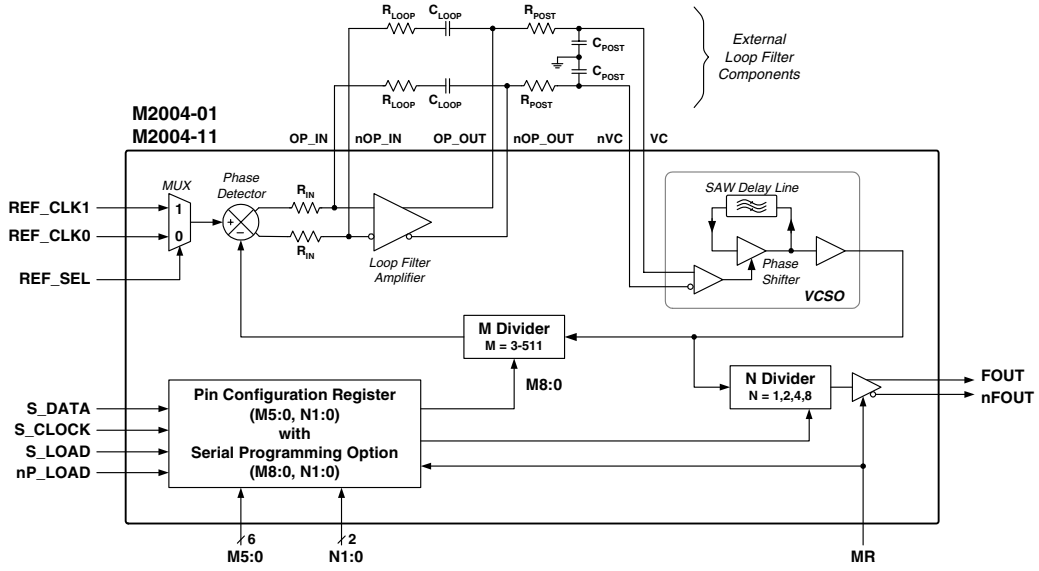


Figure 3: Detailed Block Diagram

DEVICE CONFIGURATION TABLES

Reference Clock Input Selection

REF_SEL Pin Setting (Pin 25)	Reference Input Selection
0	REF_CLK0
1	REF_CLK1

Table 3: Reference Clock Input Selection

M and N Pin Selection Option

Pin Selection of M Divider Using M5:0 Pins

M5:0 Pin Settings[1] (Pins 32 - 27) M5 - M0	Definition	Sample Input Clock Freq (MHz) F_{VCSO}=$_2$ 622.08	F_{VCSO}=$_3$ 625.00
5[4] 4 3 2 1 0	**Feedback Divider Value "M"**		
0 0 0 0 1 1	M = 3 minimum		
0 0 0 1 0 0	M = 4	155.52	156.25
⋮			
0 0 1 0 0 0	M = 8	77.76	
⋮			
0 1 0 0 0 0	M = 16	38.80	
⋮			
0 1 1 0 0 1	M = 25		25.00
⋮			
1 0 0 0 0 0	M = 32	19.44	
⋮			
1 1 1 1 1 1	M = 63		

Table 4: Pin Selection of M Divider Using M5:0 Pins

Note 1: Bits M8:6 default to 0.
Note 2: F_{VCSO} = 622.08 MHz (e.g., M2004-01-622.0800)
Note 3: F_{VCSO} = 625.00 MHz (e.g., M2004-01-625.0000)
Note 4: M5 pin has a pull-up resister; M4-M0, pull-down.

M and N Pin Selection Option (Continued)

Pin Selection of N Divider Using N1:0 Pins

N1:0 Settings (Pin 13 and 12) N1	N0	N Divider Value	Sample Output Frequency (MHz) [1] (FOUT, nFOUT)
0	0	1	622.08
0	1	2	311.04
1	0	4	155.52
1	1	8	77.76

Table 5: Pin Selection of N Divider Using N1:0 Pins

Note 1: F_{VCSO} = 622.08MHz (e.g., M2004-01-622.0800)

Serial Programming Alternative (Using S_DATA Pin)

Serial Bits	Settings per Bit	Definition
T1:0	1 0	**Normal/Test Mode**
	0 0	Normal Operation *
	*Note: T1 and T0, used for test automation, must be set to 0	
N1:0	1 0	**Output Divider Value "N"**
	0 0	N = 1 minimum
	⋮	
	1 1	N = 8 maximum
M8:0	8 7 6 5 4 3 2 1 0	**Feedback Divider Value "M"**
	0 0 0 0 0 0 0 1 1	M = 3 minimum
	⋮	
	0 0 0 1 0 0 0 0 0	M = 32
	⋮	
	0 0 0 1 1 1 1 1 1	M = 63
	⋮	
	1 1 1 1 1 1 1 1 1	M = 511 maximum

Table 6: Serial Programming Alternative (Using S_DATA Pin)

FUNCTIONAL DESCRIPTION

The M2004-01/-11 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks. An internal high “Q” SAW delay line provides a low jitter clock signal.

The device can be pin-configured for feedback divider and output divider values. These divider values can also be set through serial programming. Output is LVPECL compatible. External loop filter component values set the PLL bandwidth to optimize jitter attenuation characteristics.

The M2004-11 adds Hitless Switching with Phase Build-out (HS/PBO) to provide SONET/SDH MTIE and TDEV compliance during a reference clock reselection using the internal mux or when using an external mux.

The M2004-01/-11 is ideal for clock jitter attenuation and frequency translation in 2.5 or 10 Gb optical network line card applications.

Input Reference Clocks

An internal input MUX is provided for input reference clock selection. One input reference clock is selected from between two single-ended LVCMOS / LVTTL clock inputs. The maximum input frequency is 175MHz.

PLL Operation

The M2004-01/-11 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The “M Divider” divides the VCSO output frequency, feeding the result into the phase detector. The selected input reference clock is fed into the other input of the phase detector. The phase detector compares its two inputs. It then causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

The value of M directly affects closed loop bandwidth.

The M Divider

The relationship between the VCSO center frequency (Fvcso), the M divider, and the input reference frequency (Fref_clk) is:

$$Fvcso = Fref\_clk \times M$$

The product of M and the input frequency must be such that it falls within the “lock” range of the VCSO.

See APR in AC Characteristics on pg. 8.

N Divider and Outputs

The M2004-01/-11 provides one differential LVPECL output pair: FOUT, nFOUT. By using the N divider, the output frequency can be the VCSO center frequency (Fvcso) or 1/2, 1/4, or 1/8 Fvcso.

The N1 and N0 pins select the value for the N divider.

See Table 5, Pin Selection of N Divider Using N1:0 Pins, on pg. 3.

When the N divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{N} = Fref\_clk \times \frac{M}{N}$$

Configuration of M and N Dividers

The M and N dividers can be set by pin configuration or serial programming. The divider configuration of the M2004-01/-11 is reset when the input pin MR is set HIGH. MR is set LOW for divider configuration to be operational.

See Table 7, Pin Configuration & Serial Programming Functions, on pg. 5.

Pin Configuration M and N Dividers

The M2004-01/-11 can be pin-configured with the input pins M0 - M5, N0, and N1.

Pin configuration of dividers occurs when nP_LOAD is LOW. The data on pins M5:0 and pins N1:0 is passed transparently (directly) to the M and N dividers.

On the LOW-to-HIGH (rising edge) transition of the nP_LOAD input, the data is latched.

With nP_LOAD set HIGH, the pin-configured values remain loaded in the M and N dividers; the dividers are unaffected by any change to the M5:0 or N1:0 inputs. As a result, the M5:0 and N1:0 pins can be used to set the power-up default values for M and N. (The dividers are also unaffected by any S_DATA serial input as long as there is no rising edge transition of S_LOAD.)

See Table 7, Pin Configuration & Serial Programming Functions, on pg. 5. See also Figure 8, Times for M5:0 and N1:0, on pg. 9.

Serial Programming of M and N Dividers

The M2004-01/-11 is serially programmed with S_DATA, S_CLOCK, and S_LOAD.

See Figure 4, Serial Configuration Timing Diagram, below.

Serial input mode is enabled when nP_LOAD is HIGH and S_LOAD is LOW (at point "a" in the the timing diagram, Figure 4). Data on the S_DATA input pin is serially loaded into the configuration shift register with each rising edge of the S_CLOCK input. (The T1 bit is input first, M0 last.)

When the shift register is full, its entire contents is loaded in parallel into the M and N dividers. This occurs on the rising edge of the S_LOAD input (at point "b" in the timing diagram). This load is transparent; the dividers immediately contain the serially programmed values.

If S_LOAD is held HIGH, any S_DATA input is passed transparently (directly) to the M and N dividers on each rising edge of S_CLOCK.

The data is latched on the falling edge transition of the S_LOAD input (at point "c" in the timing diagram). With S_LOAD set LOW, the serially programmed values remain in the M and N dividers, unaffected by any serial pin input.

See Table 7, Pin Configuration & Serial Programming Functions, below. See also Figure 8, Times for M5:0 and N1:0, on pg. 9.

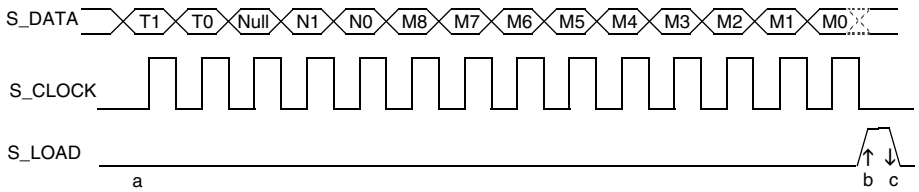
Pin Configuration & Serial Programming Functions

L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

Pins							Function
MR	nP_LOAD	M5:0	N1:0	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Resets the dividers and forces FOUT to LOW and nFOUT to HIGH.
Pin Configuration of M and N Dividers							
L	L	Data	Data	X	X	X	Data on M5:0 and N1:0 input pins is passed directly (and become immediately transparent) to the M and N dividers respectively.
L	↑	Data	Data	L	X	X	Data is latched into M and N dividers and remains loaded until next HIGH-to-LOW transition of nP_LOAD or a serial load occurs.
Serial Programming of M and N Dividers							
L	H	X	X	L	↑	Data	Serial input mode. Data on the S_DATA pin is serially loaded into the shift register on each rising clock of S_CLOCK. (However, serial input does not affect the values in the M and N dividers.)
L	H	X	X	↑	L	Data	Entire contents of the shift register are passed (and become immediately transparent) to the M and N dividers.
L	H	X	X	↓	L	Data	M and N divider values are latched.
L	H	X	X	L	X	X	Serial input does not affect the values in the M and N dividers.
L	H	X	X	H	↑	Data	Serial input affects dividers: S_DATA passed directly to M and N dividers as it is clocked.

Table 7: Pin Configuration & Serial Programming Functions

Serial Configuration Timing Diagram



Points a, b, and c referred to in "Serial Programming of M and N Dividers" description above.
The T1 bit is loaded first, M0 last.

Figure 4: Serial Configuration Timing Diagram

Hitless Switching and Phase Build-out *

A proprietary automatic Hitless Switching (HS) function is included in the M2004-11. The HS function provides SONET/SDH MTIE and TDEV compliance during a reference clock reselection using the internal mux or when using an external mux (through detection of the resulting phase transient).** A Phase Build-out (PBO) function is also incorporated to absorb most of the phase change in the reference clock input.

The combined HS/PBO function is armed after the device locks to the input clock reference. Once armed, HS/PBO is triggered by either:

- Changing REF_SEL to switch the input reference clock.
- Detection at the phase detector of an input phase transient beyond 4 ns.

Once triggered, the HS function narrows loop bandwidth to control MTIE during locking to the new input phase. With proper configuration of the external loop filter, the output clocks will comply with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the phase detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

Note *: The M2004-01 does not include HS/PBO.

Note **: Transient-triggered HS/PBO is not suitable for use with an unstable reference clock that would induce phase jitter beyond 2 ns at the phase detector (e.g., Stratum DPLL clock sources and unstable recovered network clocks intended for loop timing configuration). Therefore, the M2004-11 also offers the internal mux-triggered HS/PBO capability.

When the PLL locks to within 2 ns of the input clock phase, the PLL returns to normal loop bandwidth and the HS/PBO function is re-armed.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2004-01/-11 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 5). Due to the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 5, below.

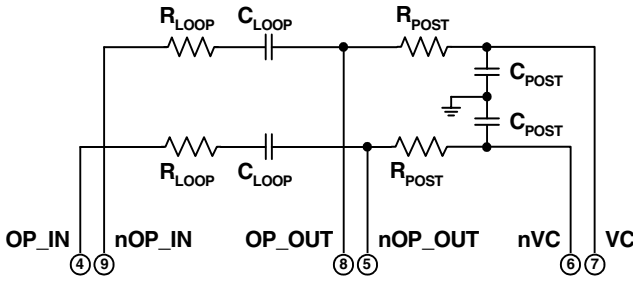


Figure 5: External Loop Filter

PLL bandwidth is affected by the "M" value as well as the VCSO frequency. See Table 8, External Loop Filter Component Values M2004-01/-11, on pg. 6.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

External Loop Filter Component Values [1] M2004-01/-11

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 16kΩ, VCSO Bandwidth = 700kHz. See AC Characteristics on pg. 8 for PLL Loop Constants.

Device Configuration			Example External Loop Filter Component Values				Nominal Performance Using These Values		
F_{Ref} (MHz)	F_{VCSO} (MHz)	M Divider Value	R loop	C loop	R post	C post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44	622.08	32	13kΩ	0.47µF	33kΩ	220pF	3.8kHz	5.6	0.06
19.44	622.08	32	39kΩ	0.022µF	20kΩ	220pF	12.7kHz	7.7	0.03
19.44	622.08	32	2.2kΩ	10.0µF	22kΩ	3300pF	710Hz	4.4	0.10
155.52	622.08	4	3.9kΩ	0.47µF	39kΩ	100pF	11.0kHz	4.7	0.09
155.52	622.08	4	750Ω	10.0µF	7.5kΩ	1000pF	1.6kHz	4.2	0.10

Table 8: External Loop Filter Component Values M2004-01/-11

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 9: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings ard stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature					
		Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 10: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			162		mA	
LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_CLK0, REF_CLK1, REF_SEL, MR, nP_LOAD, S_LOAD, S_CLOCK, S_DATA, N0:N1, M0:M5	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		1.3	V	
Inputs with Pull-down	I_{IH}	Input High Current	REF_CLK0, REF_CLK1, REF_SEL, MR, nP_LOAD, S_LOAD, S_CLOCK, S_DATA, N0:N1, M0:M4			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	M5			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			µA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Outputs	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	

Note 1: Single-ended measurement. See Figure 6, Output Rise and Fall Time on pg. 9.

Table 11: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	REF_CLK0, REF_CLK1	1		175	MHz	
			S_CLOCK			50	MHz	
	F_{OUT}	Output Frequency	FOUT, nFOUT	38		700	MHz	
	APR	VCSO Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor			16		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.5		ps	
			50kHz to 80MHz		0.5		ps	
	odc	Output Duty Cycle [2]	N = 2, 4, or 8	45	50	55	%	
			N = 1	40	50	60	%	
	t_R	Output Rise Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_F	Output Fall Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_{SETUP}	Setup Time [3]	M5:0, N1:0 to nP_LOAD	5			ns	
			S_DATA to S_CLOCK					
	t_{HOLD}	Hold Time [3]	M5:0, N1:0 to nP_LOAD	5			ns	
			S_DATA to S_CLOCK					
			S_CLOCK to S_LOAD					
	t_{IPW}	Input Pulse Width [4]	S_LOAD	10			ns	
	t_{LOCK}	PLL Lock Time				100	ms	
	MTIE	Mean Time Interval Error [5]	M2004-11		Compliant with GR-253-CORE			

Table 12: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 8, External Loop Filter Component Values M2004-01/-11 on pg. 6.
Note 2: See Parameter Measurement Information on pg. 9.
Note 3: See Figure 8, Times for M5:0 and N1:0 and Figure 9, Times for S_DATA on pg. 9.
Note 4: See Figure 9, Times for S_DATA on pg. 9.
Note 5: Requires proper loop filter settings. Consult factory.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

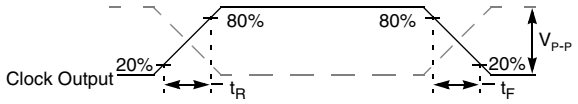


Figure 6: Output Rise and Fall Time

Output Duty Cycle

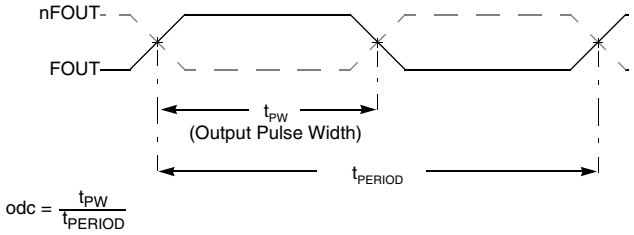


Figure 7: Output Duty Cycle

Times for M5:0 and N1:0

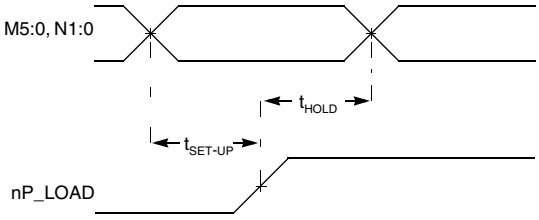


Figure 8: Times for M5:0 and N1:0

Times for S_DATA

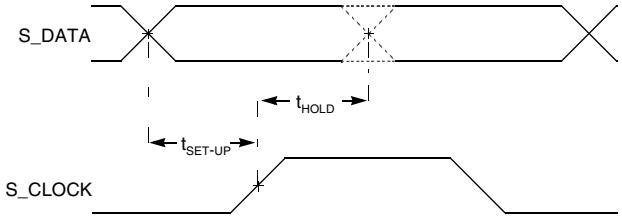


Figure 9: Times for S_DATA

Times for S_CLOCK and S_LOAD

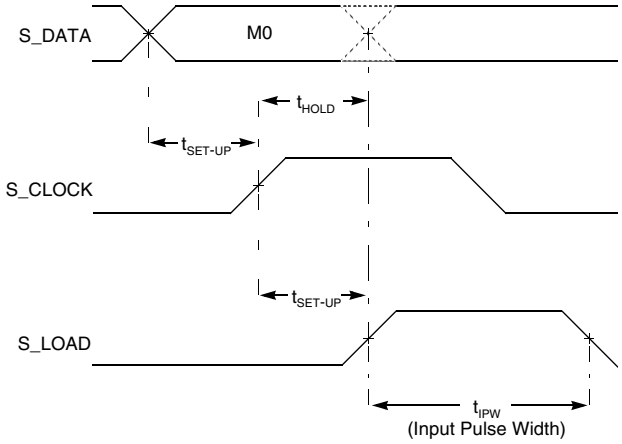


Figure 10: Times for S_CLOCK and S_LOAD

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

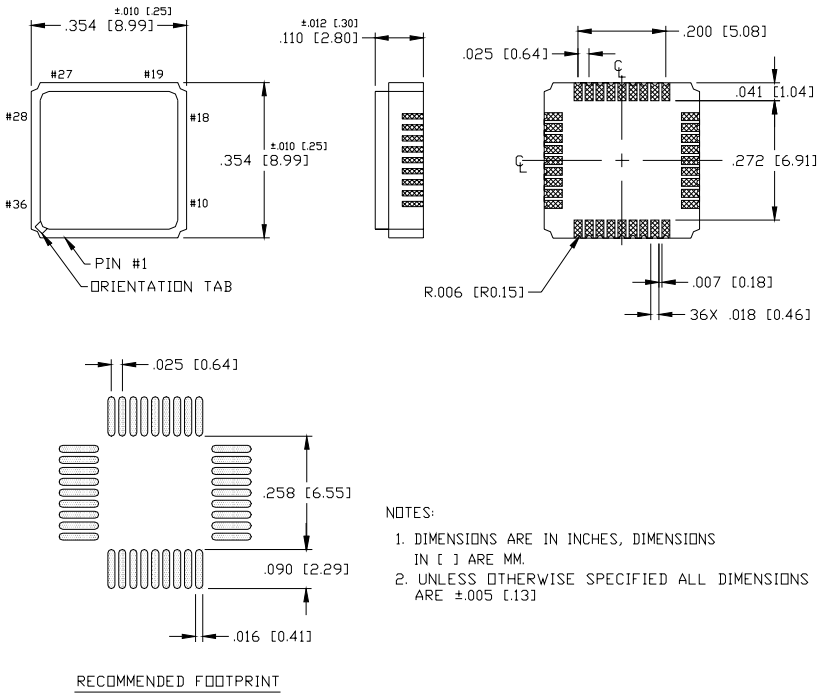


Figure 11: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

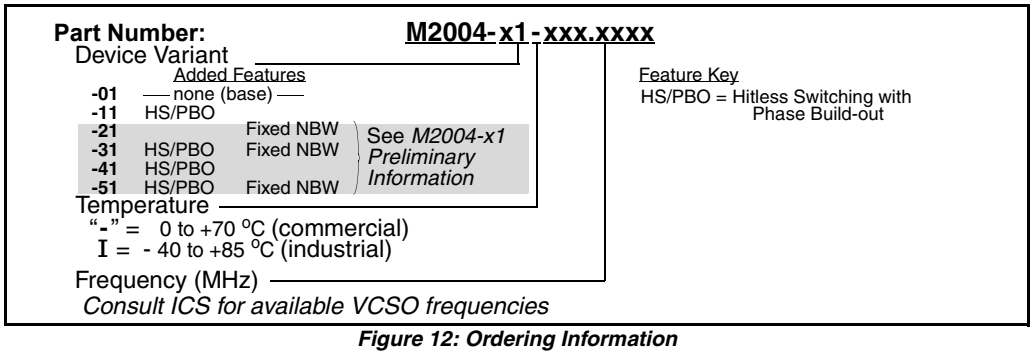


Figure 12: Ordering Information

Example Part Numbers

For VCSO Freq (MHz)	Temperature	Part Number
622.08	commercial	**M2004-01-622.0800** or **M2004-11-622.0800**
	industrial	**M2004-01I622.0800** or **M2004-11I622.0800**

Table 13: Example Part Numbers

Consult ICS for the availability of other VCSO frequencies.