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M21245-15

3G/HD/SD-SDI Multi-rate Reclocker

Rev V6

Applications

- 3G/HD/SD-SDI Video Switchers
- 3G/HD/SD-SDI Video Routers
- 3G/HD/SD-SDI Video Distribution Amplifiers
- DVB-ASI Equipment

Features

- SMPTE 259-C, 292, 424M, and DVB ASI Compliant
- Greater than 0.6 UI Input Jitter Tolerance
- Integrated 50 Ω input termination
- Input equalization and output de-emphasis for 40" of FR4 trace
- 230 mW power consumption (1.2 V operation)
- Integrated regulators for multi-voltage operation (1.2 V - 3.3 V)
- Electrically independent input, output, and core supply rails
- Output enable/disable and configurable auto or manual bypass mode
- Automatic and manual modes for rate indication and selection
- Loss of Lock (LOL), Loss of Signal (LOS) and data rate Indication
- Two-wire and four-wire serial interface programmability
- Industrial operating temperature range (-40 °C to +85 °C)
- Optional recovered serial clock output

The M21245 is a serial digital video reclocker with integrated trace equalization and automatic rate detect (ARD) circuitry. It operates at SDI data rates ranging from 270 Mbps to 2970 Mbps and is compliant to SMPTE 424M, SMPTE 292, and SMPTE 259M-C. At 270 Mbps it also supports DVB-ASI.

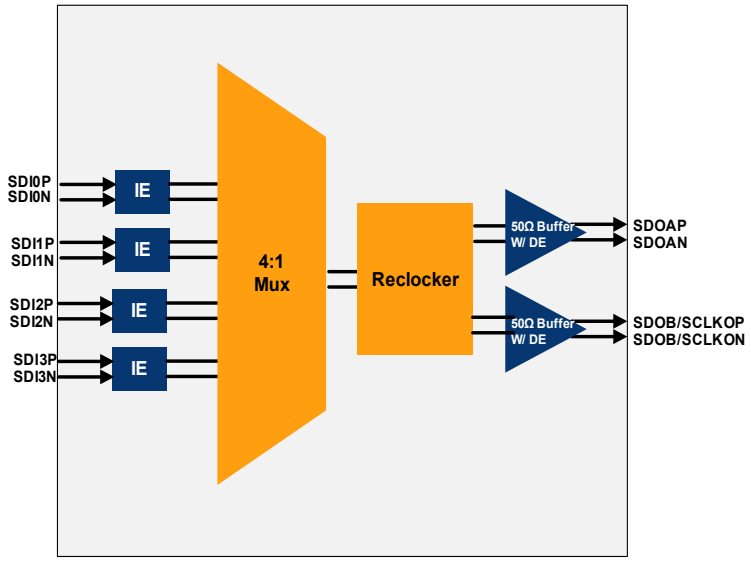
The M21245 has an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial outputs with very low output jitter. The reclocker requires a single external 27 MHz crystal, which is used as the reference clock for all four channels. It includes per-lane analog input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

This device features integrated supply regulators allowing it to be powered from 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.2 V, it consumes only 230 mW at 3G-SDI. Furthermore, the power rails for the core, input, and output circuitry are electrically independent and as such may be connected to different voltage rails on the board. This feature allows the M21245 to be DC-coupled to any upstream or downstream device regardless of its input/output voltage level.

The device may be configured by setting the internal registers though standard two-wire and four-wire interfaces.

The M21245 is offered in a green and RoHS compliant, 6 mm x 6 mm, 40-pin QFN package.

M21245 Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M21245G-15*	6x6 mm, 40-pin QFN package	-40 °C to 85 °C

* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

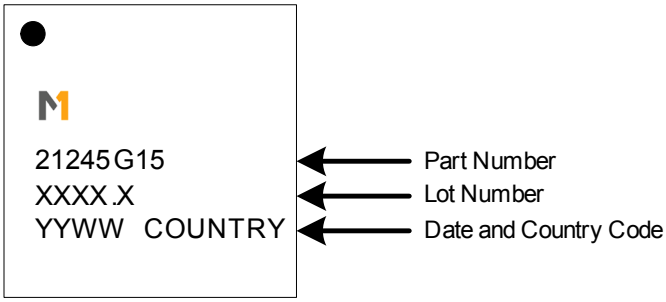
Revision History

Revision	Level	Date	Description
V6	Released	December 2015	Updated package drawing, Figure 3-12. Package effective as of July 2014. Added package dimensions, Figure 3-13.
H (V5)	Released	July 2012	Section 4.6.2: Revised four-wire interface description.
G (V4)	Released	January 2012	Table 1-8: Added 2-state input to V_{IH} and V_{IL}. Section 4.9: Advised using a 10 kΩ pull-up to DV_{DDIO} when in "interrupt mode."
F (V3)	Released	January 2011	In the previous revision of this device, M21245G-14, the Loss of Lock (LOL) alarm would be erroneously triggered when pathological signals were used. As a workaround, MACOM recommended masking the faulty LOL alarm by setting register 96h bit[6] to 1b. In the latest version, M21245G-15, the faulty algorithm has been corrected. Therefore, the requirement to mask the LOL alarm has been removed from this data sheet. Please note that this change has been made to be fully backwards compatible, so setting register 96h bit[6] to 1b, while unnecessary, will not affect the function or performance of the device. Ordering Information: Updated part number from -14 to 15. Table 1-7: Updated XTAL and reference clock electrical specifications, input Impedance typical from to 400 kΩ to 200 Ω i input amplitude range from 1.6 V-2.0 V to 0.8 V to 1.2 V and max rise/fall times from 1 ns max to 2 ns typical and 6 ns max. Table 1-8: Updated V_{OH} from 0.75 to 0.80 x DV_{DDIO} and I_{OL} from 24 mA to 3 mA. Figure 3-1: Updated the pinout diagram to reflect new pin naming convention. Table 3-1: Updated table to reflect new pin naming convention. Figure 3-6: Updated figure from pull-down to pull-up. Table 5-1: Updated register map table. Added all registers needed to perform EEPROM checksum. Register 0Ah: Added this register to provide programmability to SDOB De-emphasis. Register 0Eh: De-featured xAlarm status mode. Register 0Eh: Modified Interrupt mode xAlarm pulse widths to reflect their true value with respect to a 10K Ω pull up resistor. Register 82h: Updated chip version from 03h to 04h. Figure 4-3: Updated self bias diagram to reflect conditions necessary for self biased mode. Section 4.6.2: Updated to include the detailed timing description for four-wire interface when conducting a write operation followed by a read operation. Table 4-6: Updated the EEPROM Addresses. Table 4-7: Updated the EEPROM Addresses. Section 4.7.1: Clock Recovery: Updated the data to clock delay to 60 ps. Section 4.2: Included conditions necessary for self biased mode. Section 4.6.1: Added note defeaturing xAlaram pin in hardware control mode. Section 4.9: De-featured xAlarm pin in hardware mode and limited xAlarm pin usage to Interrupt Mode only.

Revision History

Revision	Level	Date	Description
E (V2)	Released	August 2010	Status for floating logic state for pin MF4 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Status for floating logic state for pin MF5 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Changed MF4 and MF5 levels in Table 3-1. Added note to Figure 4-3. Changed MF4 and MF5 levels in Table 4-2. Changed MF3 function description in Table 4-5.
D (V1)	Released	May 2010	Refer to D revision for details.
C (V1P)	Preliminary	April 2010	Refer to C revision for details.
B (V2A)	Advance	October 2009	Refer to B revision for details.
A (V1A)	Advance	September 2008	Initial release.

M21245 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with DV_{DDO} = 1.2 V, AV_{DDCORE} = 1.2 V, DV_{DDCORE} = 1.2 V, AV_{DDI} = 1.2 V, CML inputs/outputs at 800 mV differential (R_{LOAD} = 50 Ω), and PRBS 2^{10} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	1, 3	-0.5	3.6	V
AV_{DDO}	Analog supply for output circuitry	1, 3	-0.5	3.6	V
DV_{DDIO}	Digital supply for input/output circuitry	1, 3	-0.5	3.6	V
DV_{DDCORE}	Digital core positive supply	1, 3	-0.5	1.5	V
AV_{DDCORE}	Analog core positive supply	1, 3	-0.5	1.5	V
T_{STORE}	Storage temperature	1, 3	-65	150	°C
$V_{IN, CMOS}$	DC input voltage (CMOS)	1, 3	-0.5	DV_{DDIO}+0.5	V
V_{IN}	DC input voltage (PCML)	1, 3	-0.5	AV_{DDI}+0.5	V
$V_{ESD, HBM}$	Human Body Model (HBM)	1, 2, 3	-2	2	kV
$V_{ESD, CDM}$	Charge Device Model (CDM)	1, 2, 3	-500	500	V
LU	Latch up @ 85 °C	1, 3	-150	150	mA
$I_{IN, PCML}$	Maximum high-speed input current	1, 3	-100	100	mA

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV_{DDIO}	Digital I/O positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDI}	Analog input positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDO}	Analog output positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDCORE}	Analog core positive supply	—	1.14	1.2	1.26	V
DV_{DDCORE}	Digital core positive supply	—	1.14	1.2	1.26	V
T_{CASE}	Case temperature	—	-40	25	+85	°C

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Typical	Maximum	Unit
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 1	1, 3	230	290	mW
			1, 4	250	350	
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 2	1, 3	240	300	mW
			1, 4	260	360	
P_{TOTAL}	Total power consumption	DV_{DDCORE} = AV_{DDCORE}= 1.2 V AV_{DDI} = DV_{DDIO} = 1.2 V AV_{DDO} = 1.8 V SDO Swing Level 3	1, 3	260	370	mW
			1, 4	270	450	
		DV_{DDCORE} = AV_{DDCORE}= 1.2 V AV_{DDI} = DV_{DDIO} = 3.3 V AV_{DDO} = 3.3 V SDO Swing Level 3	2, 3	720	1070	
θ_{JA}	Junction to ambient thermal resistance		5	35	—	°C/W
θ_{JC}	Junction to case thermal resistance		5	3	—	°C/W

NOTE:

1. Internal regulators disabled.
2. Internal regulators enabled.
3. SDOB/SCLK disabled.
4. SDOB/SCLK enabled.
5. Airflow = 0 m/s.

Table 1-4. SDI High Speed (Positive Current Mode Logic) Input Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDI input data rate	SD Operation (SMPTE 259M,C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	Mbps
		3G Operation (SMPTE 424M)		—	2970, 2967	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
V_{IN}	Differential input voltage	At the chip input (point blank) Input equalization disabled LOS enabled (default setting)	1, 3	300	800	1600	mV_{PPD}
V_{ICM}	Input common mode voltage	At the chip input (point blank) Input equalization disabled LOS enabled		AV_{DDI}-0.6	—	AV_{DDI}+0.1	V
R_{IN}	Input termination to AV_{DDI}			40	50	60	Ω
IE	Input equalization		2	—	0, 2, 4, 6	—	dB

NOTE:

1. For example: 1200 mV_{PP} differential = 600 mV_{PP} for each single-ended terminal.
2. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
3. When using long traces and input equalization enabled, MACOM recommends a minimum input swing of 400 mV_{PPD}. With pathological patterns, DC-coupling produces the best results.

Table 1-5. SDO High Speed (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDO output data rate	SD operation (SMPTE 259M,C)		—	270	—	Mbps
		HD operation (SMPTE 292)		—	1485, 1483.5	—	
		3G operation (SMPTE 424M)		—	2970, 2967	—	
		Reclocker bypassed		18	—	3400	
F_{CLOCK}	Serial clock output frequency	SD operation (SMPTE 259M,C)	1, 7	—	270	—	MHz
		HD operation (SMPTE 292)		—	1485, 1483.5	—	
		3G operation (SMPTE 424M)		—	2970, 2967	—	
V_{OUT}	Differential output swing (peak to peak, differential)	Swing level 1	2	470	600	720	mV_{PPD}
		Swing level 2	2	600	800	970	
		Swing level 3	2,3	960	1200	1500	
V_{OCM}	Output common mode voltage	DC-coupled	2, 6	—	AV_{DDO}-V_{OUT}/4	—	
t_R/t_F	SDO output rise/fall time	From 20%-80% of the swing for all levels		—	85	130	ps
$t_R/t_{F\ DIFF}$	Rise/Fall time mismatch	From 20%-80% of the swing for all levels	6	—	—	30	ps
DCD_{DATA}	Output duty cycle distortion	For all data rates	4	—	—	15	ps
R_{OUT}	Output termination to AV_{DDO}			40	50	60	Ω
DE	Output de-emphasis		5	—	0, 2, 4, 6	—	dB

NOTE:

1. Serial clock output enabled.
2. Differential swing is maximum output level (de-emphasis is disabled or maximum level when de-emphasis is enabled), maximmum level includes overshoot.
3. 1200 mV swing level requires AV_{DDO} to be 1.8 V or higher.
4. Measured in reclocked mode.
5. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
6. Guaranteed by design.
7. See Section 4.7 for information on clock data alignment.

Table 1-6. Reclocker Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
t_{LOCK}	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBW, PEAK}$	Loop bandwidth peaking	—	1	—	0.1	—	dB
F_{LBW}	Loop bandwidth (nominal setting)	3G operation (2.97 Gbps)	1	—	1.7	—	MHz
		HD operation (1.485 Gbps)	1	—	0.85	—	
		SD operation (270 Mbps)	1	—	0.17	—	
J_{TOL}	Input jitter tolerance	3G, HD, and SD operation	2	> 0.6	—	—	UI p-p
J_{GEN}	Total output jitter	3G operation (2.97 Gbps)	2, 3	—	0.07	0.11	UI p-p
		HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

NOTE:

1. 0.2 UI input jitter applied at SDI input.
2. Measured with $PRBS2^{10}$-1.
3. Input jitter = 20 ps p-p.

Table 1-7. XTALP/N and Reference Clock Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
F_{REF}	XTAL/Ref clock frequency	3	—	27	—	MHz
$F_{REF, ppm}$	XTAL/Ref clock frequency accuracy	—	-100	0	100	ppm
C_{LOAD}	XTAL load capacitance	1	—	20	—	pF
$CLOCK_{JITT}$	Jitter (RMS)	2, 4	—	—	1	ps
$CLOCK_{DCT}$	Reference clock duty cycle tolerance	2	40	—	60	%
R_{IN}	Input impedance	2, 5	200	750	1500	Ω
V_{IN}	Input amplitude	2	0.8	—	1.2	V
t_R/t_F	Rise/Fall time	2, 6	—	2	6	ns

NOTE:

1. This capacitance is supplied internally (no external cap is required).
2. When using an external reference clock source, this should be AC-coupled through a 0.1 µF capacitor.
3. When using an external clock a small increase in jitter may be seen. For best performance a crystal is recommended.
4. Jitter bandwidth is from 12 kHz to 20 MHz.
5. Measured with TDR module.
6. 10% to 90% rise and fall times.

Table 1-8. Digital Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Output Logic High	1	0.80 x DV_{DDIO}	DV_{DDIO}	—	V
V_{OL}	Output Logic Low	2	—	—	0.2 x DV_{DDIO}	V
V_{IH}	Input Logic High	3, 5	0.85 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IF}	Input Logic Floating	3, 5	0.25 x DV_{DDIO}	—	0.75 x DV_{DDIO}	V
V_{IL}	Input Logic Low	3, 5	0	—	0.15 x DV_{DDIO}	V
V_{IH}	Input Logic High	4, 5	0.75 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IL}	Input Logic Low	4, 5	0	—	0.25 x DV_{DDIO}	V

NOTE:

1. I_{OH} = -3 mA
2. I_{OL} = 3 mA
3. 3- state input
4. 2- state input
5. Some inputs can be 2 or 3 state. Depending on which mode is selected the threshold levels will change accordingly.

2.0 Typical Performance Characteristics

Figure 2-1. Eye Diagram at Reclocker Input PRBS15 @ 3 Gbps

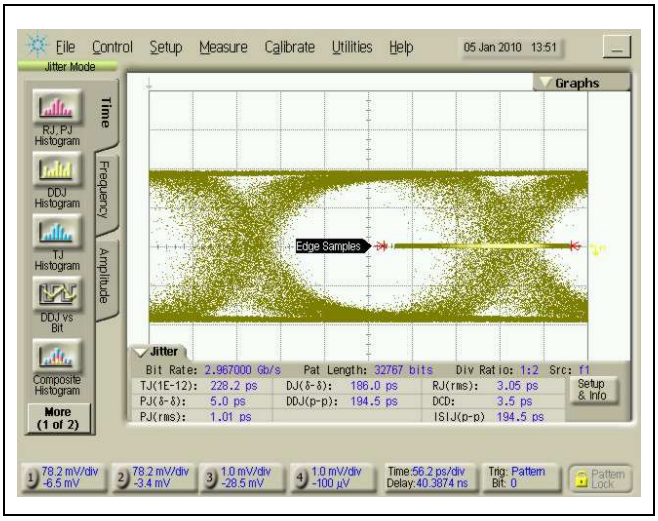
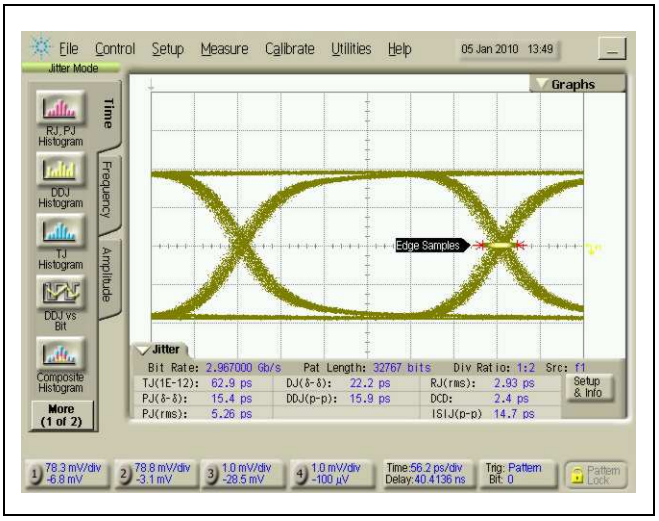


Figure 2-2. Eye Diagram at Reclocker Output PRBS15 @ 3 Gbps



3.0 Pinout Diagram, Pin Description, and Package Drawing

Figure 3-1. M21245 Pinout Diagram

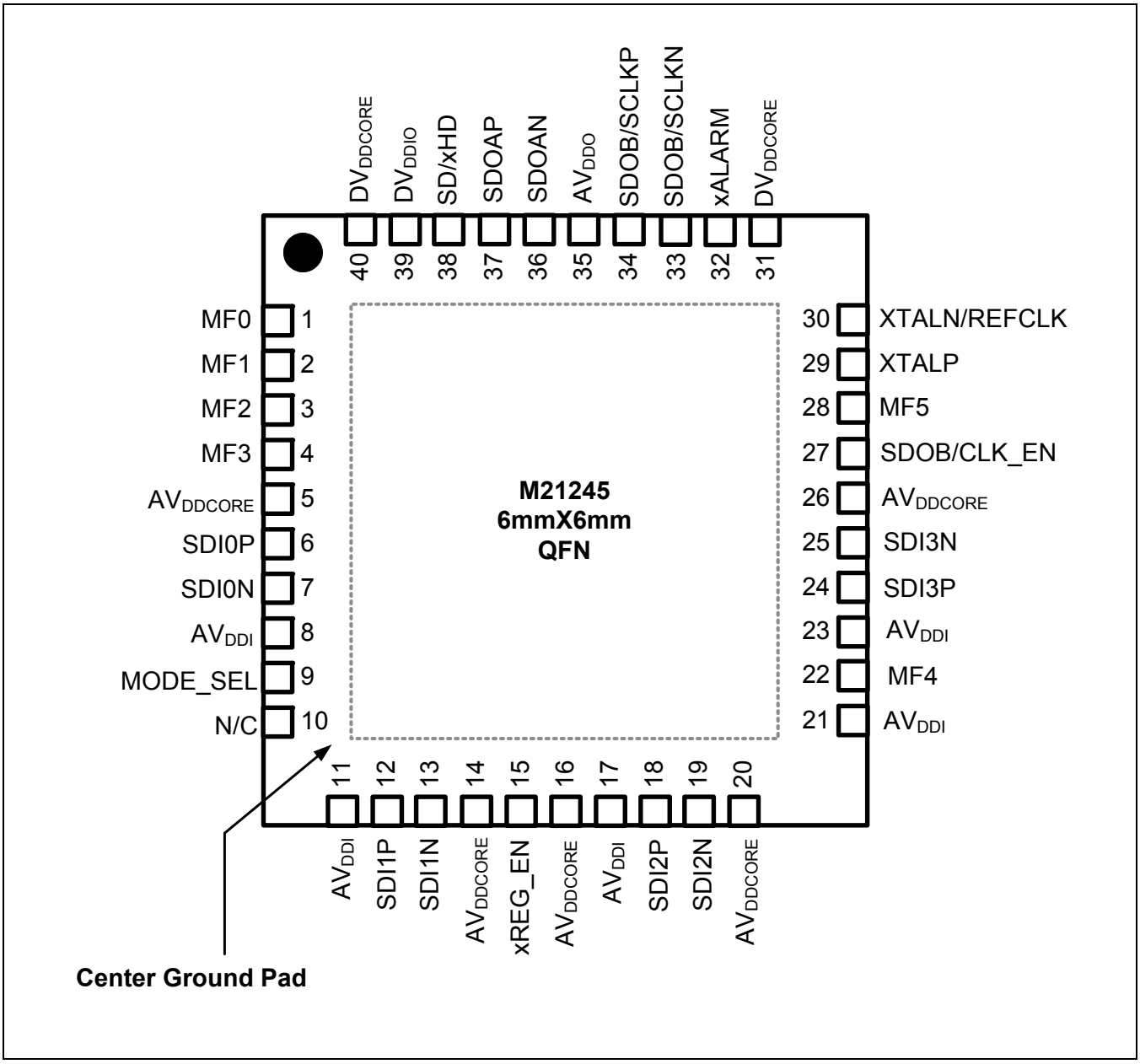


Table 3-1. M21245 Pin Description

Pin Name	Pin Number(s)	Type	Description
AV_{DDCORE}	5, 14, 16, 20, 26	Power	Analog positive supply
AV_{DDI}	8, 11, 17, 21, 23	Power	Analog positive supply
AV_{DDO}	35	Power	Analog positive supply
DV_{DDCORE}	31, 40	Power	Digital core positive supply
DV_{DDIO}	39	Power	Digital core positive supply
AV_{SS}	Center Ground Pad	Power	Ground
SDI0P, SDI0N	6, 7	PCML input	Data input lane 0; true/complement
SDI1P, SDI1N	12, 13	PCML input	Data input lane 1; true/complement
SDI2P, SDI2N	18, 19	PCML input	Data input lane 2; true/complement
SDI3P, SDI3N	24, 25	PCML input	Data input lane 3; true/complement
SDOAP, SDOAN	37, 36	PCML output	Data output lane A; true/complement
SDOBP/SCLKP, SDOBN/SCLKN	34, 33	PCML output	Data output lane B; true/complement
XTALP	29	Reference Clock	27 MHz reference XTAL connection
XTALN/REFCLK	30	Reference Clock	27 MHz reference XTAL connection or 27 MHz reference clock input
MODE_SEL	9	CMOS Control Input	Sets the device control/configuration mode: L = Device is in register access mode with two-wire serial control (SIC2) F = Device is in hardware control mode (Hardware mode is not recommended) H = Device is in register access mode with four-wire serial control (SIC4) Termination - F
SDOB/SCLK_EN	27	CMOS Control Input	SDOB/SCLK output enable: L = SDOB/SCLK output disabled F = Serial data output enabled H = Serial clock output enabled Termination - L, 100 kΩ pull down to AVSS
xREG_EN	15	CMOS Control Input	Regulator enable control, as in Figure 3-6, but pull up resistor is to AV_{DDI}. L = Integrated regulators enabled H = Integrated regulators disabled Termination - H, 100 kΩ pull up to AV_{DDI}
SD/xHD	38	CMOS Output	CMOS SD/xHD rate indicator: L = HD/3G Data rate H = SD Rate

Table 3-1. M21245 Pin Description

Pin Name	Pin Number(s)	Type	Description
xALARM	32	Output (Open Drain)	Alarm indicator for all channels (Logical OR of all individual channel alarms). Termination - Open L = Alarm asserted H = Normal operation Serial control mode (two-wire/four-wire): xALARM in interrupt mode Hardware mode: Not supported
MF0	1	CMOS Control Input	Four-wire serial control mode: Serial clock input (SCLK) Two-wire serial control mode: Clock input from master host (SCL) Hardware mode: Unused
MF1	2	CMOS Control Input	Four-wire serial control mode: Serial data output (SO) Two-wire serial control mode: Serial data I/O (SDA) Hardware mode: Unused
MF2	3	CMOS Control Input	Four-wire serial control mode: Serial data in (SI) Two-wire serial control mode: Address bit 0 (ADD0) Hardware mode: Input trace equalization control for all SDI inputs (IE_CTRL) H = Large Input EQ F = Medium Input EQ L = Input EQ disabled
MF3	4	CMOS Control Input	Four-wire serial control mode: Active low chip select (xCS) Two-wire serial control mode: Address bit 1 (ADD1) Hardware mode: Output de-emphasis (DE) control for SDO outputs (DE_CTRL) H = Large Output DE F = Medium Output DE L = DE disabled
MF4	22	CMOS Control Input	Four-wire serial control mode: Not used. Tie to DV_{DDIO} or leave floating Two-wire serial control mode: Address bit 2 (ADD2) Hardware mode: Reclocker bypass control (RC_BYPASS) L/F = Normal operation, reclocker not bypassed H = Reclocker bypassed
MF5	28	CMOS Control Input	Four-wire serial control mode: Not used. Tie to AVSS or leave floating Two-wire serial control mode: Address bit 3 (ADD3) Hardware mode: SDO disable control for all outputs (SDO_DIS) H = SDO disabled output logic high L/F = SDO enabled
NC	10	Reserved	Do not connect

Figure 3-2. I-Analog

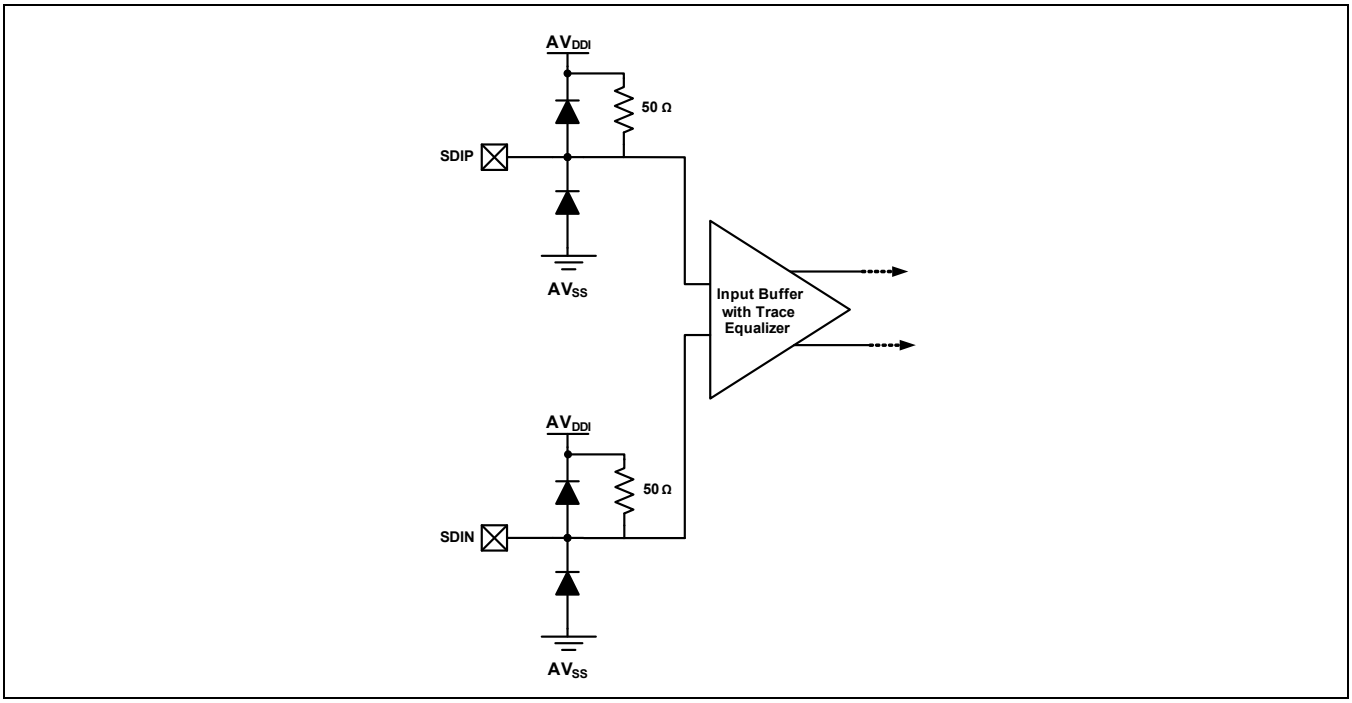


Figure 3-3. O-Analog

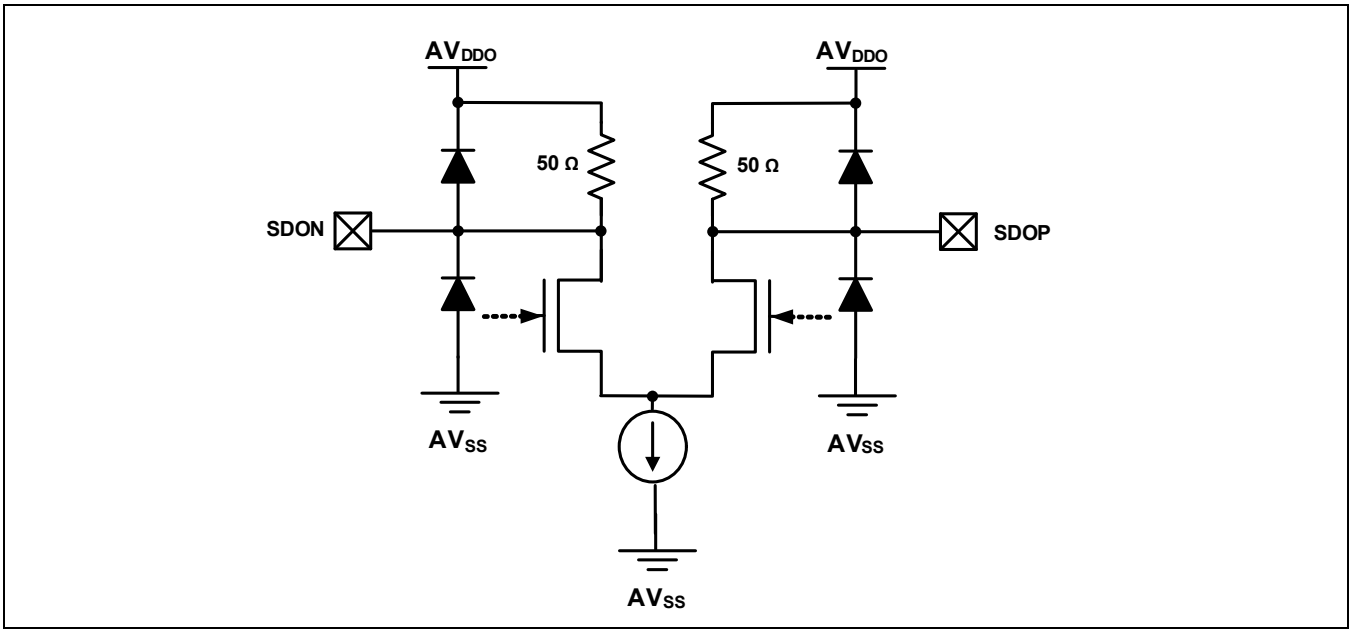


Figure 3-4. Ref Clock

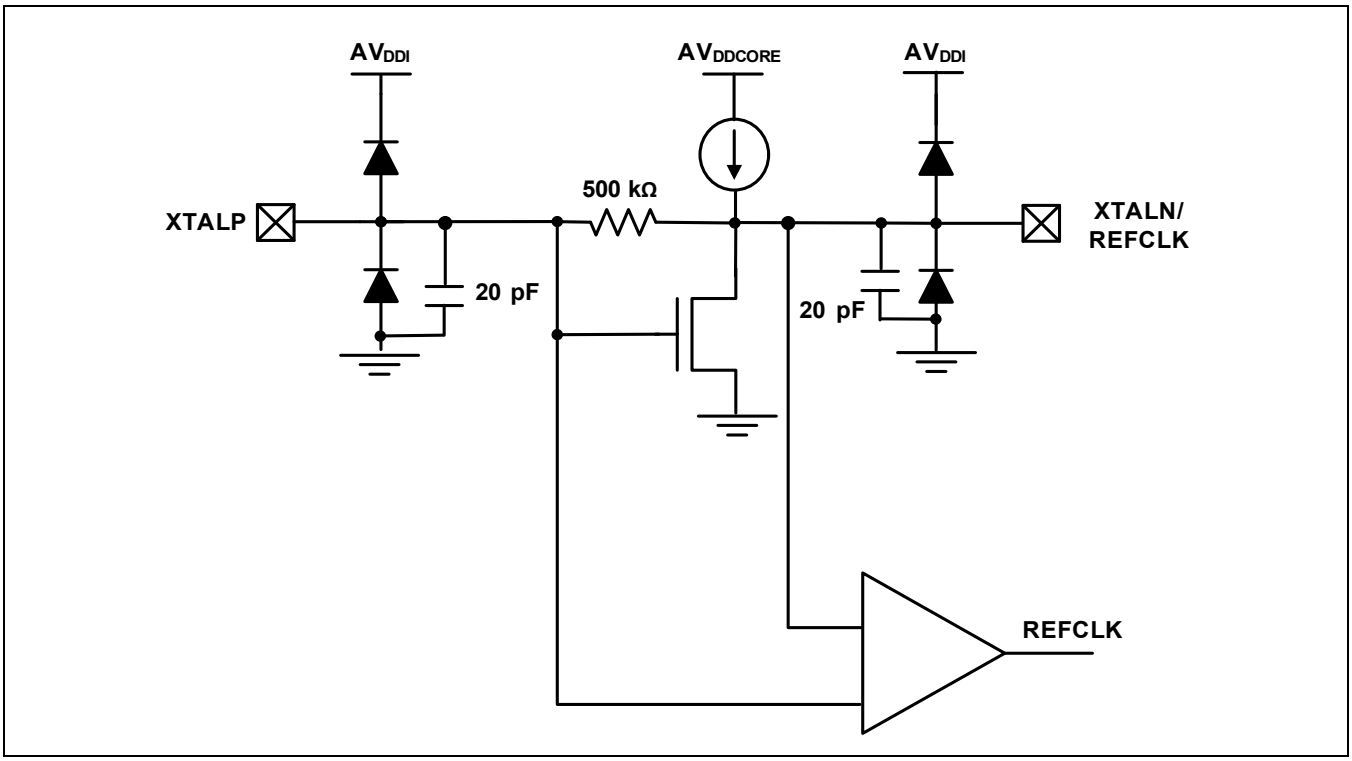


Figure 3-5. I-Digital With No Pull-up

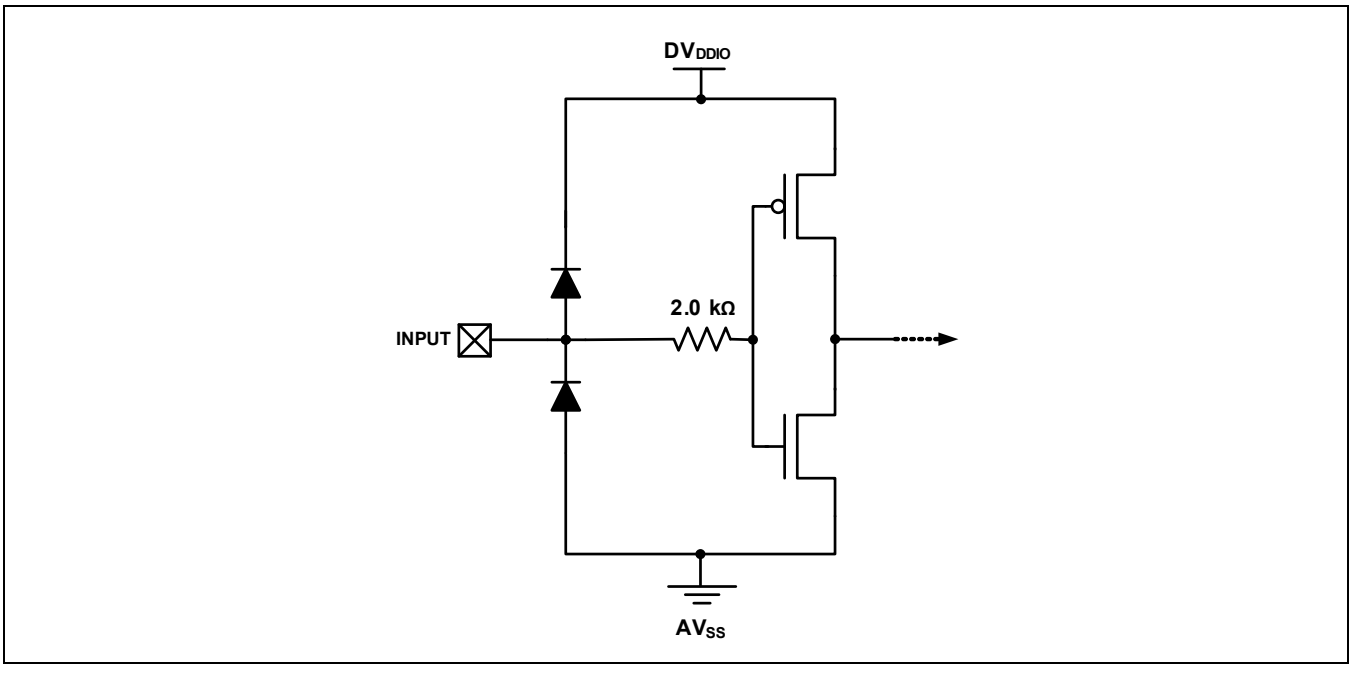


Figure 3-6. I-Digital With Pull-up

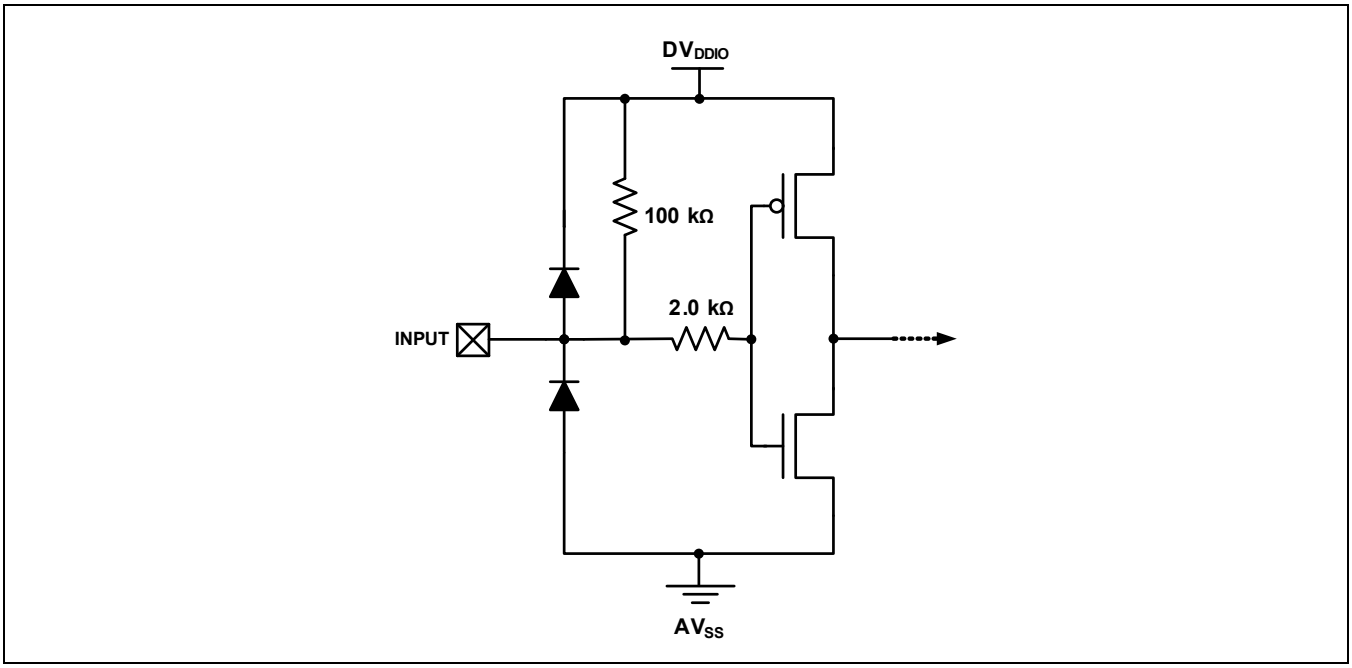


Figure 3-7. I-Digital With Pull-down

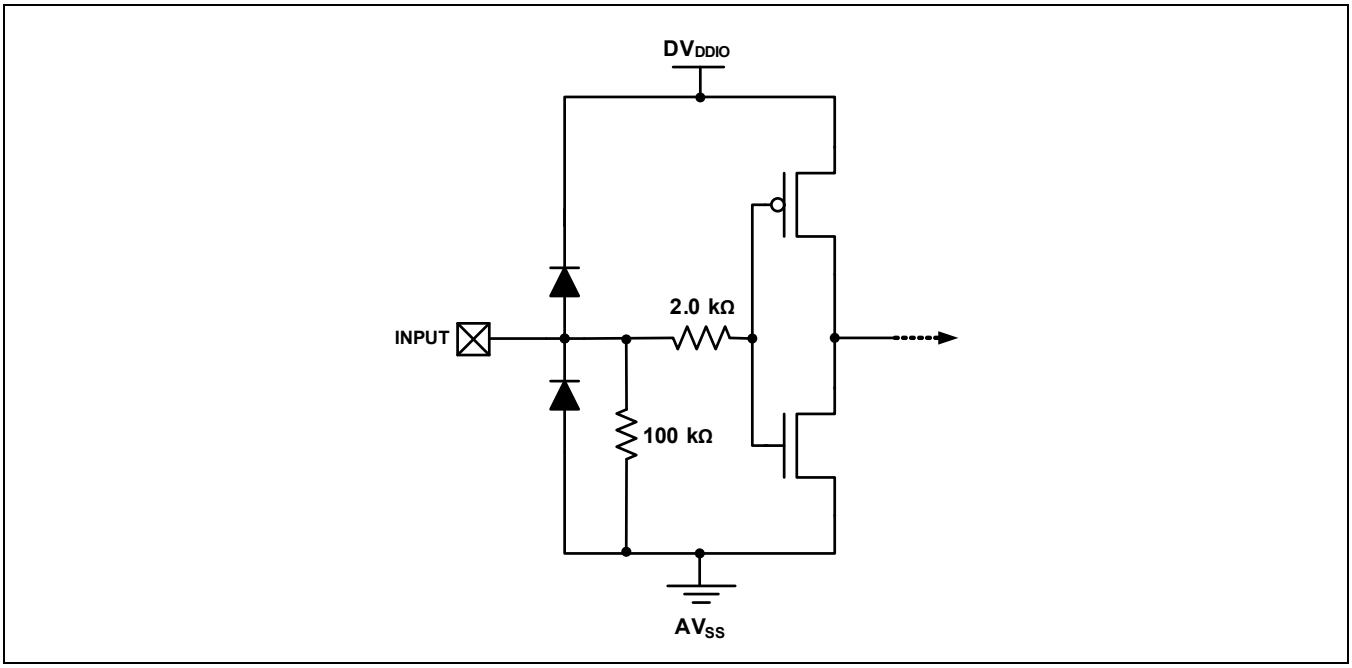


Figure 3-8. 3-State/I-Digital

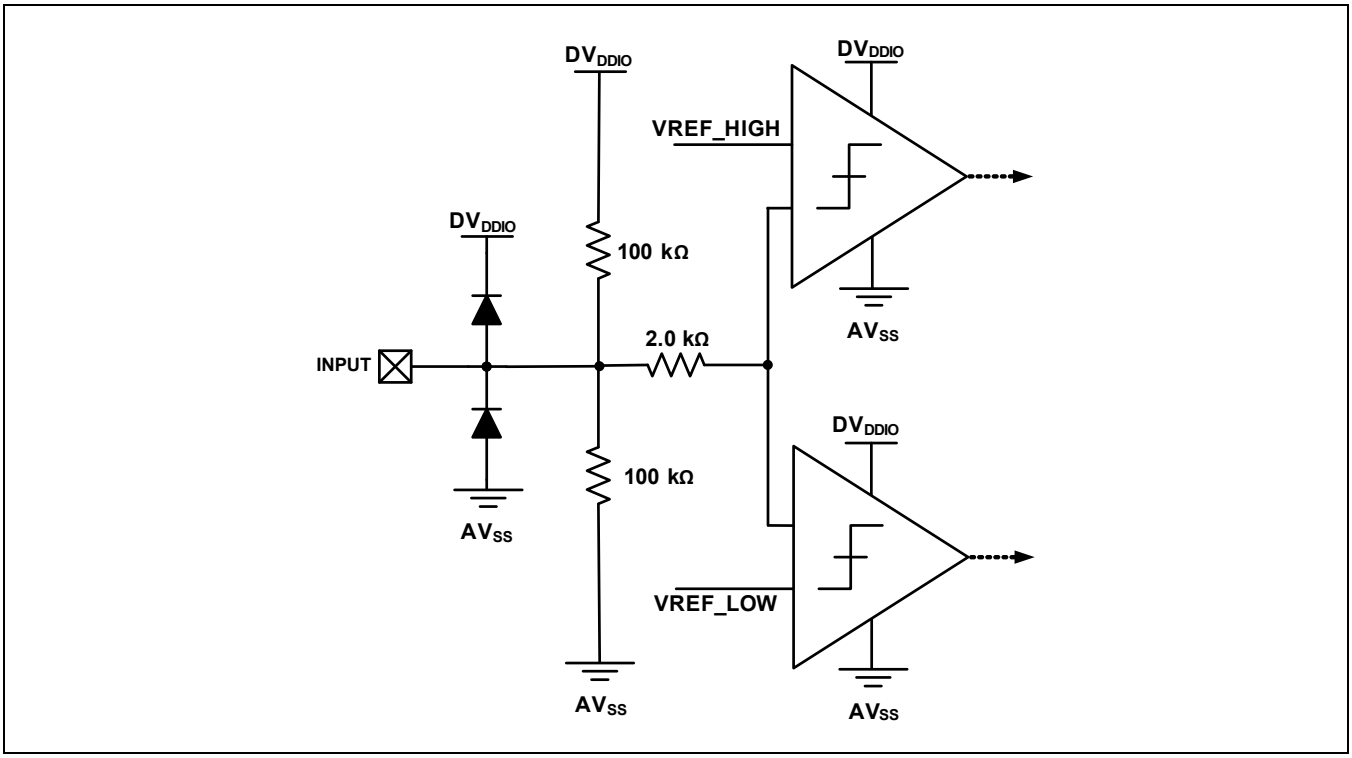


Figure 3-9. O-Digital

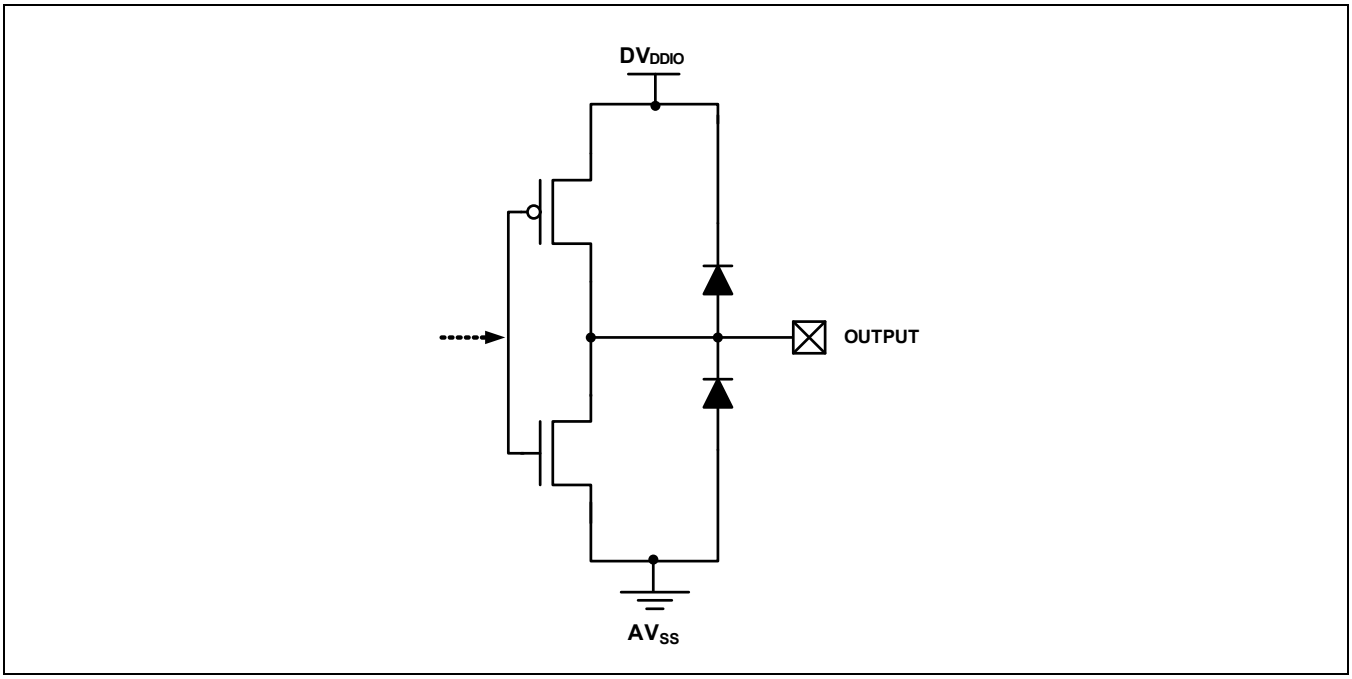
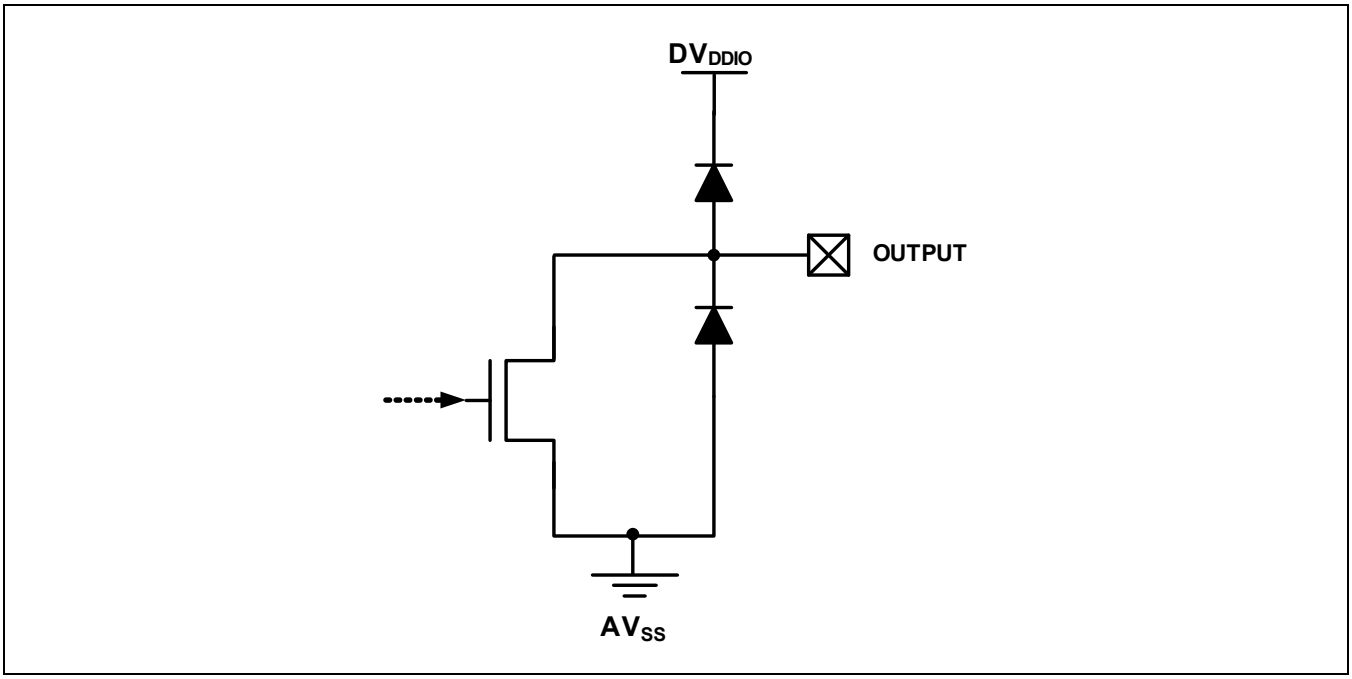


Figure 3-10. O-Open Drain



The M21245 is assembled in a 40-pin, 6 mm x 6 mm Quad Flat No-Lead (QFN) package. The exposed die paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the QFN package is shown below.

Figure 3-11. QFN Package Cross Section

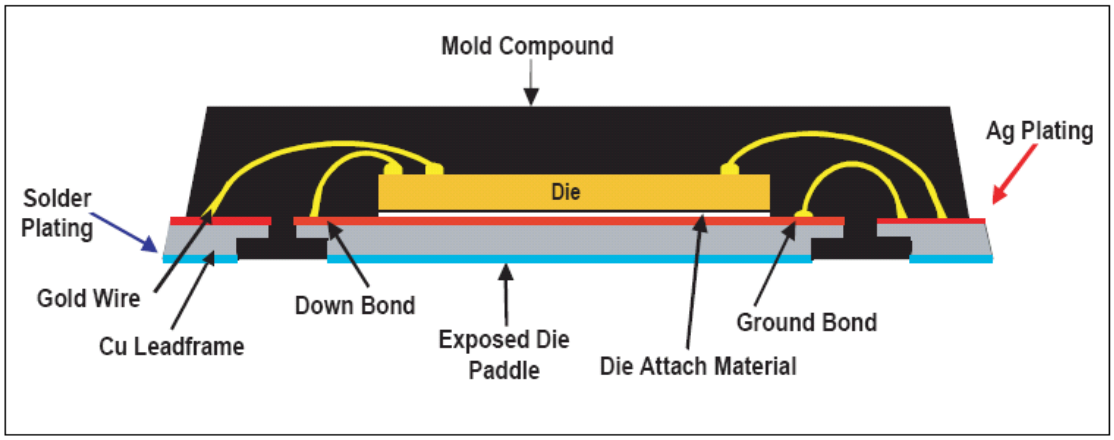
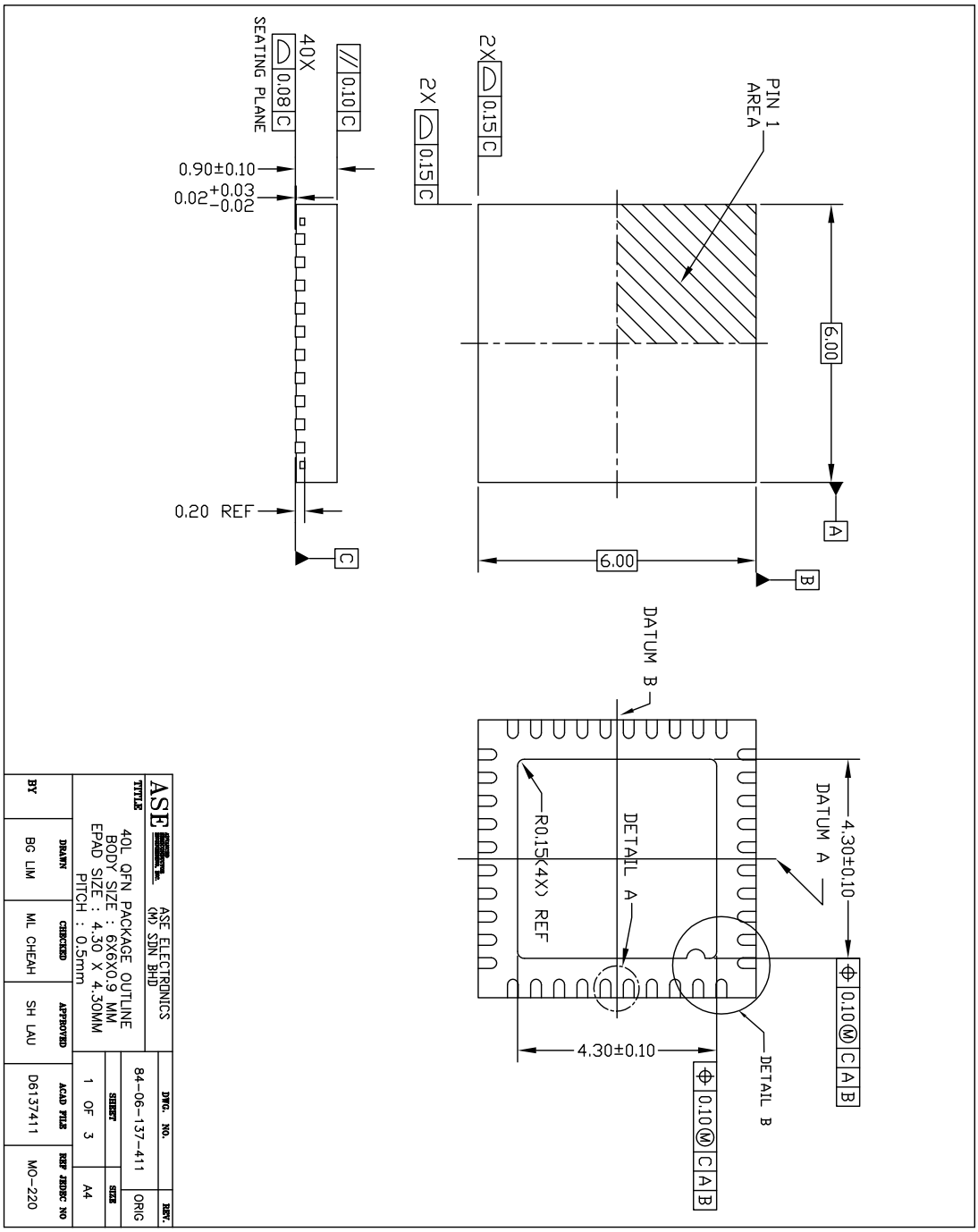
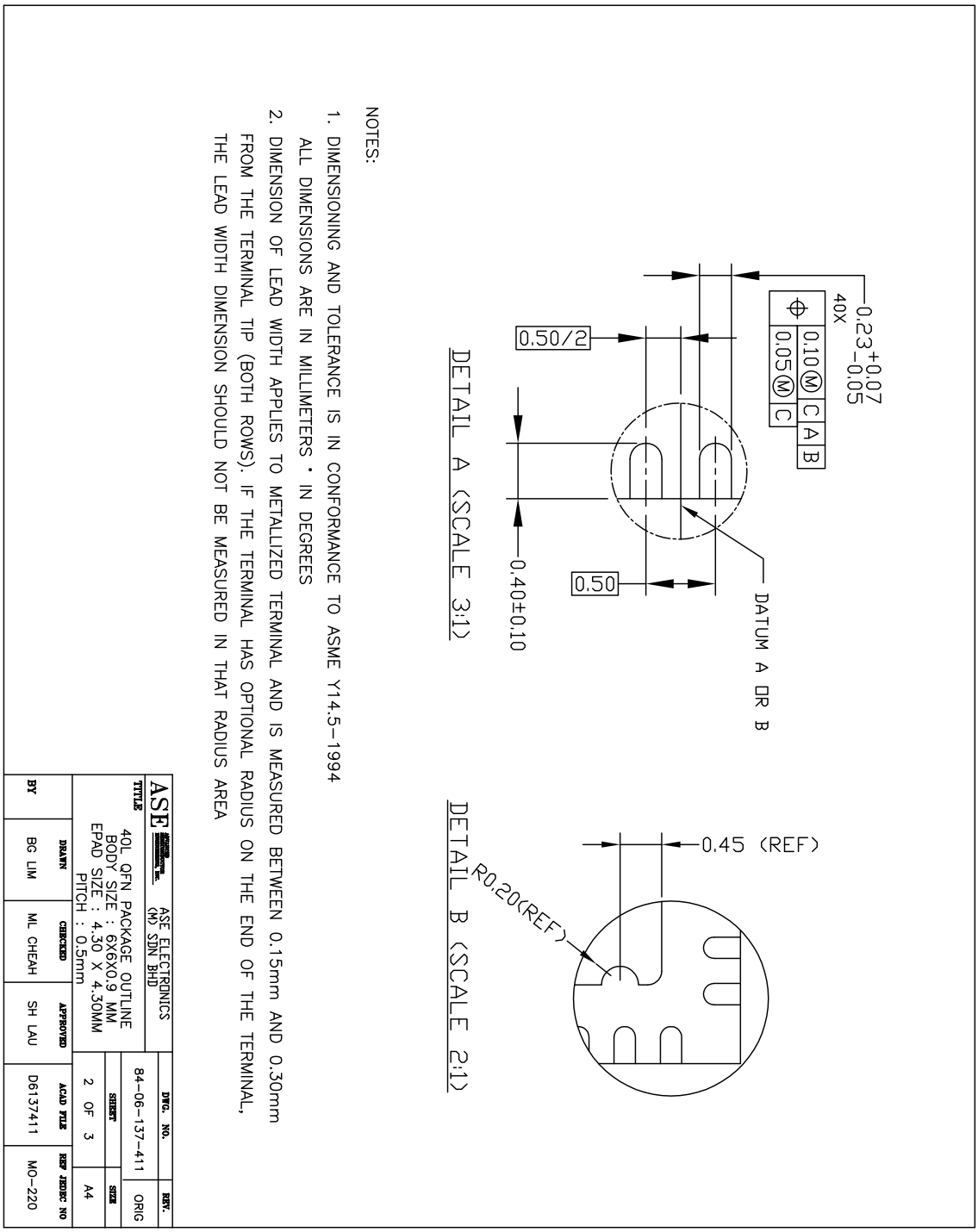


Figure 3-12. Package Outline Drawing



1. New ASE package and the old Amkor package have the same footprint dimensions.

Figure 3-13. Package Dimensions



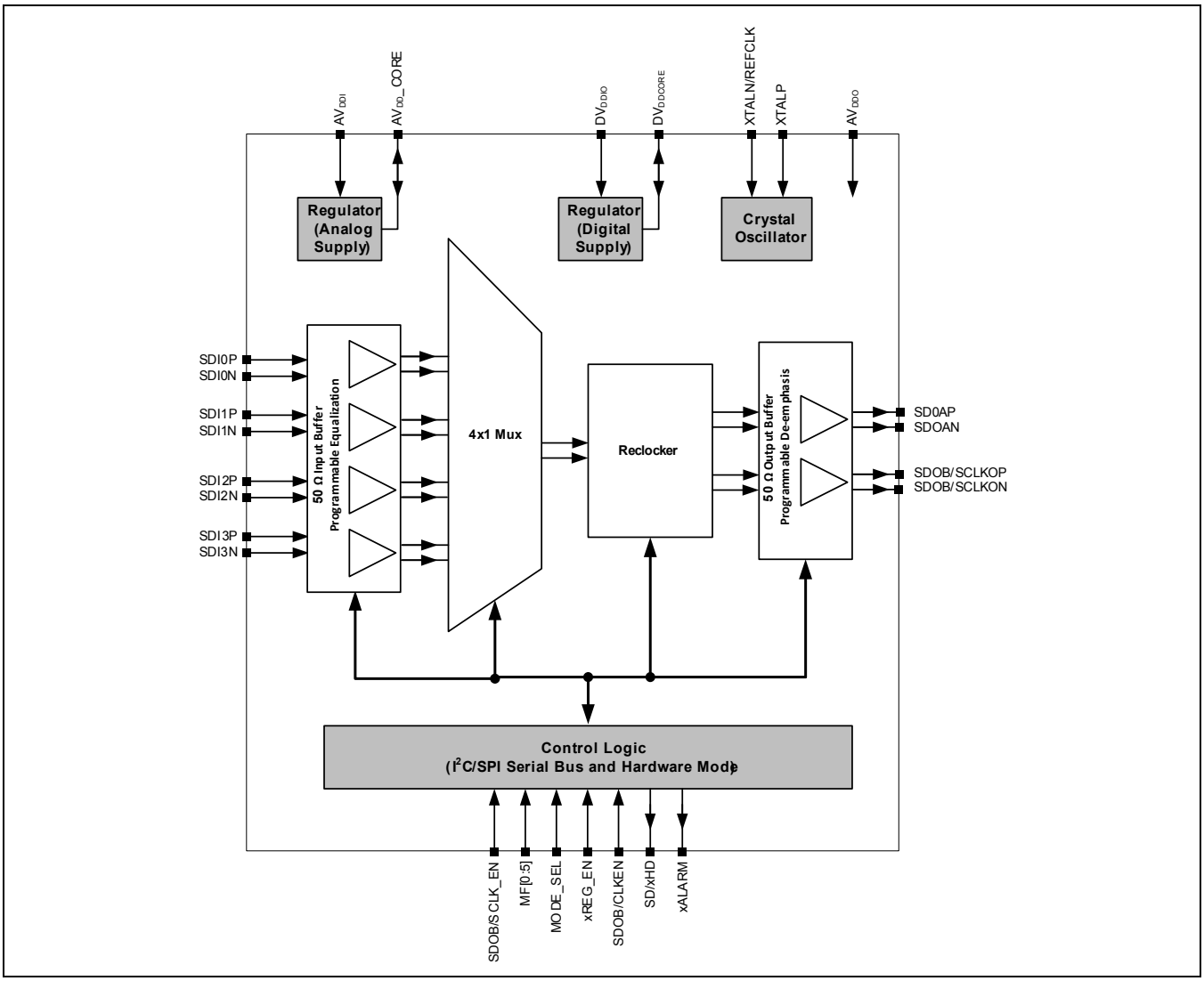
1. New ASE package and the old Amkor package have the same footprint dimensions

4.0 Functional Description

4.1 Functional Block Diagram

Figure 4-1 illustrates the M21245 block diagram. The subsequent sections provide additional detail on the operation of the device.

Figure 4-1. M21245 Block Diagram



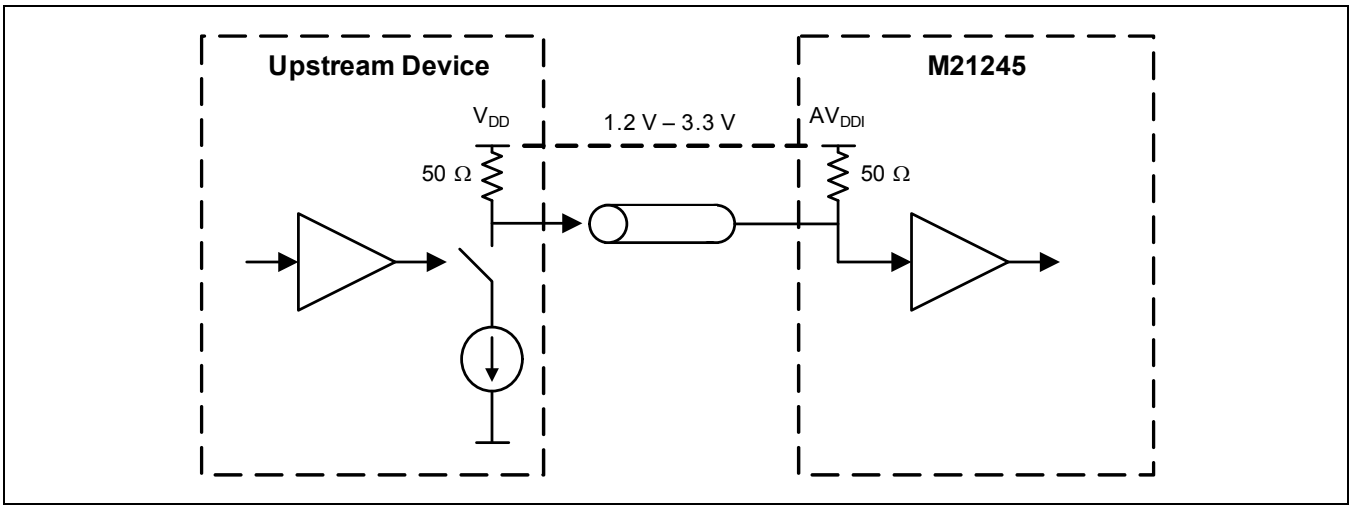
4.2 High-Speed Differential Inputs

The M21245 features four differential inputs; compatible with PCML. LVDS and LVPECL signal levels are also accommodated. Serial data to be retimed is presented to these four inputs. Each input is terminated with a 50 Ω termination to AV_{DDI}. AV_{DDI} can be supplied from any voltage ranging from 1.2 V to 3.3 V.

In order to improve signal integrity when used in large systems, each input also comes equipped with programmable input equalization (IE) for FR4 trace. There are four settings for input equalization: 0 dB (or no equalization), 2 dB, 4 dB, and 6 dB. In serial control mode, the input equalization level for each input may be set by programming the desired value to register.**Input EQ Config** (addresses 00h–03h). Alternatively, in hardware mode, the input equalization for all of the inputs may be set globally through pin.**IE_CTRL (MF2)**. In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC-coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC-coupling will result in more system jitter margin. In order to accommodate DC-coupling with the upstream device, the AV_{DDI} power domain of the M21245 is electrically independent from all other power domains therefore allowing it to be tied to the V_{DD} of the upstream device. This is demonstrated in Figure 4-2 below.

Figure 4-2. M21245 AV_{DDI} Connected to the V_{DD} of the Upstream Device



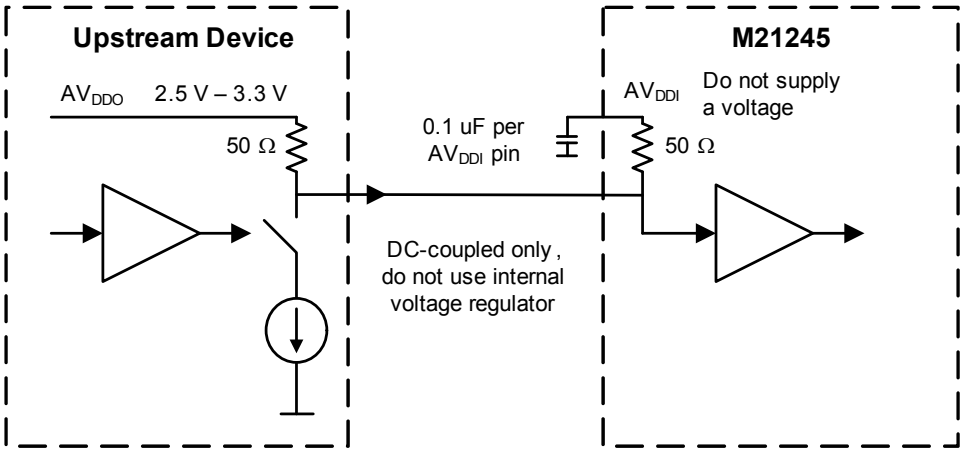
Alternatively and under certain conditions, the M21245 allows for the inputs to be self biased eliminating the need for an electrical connection between the supply voltages of the upstream device and M21245. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M21245 completely isolated, while using DC-coupling. AC-coupling should not be used with the self bias interface. This self-biasing scheme is demonstrated in Figure 4-3 below.

When using the M21245 in self biased mode, specific conditions must be met:

1. The self biased inputs must be DC-coupled. No AC-coupling is supported in self biased mode.
2. The AV_{DDO} of the upstream device must be 2.5 V or greater. AV_{DDO} levels 1.2 V and 1.8 V are not supported in this mode.
3. The common mode of the upstream signals must be greater than 600 mV.

4. Internal voltage regulators are disabled.
5. All inputs are configured in self biased mode. Combination of self biased and non-self biased is not supported.

Figure 4-3. Self Biasing the Input of M21245



NOTE:
1. For self-bias applications, no voltage must be applied to the AV_{DDI} pin. Every AV_{DDI} pin should be decoupled to GND with a 0.1 µF capacitor as shown in Figure 4-3.

A Loss of Signal (LOS) detector monitors each input and issues an alarm when the input signal level dips below the detection threshold set in register.**LOS Config** (address 06h). See Section 4.3 for more information on the LOS circuit.

In order to correct any duty cycle distortion (DCD) in the input signal, or any DC offset buildup in the internal signal path, a DC correction loop has been added. Programming register.**GBL CTRL1**.bit[1] (address 0Dh) to a '1' will disable the DC correction loop for all inputs.

The M21245 includes a 4:1 multiplexer. This allows any one of the four input signals to be routed to the reclocker. By default, SDI0 is selected to be routed to SDO0. The selected input can be set using register.**Input MUX CTRL** (address 07h).

By default, only the selected input is powered up, with all other inputs powered down. When an input is powered down, its associated LOS circuitry is disabled. If required, all the other inputs can also be powered up by setting register.**GBL CTRL1**.bit[3] (address 0Dh). This will allow for a faster response if rapid input switching is required as there is no delay waiting for the circuitry to power-up and adjust to the input signal, but has the disadvantage of consuming more power.

With all inputs enabled, the power consumption increases by 100 mW.

4.3 LOS (Loss of Signal)

The M21245 has an integrated LOS circuit on each of its four high-speed inputs. This circuit monitors the input amplitude and if it falls below the detection threshold it asserts the LOS alarm bit by setting this to a logic high. These alarm bits are latched and will need to be reset with register.**CLEAR ALARMS** (address 85h), by setting bit 0 to a high and back to a low. Hysteresis is built into the LOS circuit to avoid chattering. The LOS threshold can be set to a different level by using register.**LOS Config**.bits[7:5] (address 06h), this changes the level on all four inputs.

By default, the LOS alarm mutes the signal from that particular input. Setting register.**LOS Config**.bit[3] (address 06h) to a high will disable this feature.

4.4 High-Speed Output Description

There are two high-speed outputs available on the M21245. By default, only SDOA is powered up, setting register.**SDOB CTRL**.bit[2] (address 0Ch) high will enable SDOB. The output signal will be a copy of SDOA. In hardware mode, SDOB is enabled with the SDOB/SCLK_EN input pin in a floating (F) or high (H), see Table 3-1.

A further function of this output is a serial clock source. By setting register.**CLK EN**.bit[0] (address 06h) to high, the reclockers recovered clock is output to the SDOB/SCLK pins. In hardware mode this function is selected by setting SDOB/SCLK_EN high, see Table 3-1.

The M21245 features differential current mode logic (CML) drivers with integrated 50 Ω pull-ups to AV_{DDO} for the output of each reclocker channel. AV_{DDO} may be supplied from any voltage ranging from 1.2 V to 3.3 V.

The differential, peak-to-peak, output swing for each CML driver is programmable and may be set to 600 mV_{PPD}, 800 mV_{PPD}, or 1200 mV_{PPD}. Please note that the 1200 mV_{PPD} output swing setting is only available when AV_{DDO} is supplied from a voltage of 1.8 V or greater. The swing setting may be programmed by writing to register.**SDOA CTRL**.bits[3:2] (address 09h) for SDOA, and register.**Output CTRL**.bits[3:2] (address 0Bh) for SDOB.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 trace. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In serial control mode, the output de-emphasis level for each input may be set by programming the desired value to register.**SDOA CTRL**.bits[1:0] for SDOA and register.**SDOB CTRL DE**.bits[5:4] (address 0Ah) for SDOB. Alternatively, in hardware mode, the de-emphasis level for all of the outputs may be globally set through pin.**DE_CTRL** (MF3). In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC-coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC-coupling will result in more system jitter margin. In order to accommodate DC-coupling with the upstream device, the AV_{DDO} power domain of the M21245 is electrically independent from all other power domains therefore allowing it to be tied to the V_{DD} of the downstream device. This is demonstrated in Figure 4-4 below.