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M21262-12

CDR/Reclocker with 4:1 Input Multiplexer

Rev V3

Features

- CDR/Reclocker with 4:1 input mutliplexer
- Integrated loop filter and terminations
- Serial control or hardwired control, JTAG boundary scan
- Low power consumption of 405 mW (all channels active)
- Built-in pattern generator and receiver for module and system testing (PRBS, 8b/10b, Fibre Channel, User Programmable patterns)
- User Selectable Input Equalization and Pre-Emphasis for backplane ISI reduction

Applications

- HD/SD-SDI Routing Switchers, Distribution amplifiers, and transport systems
- SONET systems and modules
- 10 GBASE-CX4 systems
- Gigabit Ethernet systems
- PCI-Express
- SAS/S-ATA/S-ATA2 systems

Standards Compliance

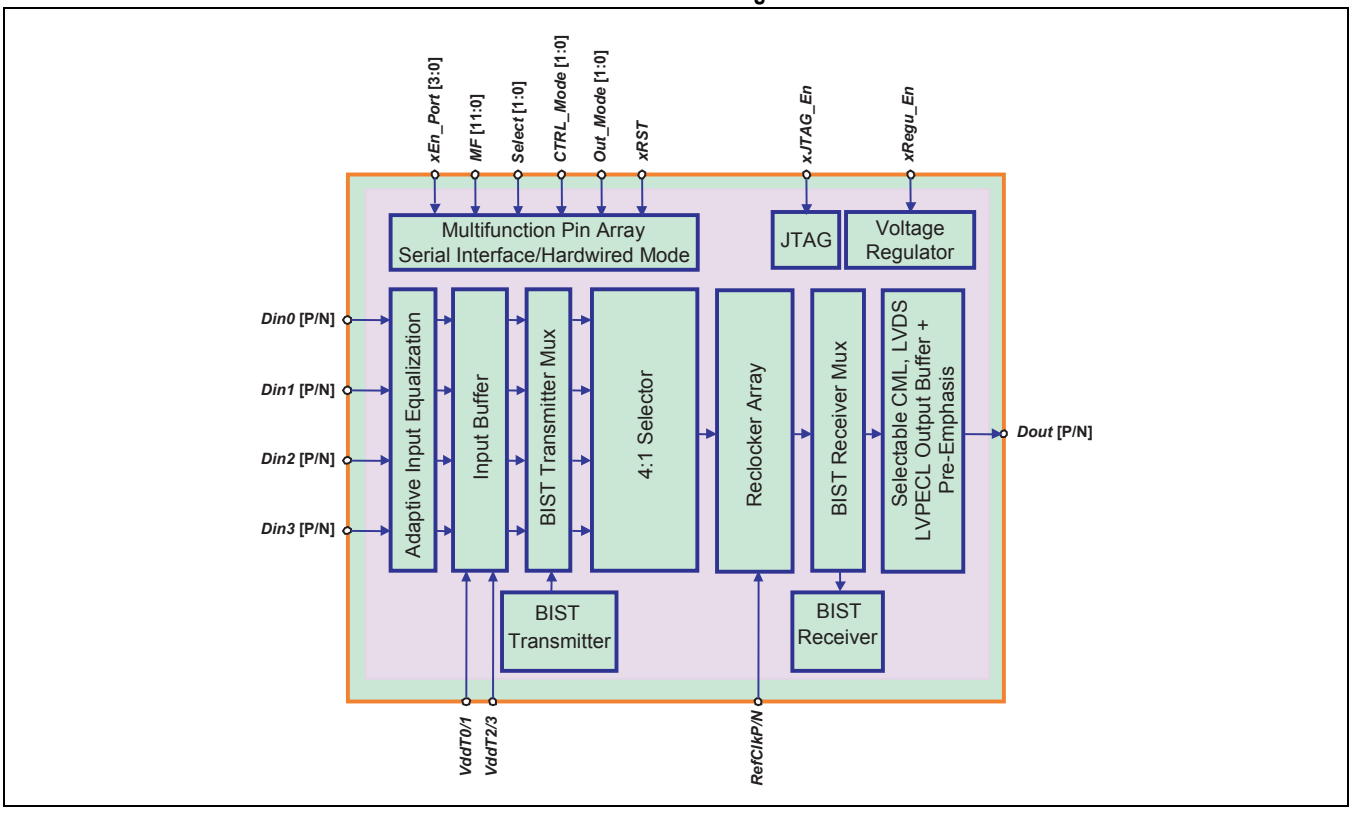
- SMPTE 292M
- SMPTE 259M
- SMPTE 344M
- SMPTE 424M

The M21262 is a CDR/reclocker with 4:1 input multiplexer for telecom, datacom, and HD/SD video applications. Each output channel has an independent multi-rate CDR capable of operating at data rates between 42 Mbps and 3.2 Gbps.

The M21262 can be controlled either through hardwired pins or through a serial programming interface. The hardwired mode eliminates the need for an external microcontroller to configure the device. The serial programming interface allows complete control of the device and is available as a two-wire or a four-wire interface.

The M21262 device supports JTAG external boundary scan, which includes all of the high-speed I/O as well as the traditional digital I/O.

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M21262-12	72-terminal, 10mm, MLF	-40 °C to 85 °C
M21262G-12*	72-terminal, 10mm, MLF	-40 °C to 85 °C

* The letter “G” designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

Revision History

Revision	Level	Date	Description
V3	Release	May 2015	Updated logos and page layout. No content changes.
C (V2)	Release	April 2008	Added SMPTE 424M in standards compliance list. Revised Section 2.8. Added 2 x HD-SDI data in Table 1-6, Table 1-15, and Table 2-14.
B (V1)	Release	April 2007	Removed M21261 from data sheet. Added support for datacom/telecom rates up to 3.2 Gbps. Updated specification tables. Updated register tables.
A (V1P)	Preliminary	April 2004	Initial release. Original Document Number 21261-DSH-001-A.

Table of Contents

1.0 Functional Description

1.1 Detailed Feature Descriptions

1.1.1 Conventions

Throughout this data sheet, physical pins will be denoted in ***bold italic*** print. An array of pins can be called by each individual pin name (e.g. ***MF0***, ***MF1***, ***MF2***, ***MF3***, and ***MF6***) or as an array (e.g. ***MF*** [6, 3:0]). The M21262 control is accessed through registers that employ an 8-bit address and an 8-bit data scheme. Registers are denoted in italic print, (e.g. *TestRegister)* and individual bits within the register will be called out as *TestRegister* [4:3] to denote the 4th and 3rd bit where bit 0 is the LSB and bit 7 is the MSB. Many features of the device are bit mapped within a register; if the status of the other bits are uncertain, it is recommended that the user reads the value from the register before writing, to assure only the desired bits change. Writing in the same value to the bits within a register does not cause glitches to the unchanged features. The addresses for the registers as well as their functions can be found in detail in Chapter 3. The purpose of the text description is to highlight the features of the registers. For redundant items, such as the channel number, the registers will have a nomenclature of *TestReg_*0 for channel 0, *TestReg_*1 for channel 1, *TestReg_*2 for channel 2, *TestReg_*3 for channel 3.

1.1.2 Reset

Upon application of power, the M21262 automatically generates a master reset. At any time, forcing ***xRST*** = L causes the M21262 to enter the master reset state. A master reset can also be initiated through the registers in the serial interface control mode by writing AAh to *Mastreset*. Once a master reset is initiated, all registers are returned to the default values, the internal state machines cleared, and all CDR/RCLK/BIST reset to the out-of-lock condition. After a reset, the register *Mastreset* will automatically return to the default value of 00h.

The CDR/RCLK can be soft reset by setting CDR *RCLK_ctrlA* [7] = 1. The bit should be returned to 0b for normal operation. After a soft reset, the registers that determine the CDR/RCLK operation options such as data rate, window sizes, etc., remain unchanged and only the CDR/RCLK state machine is reset, resulting in an out-of-lock condition.

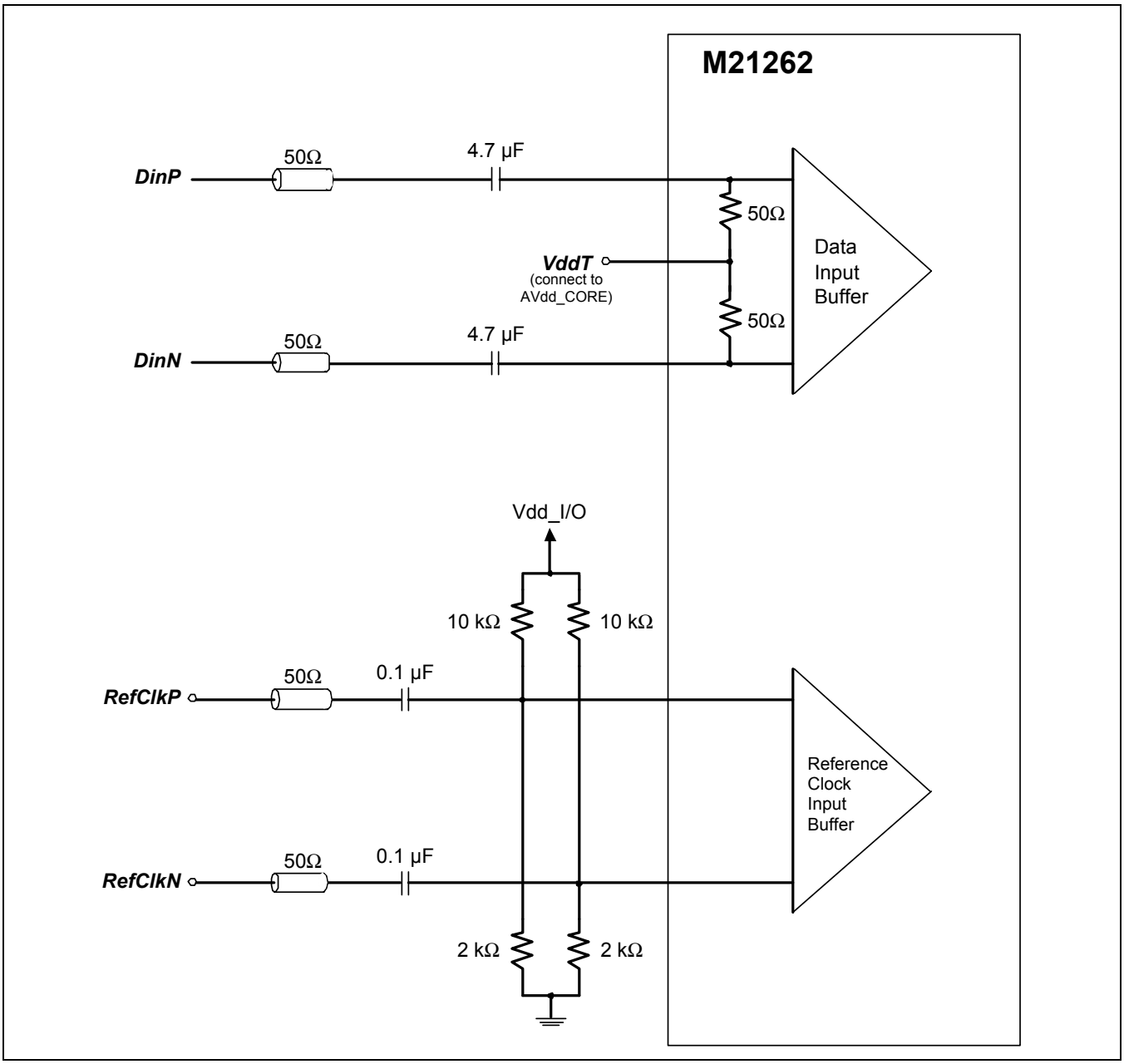
1.1.3 Internal Voltage Regulator

The digital and analog core are designed to run at 1.2V, however, for operation from 1.8V to 3.3V, an internal linear regulator is provided. ***xRegu_En*** = L enables the voltage regulator which uses ***AVdd_I/O*** and ***DVdd_I/O*** to generate the required 1.2V for ***AVdd_Core*** and ***DVdd_Core***. In this mode, the ***AVdd_Core*** and ***DVdd_Core*** pins should be connected to a floating DC low inductance PCB plane and AC bypassed to ***Vss*** using standard decoupling techniques. If desired, ***AVdd_Core*** and ***DVdd_Core*** can be separated into individual planes. If 1.2V is available, it can be connected directly to ***AVdd_Core*** and ***DVdd_Core,*** to save power, by bypassing the internal linear regulator with ***xRegu_En*** = H. In this case, it is recommended that the ***AVdd_Core*** and ***DVdd_Core*** pins be tied together to a common PCB plane, and bypassed to ***Vss*** with standard decoupling techniques.

1.1.4 High-Speed Input/Output Pins

The high-speed input data interface is a differential input buffer, similar to a PCML design that is referenced to Avdd_CORE (1.2V). The high-speed serial differential data (42 Mbps to 3200 Mbps) enters the device via ***Din*** [3:0, P/N]. Inputs 0 and 1 are internally terminated with 50Ω to ***VddT0/1*** and inputs 2 and 3 are terminated with 50Ω to ***VddT2/3***. The ***VddT*** pins should be connected to ***AVDD_Core*** for a proper termination of the inputs. See Figure 1-1 for recommended data and reference clock input coupling circuits.

Figure 1-1. Recommended Data and Reference Clock Input Coupling Circuitry



The M21262 supports multiple high-speed output modes. The output modes are selectable with hardwired pins only. The I/O interface is set with ***Out_Mode*** [1:0] and the output level with ***MF*** [9:8] as shown in Table 1-1. In the serial interface mode, the *Out_ctrl*_N [7:6] register is used to set the data level, and ***Out_Mode*** [1:0] is used to set the interface type. In the serial interface mode, the data output can be enabled with *Out_ctrl*_N [2] = 1b (default) and the output data polarity can be flipped by setting *Out_ctrl*_N [3] = 1b (default: no inversion). Output data polarity flip is an internal function that would have the same effect as switching the P and N terminals. The recommended ***AVdd_I/O*** for the different output interfaces is shown in Table 1-2. The nonstandard lower swing modes for PECL and InfiniBand are provided for lower power dissipation, when desired.

Table 1-1. Output Interface and Level Mapping (For both hardwired and software modes)

Multifunction Pins & Register MF [9:8] *Out_ctrl_N [7:6]*	**PCML Mode** ***Out_Mode*** **[1:0] = 00b**	**LVDS Mode** ***Out_Mode*** **[1:0] = 01b**	**PCML+ Mode** ***Out_Mode*** **[1:0] = 11b**
00b	Off	Off	Off
01b	550 mV	RRL at 450 mV	900 mV
10b	900 mV	GPL at 650 mV	1200 mV
11b	1200 mV	1000 mV	1500 mV

Table 1-2. Output Interface and Recommended AVdd_I/O Range

Output Logic	***AVdd_I/O*** **Range (V)**
Off	1.8–3.3
PCML at 550 mV	1.8–3.3
PCML at 900 mV	1.8–3.3
PCML at 1200 mV	1.8–3.3
PCML+ at 1500 mV	1.8–3.3
LVDS GPL	1.8–3.3
LVDS RRL	1.8–3.3

1.1.5 Selector Settings

Table 1-3 details the selector configuration for each setting for the hardwired pins ***Select_Mode***[1:0].

The M21262 allows the user to route any of the four inputs to the output channel. The selector can be configured through the control register or through the hardwired pins ***Select_Mode***[1:0].

Table 1-3. Selector Configuration Settings

Mode 0	Mode 1	Output
0	0	input 0
0	1	input 1
1	0	input 2
1	1	input 3

1.1.6 Reclocker Reference Frequency

An external reference clock is applied to ***RefClk***[P/N] to enable frequency acquisition in the Reclocker. PCML, LVTTL, CMOS are examples of the wide variety of interfaces supported for the reference clock. The inputs contain a DC-coupled 100Ω differential termination between ***RefClkP*** and ***RefClkN*** along with a 100 kΩ pull-down on each terminal to ***Vss***. After this termination/pull-down block, the inputs are AC coupled internally. The common-mode and allowable voltage swings are specified in Table 2-10. The ***RefClk*** common-mode must be above 250 mV, which may require external pull-ups, in the case of external AC coupling.

1.1.7 Multifunction Pins Overview

The M21262 is designed to be an extremely versatile device, with many user selectable options in the CDR/RCLK and I/O to optimize performance. All of these options can be accessed and controlled through the serial interface. The serial interface I/O pins and address pins are mapped to the multifunction pins ***MF*** [11:0]. A subset of the key features for most applications, such as standard data rates, I/O levels, etc., can be selected through ***MF*** [11:0] in the hardwired mode. The hardwired mode does not require the use of the serial interface. In this mode, upon power up (auto reset on power up), the M21262 function is determined by the status of the hardwired pins. During operation, the hardwired pins can change states, which would cause the device to follow with the appropriate action. Another feature of the multifunction pins is to support JTAG testing of this device during PCB manufacturing.

The various control and test modes of this device are selected with three pins: ***CTRL_Mode*** [1:0]**,** and ***xJTAG_En***. ***xJTAG_En =*** L overrides ***CTRL_Mode*** [1:0]**,** and puts the device in JTAG test mode, while ***xJTAG_En*** = H allows ***CTRL_Mode*** [1:0] to determine the M21262 control mode, as summarized in Table 1-4.

Table 1-4. Mode Select Pins

Pin	JTAG Test Mode	Hardwired Mode	4-Wire Serial	I^2C-Compatible 2-Wire Serial
xJTAG_En	L	H	H	H
CTRL_Mode [1:0]	no impact	11b	00b	01b

1.1.8 Multifunction Pins Defined for Hardwired Mode

In the hardwired mode, a subset of options in the M21262 can be accessed with hardwired physical pins, as defined in Table 1-5. The hardwired bit rates along with the default reference clock frequency are shown in Table 1-5. Table 1-6 provides the default reference clock frequency associated with each hardwired data rate.

Table 1-5. Multifunction Pins for Hardwired Mode

Pin	Name	Function	Description
MF0	Rate_Sel_0	Data rate selection	CDR/Reclocker data rate select (see Table 1-6 for description)
MF1	Rate_Sel_1	Data rate selection	CDR/Reclocker data rate select (see Table 1-6 for description)
MF2	Rate_Sel_2	Data rate selection	CDR/Reclocker data rate select (see Table 1-6 for description)
MF3	Rate_Sel_3	Data rate selection	CDR/Reclocker data rate select (see Table 1-6 for description)
MF4	xPre_Emp_En	Pre-emphasis control	L = Pre-emphasis enable H = Pre-emphasis disable
MF5	RSVD_Int_0	MACOM internal	Internal use only
MF6	RSVD_Int_1	MACOM internal	Internal use only
MF7	xPol_Flip_En	Data polarity flip	L = Data polarity flip H = Standard data polarity
MF8	Out_Level_[1:0]	Output level selection	00b: All outputs disabled 01b: 500 mV (CML) 10b: 900 mV (CML) 11b: 1200 mV (CML) See Table 1-1 for the other output interface modes.
MF9		Output level selection	
MF10	xEQ_En	Equalization control	L = Input equalization enabled H = Input equalization disabled
MF11	xRCLK_BYP_En	CDR/RCLK bypass control	L = CDR/Reclocker bypassed and powered down H = CDR/Reclocker enabled

Table 1-6. Hardwired Bit Rates and Associated Reference Frequencies

Pins *MF[3:0]*	Application	Bit Rate (Mbps)	Reference Frequency (MHz)
0000	2 x HD-SDI	2967/2970	12.0
0001	HD-SDI	1485 /1483.5	12.0
0010	2 x SD-SDI	540	12.0
0011	Progressive Scan Video	360	12.0
0100	SD-SDI	270	12.0
0101	Legacy Comp Video	177	12.0
0110	Legacy Comp Video	143	12.0

1.1.9 Multifunction Pins: Four-Wire Serial Interface

The second serial interface mode is a four-wire programming interface that has been traditionally used on MACOM earlier generation crosspoints and CDRs and is capable of higher speed operation then the two-wire interface. The interface consists of a unidirectional clock and a data input and data output line. For use with multiple ICs, a serial interface chip select pin is provided. Table 1-7 illustrates how the four-wire serial interface maps into the multifunction pins. This serial interface can operate with a maximum clock rate of 20 MHz.

Table 1-7. Multifunction Pins for Four-Wire Interface

Pin	Function	Description
MF4	SDI	Serial Data In
MF5	xCS	Chip Select, active low
MF10	SCLK	Clock
MF11	SDO	Serial Data Out

The serial I/O shifts data in from the external controller on the rising edge of ***SCLK***. The serial I/O operation is gated by ***xCS***. Data is shifted in on ***SDI*** on the falling edge of ***SCLK***, and shifted out on ***SDO*** on the rising edge of ***SCLK***. To address a register, a 10-bit input consists of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), followed by the 8-bit ADDR (MSB first) as shown in Figure 1-2.

Figure 1-2. Serial Word Format

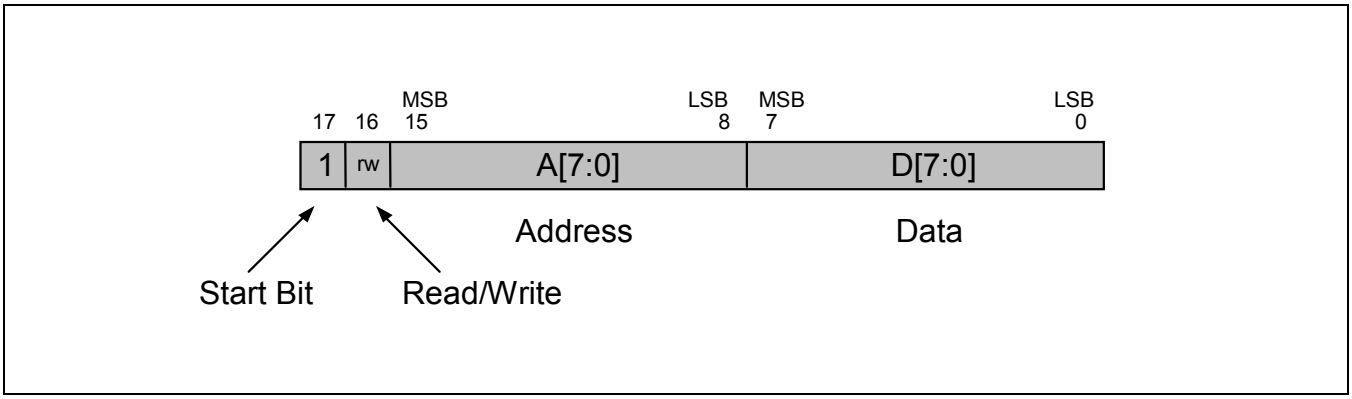


Figure 1-3 illustrates the Serial Write Mode. To initiate a Write sequence, ***xCS*** goes low before the falling edge of ***SCLK***. On each falling edge of the clock, the 18-bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register. The rising edge of ***xCS*** must occur before the falling edge of ***SCLK*** for the last bit. Upon receipt of the last bit, one additional cycle of ***SCLK*** is necessary before DATA transfers from the input shift register to the addressed register. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 1-3. Serial WRITE Mode

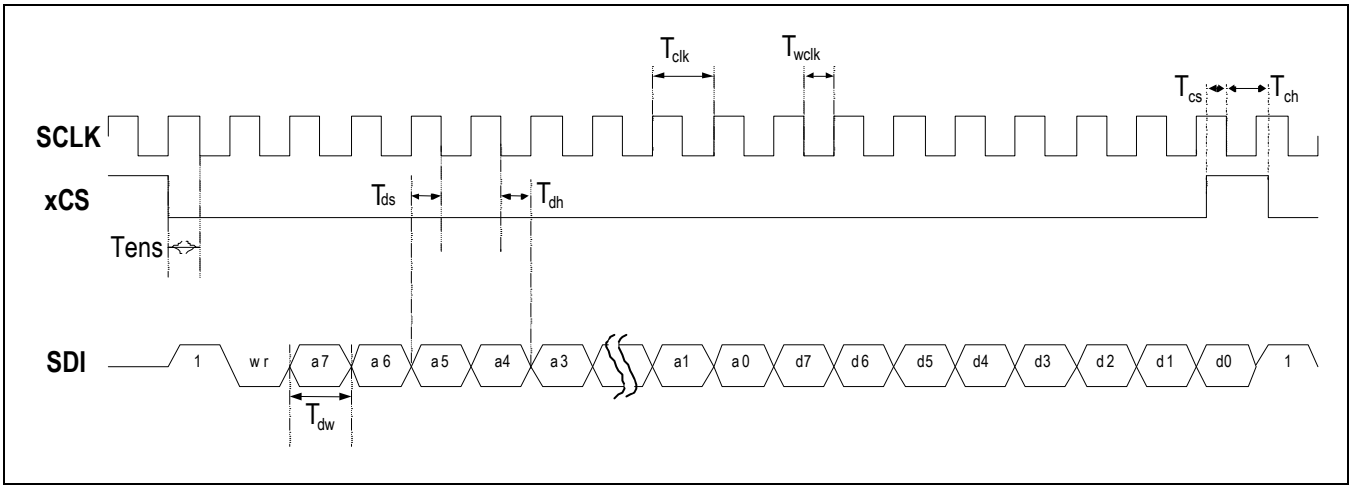
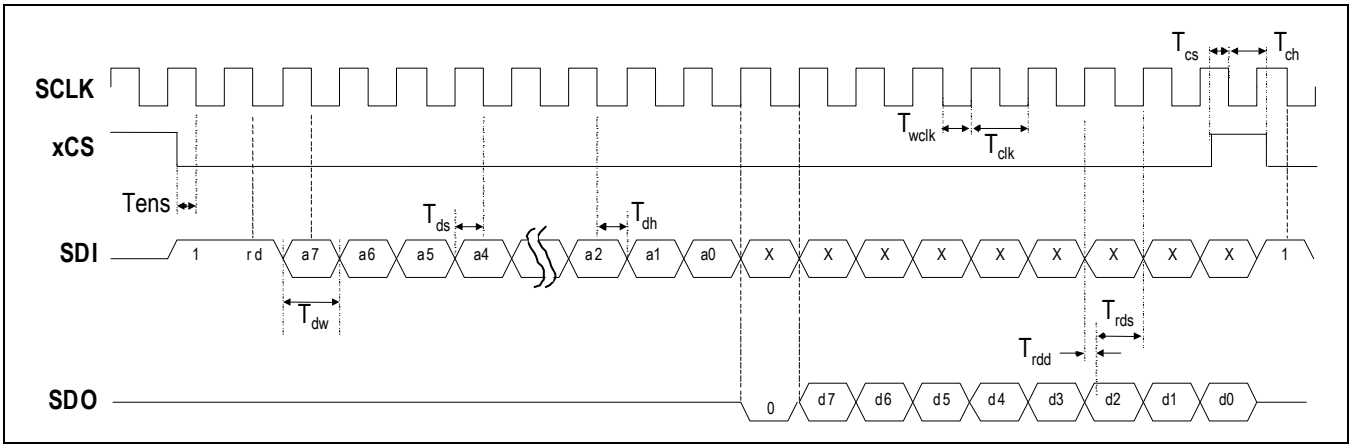


Figure 1-4 illustrates the Serial Read mode in where ***xCS*** goes low before the falling edge of ***SCLK***. On each falling edge of ***SCLK***, the 10-bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8-bits of the DATA are shifted out. The SB for a Read is always 0.

Figure 1-4. Serial READ Mode



On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16-bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of ***xCS*** always resets the serial operation for a new Read or Write cycle.

The timing diagrams for the serial write and read operations are shown in Figure 1-3 and Figure 1-4, respectively. Table 1-8 contains the specifications for the various timing parameters for the serial programming interface.

Table 1-8. Serial Interface Timing—Specified at Recommended Operating Conditions

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
t_{dw}	Data width	—	14	—	—	ns
t_{dh}	Data hold time	—	5	—	—	ns
t_{ds}	Data setup time	—	5	—	—	ns
t_{ens}	Enable setup time	—	5	—	—	ns
t_{cs}	Chip select setup time	—	2	—	Tclk - 2	ns
t_{ch}	Chip select hold time	—	2	—	—	ns
t_{rdd}	Read data output delay	—	1	—	—	ns
t_{rds}	Read data valid	—	9	—	—	ns
t_{clk}	SCLK period width	—	14	—	—	ns
t_{wclk}	SCLK minimum low duration	—	5	—	Tclk - 5	ns
t_r	Output rise time	1	1	—	4	ns
t_f	Output fall time	1	1	—	4	ns

NOTES:

1. Edge rate in the high-edge rate mode.
2. Designed for max serial speed of 20 MHz read/write.

1.1.10 Two-Wire Serial Interface

The two-wire serial interface is compatible with the I^2C standard. The M21262 supports the read/write slave-only mode, 7-bit device address field width, and supports the standard rate of 100 Kbps, fast mode of 400 Kbps, and high-speed mode of 3.4 Mbps. The 7-bit address for the device is determined with ***MF*** [6:0], which allows for a maximum of 124 unique addresses for this device. The four addresses 000001xx should not be used. SDA (***MF11***) and SCL (***MF10***) can drive a maximum of 500 pF each at the maximum rate. During the write mode from the master to the M21262, data is latched into the internal M21262 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. Table 1-9 summarizes the multifunction pins for the two-wire serial interface mode. For further information on timing, please see the I^2C bus specification standard.

Table 1-9. Multifunction Pins for Two-Wire Interface

Pin	Function	Description
MF0	Address bit 0	7-bit device address; address bit 0 is LSB, address bit 6 is MSB
MF1	Address bit 1	
MF2	Address bit 2	
MF3	Address bit 3	
MF4	Address bit 4	
MF5	Address bit 5	
MF6	Address bit 6	
MF10	SCL	Clock input
MF11	SDA	Data input/output

1.1.11 JTAG

The M21262 supports JTAG external boundary scan, which includes all of the high-speed I/O, as well as the traditional digital I/O. Table 1-10 shows the multifunction pins signal mapping for JTAG testing.

Table 1-10. Multifunction Pins for JTAG

Pin	Function	Description
MF8	TMS	Test select
MF9	TDI	Test data input
MF10	TCK	Test clock
MF11	TDO	Test data output

1.1.12 Input Deterministic Jitter Attenuators

Each of the four input channels contains an input equalizer to compensate for high-frequency loss. In the hardwired mode, there is the option to set input equalization on or off. In the two-wire serial interface control mode, the default state allows for configurable input equalization settings using *Ineq_ctrl*_N [2:0], for which the default setting of 100b is optimized for trace lengths between 10–46 inches.

The input equalization settings have been optimized for a variety of backplane PCB applications, such as board traces and cables. For board traces on FR4, the input equalizer can drive trace lengths of up to 72” at 1.6 Gbps and up to 60” at 3.1875 Gbps. The equalizer has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The input equalizer was designed to compensate for the deterministic jitter accumulation effects of typical backplane interconnects, which have bandwidths of hundreds of MHz to a few GHz. The equalizers are not expected to make a significant difference in performance with signal data rates less than 1 Gbps.

Another component of input deterministic jitter is inter-symbol interference (ISI) due to DC offsets. By default, a DC servo-like circuit is enabled to correct for this type of deterministic jitter, and can be disabled by setting

Ineq_ctrl [4] = 0b. The DC servo can also be used to track changes in the common mode, for single-ended operation. When the CDR, DC servo, and AIE are all enabled, the jitter tolerance should be greater than 1 UI.

Figure 1-5. STS-48 waveform after transmission through 76" of PCB traces (input to M21262)

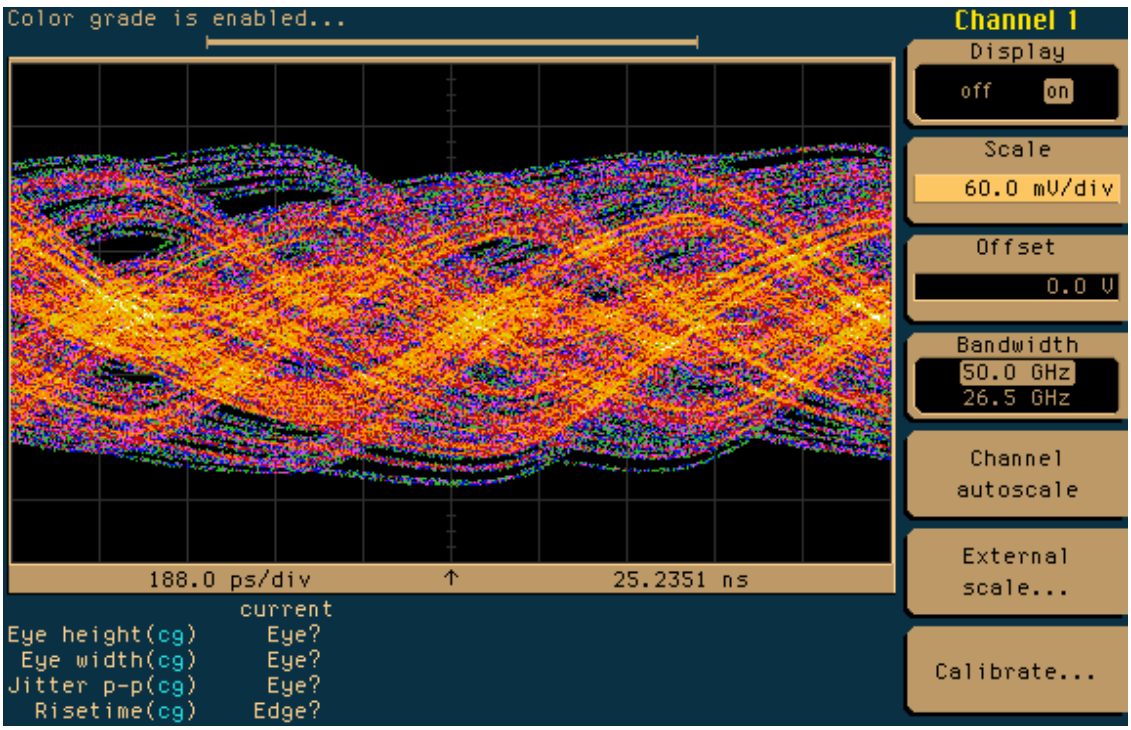
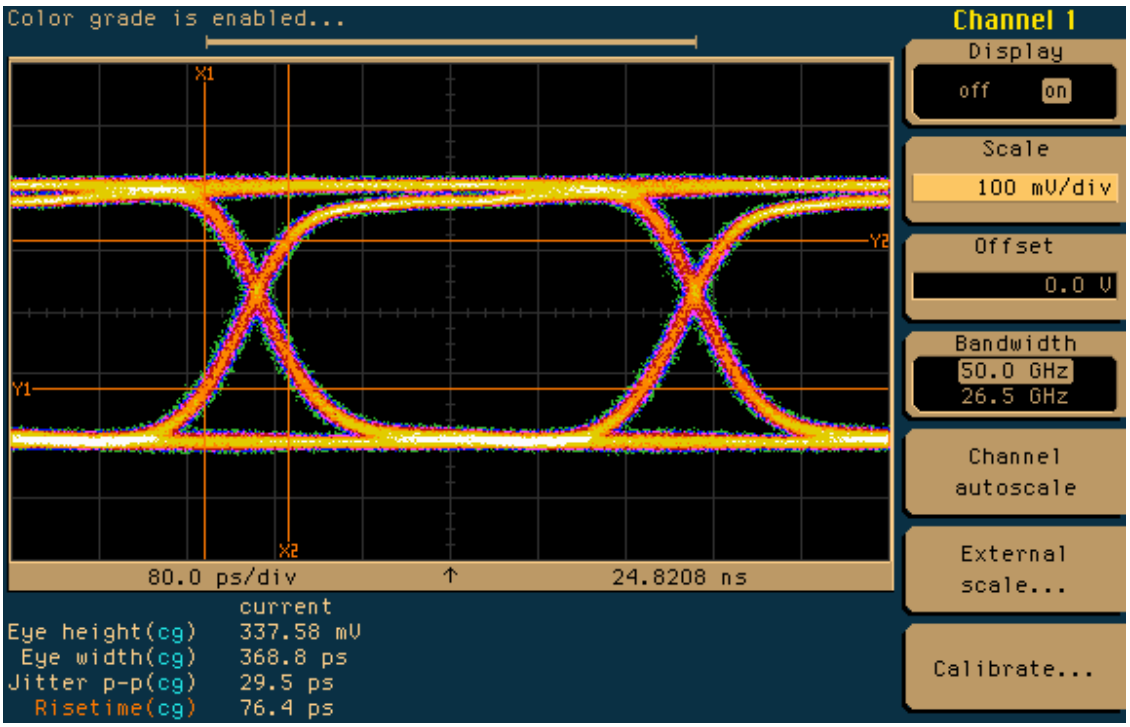


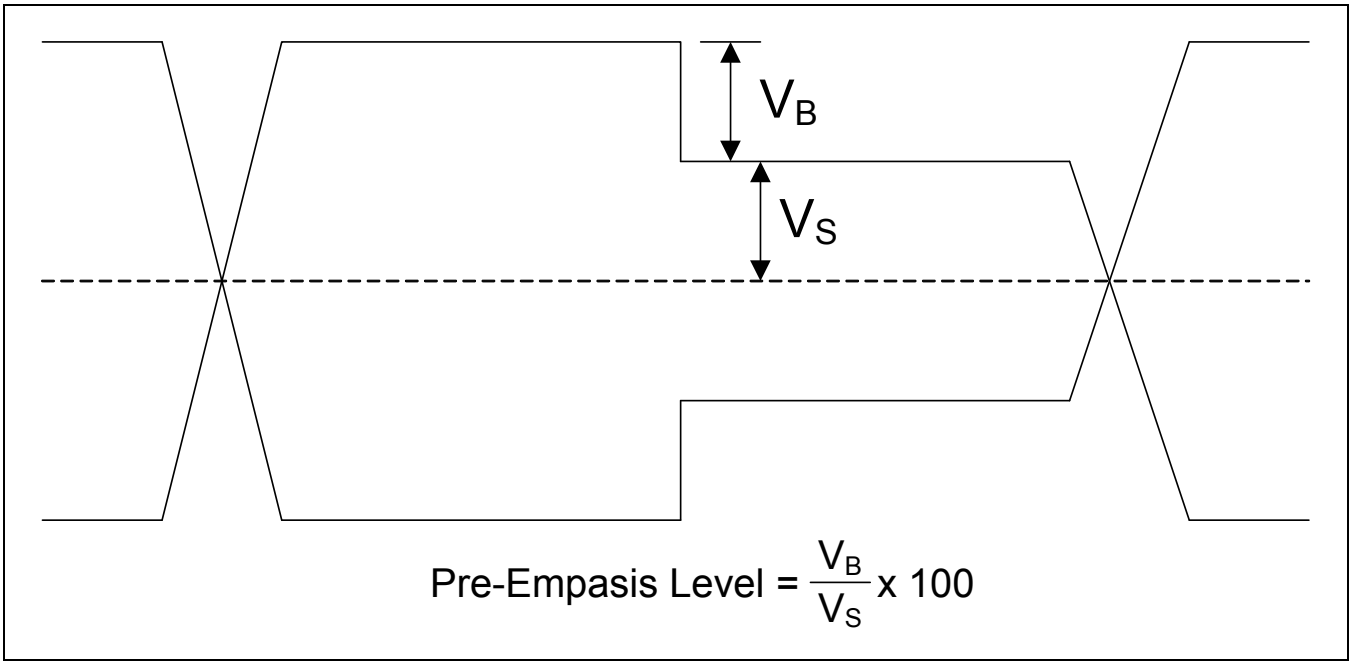
Figure 1-6. STS-48 waveform at M21260 output with input shown in Figure 1-4



1.1.13 Output Pre-Emphasis

The output channel contains an output pre-emphasis circuit that can be used to select the optimal pre-emphasis level. The pre-emphasis settings have been optimized for a variety of backplane PCB applications. For board traces on FR4, the pre-emphasis circuit can drive trace lengths up to 60” at 1.6 Gbps. Like the input equalizer settings, the output pre-emphasis circuit has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The digital pre-emphasis level is selected, for each output channel, with *Preemp_ctrl* [2:0], and the default value of 000b corresponds to pre-emphasis disabled. The pre-emphasis circuit tracks the signal data rate throughout the multirate range, however, like the input equalizer, it is designed to compensate for the bandwidth limitations of the interconnect, and may not have the desired effects at the low end of the multirate range. When the CDR/RCLK has been disabled or bypassed, analog pre-emphasis must be used in place of digital pre-emphasis. Writing the data value 1b to the register *Preemp_ctrl* [3] enables analog pre-emphasis, whereas writing the data value 0b to the register *Preemp_ctrl* [3] enables digital pre-emphasis. Once analog pre-emphasis has been enabled, the boost level may be chosen with *Preemp_ctrl* [5:4], and the bandwidth may be chosen with *Preemp_ctrl* [6]. The output pre-emphasis function is available for all data interfaces and levels.

Figure 1-7. Definition of Pre-Emphasis Levels



1.1.14 CDR/RCLK Overview

When the CDR/RCLK achieves phase lock onto the incoming data stream, it removes the incoming random jitter above its loop bandwidth. The M21262 output data has extremely low jitter, due to retiming with a very low jitter generation CDR/RCLK. Clock outputs are also provided, but are disabled by default.

Each CDR/RCLK is capable of multirate operation which is achieved by a combination of built in VCO frequency dividers (VCD), Data Rate Dividers (DRD), and a wide VCO tuning range (F_{min} = 2.0 GHz, F_{max} = 3.2 GHz). As a result, the allowed input data range is F_{min} / DRD_{max} to F_{max} / DRD_{min}. Although the ranges are not continuous, the ranges are deliberately chosen to cover all typical applications.

By default, the loop bandwidth is set to pass 2 x HD-SDI Video and SONET STS-48 specifications, with less than 0.1 dB of bandwidth peaking. Within a given VCO frequency range, the bandwidth will scale proportionately. For example, if the loop bandwidth (LBW) is 1.19 MHz at 1.485 GHz, then at 2.97 GHz the LBW will be 2.38 MHz, and peaking will be less than 0.1 dB. When DRD is not equal to 1, the bandwidth at DRD = 1 scales by the DRD divide ratio. For example, if the LBW is 2.38 MHz at 2 x HD-SDI with DRD = 1, then if DRD = 2 for HD operation, the LBW will be 1.19 MHz. In general, the default bandwidth will meet SMPTE specifications for all bit rates down to 143 MHz. Internal filter components assure that the peaking will not exceed 0.1 dB for all DRDs up to 16. In the hardwired mode, the LBW will be properly set for the hardwired bit rates. In the serial register mode, the default bandwidth scales automatically with the input bit rate, and the bandwidth can be tuned through registers.

The CDR/RCLK requires an external reference clock to be connected to the ***RefClkP/N*** pins. The CDR/RCLK contains an internal frequency prescaler that allows a single reference to be used for multiple bit rates and thereby ease the burden of having to route and switch multiple frequency references.

Frequency acquisition is accomplished with two key sections. The first section is a secondary phase/frequency lock loop (P/FLL) that drives the VCO towards the desired frequency. The second section is the loss-of-lock circuitry (LOLCir), that turns on or off the secondary P/FLL. In general LOL has register bits (*Alarm_LOL*) which are active high, and pins (***xLOL***[3:0]) which are active low, for wired OR use to be wired OR externally. In the general context, they will be referred to as LOL which is active H. With both methods, frequency acquisition takes place when the LOLCir determines an out of lock condition (LOL = H) for each CDR/RCLK, when the VCO frequency exceeds a given range (window). LOLCir enables the secondary P/FLL to drive the VCO close to the desired frequency (the input data bit rate). When the VCO falls within a given frequency range where the CDR/RCLK loop can acquire phase lock, LOLCir turns off the secondary P/FLL and sets LOL = L, allowing the CDR/RCLK to achieve phase lock. During this time, LOLCir continues to monitor the frequency difference and will signal a LOL = H to start the acquisition routine again; if the frequency falls out of range. The LOLCir range is fixed in hardwired mode, and programmable in 2-wire or 4-wire serial interface mode. In general, the frequency threshold (window) for LOL = H-to-L and LOL = L-to-H are different to prevent LOL from toggling when the frequency is near one of the windows. These registers also control the frequency acquisition time. Suggested values are given in this document for general robust operation, and are used as register defaults, however, the programmability of the registers allow for optimization based on a given application (e.g. faster lock times).

1.1.15 General CDR/RCLK Features

The CDR/RCLK is reset upon ***xRST = L***, *Mastreset* = AAh, or upon power up. A soft reset through *RCLK_ctrlA* [3] = 1b resets the CDR/RCLK state machine, and presets the CDR/RCLK to an out-of-lock condition, however, the register contents that are related to CDR/RCLK setup are unchanged. It is required to force a soft reset if the bit rate is dynamically changed. The soft reset register bit needs to be cleared for proper operation. In general, a reset during operation will cause bit errors, until the CDR/RCLK achieves phase lock.

By default, the CDR/RCLK is active and powered up for normal operation. By setting *RCLK_ctrlB* [7:6] = 11b, the CDR/RCLK can be bypassed and powered down, to allow for nonstandard bit rates, or to save power when the CDR/RCLK is not required at lower bit rates. When *RCLK_ctrlB* [7:6] = 01b, the CDR/RCLK is bypassed so the output data is not retimed but active (VCO locked to the input data). In the last mode with *RCLK_ctrlB* [7:6] = 10b, the CDR/RCLK is powered down, and all signals along the input and output paths are also powered down, to save power. In this case, the input data does not reach the output.

To prevent the propagation of noise in the case where there is a LOL condition, the CDR/RCLK contains an auto-inhibit feature, which is enabled by default. When LOL is active, the output of the CDR/RCLK is fixed at a logic high state (***DoutP*** = H, ***DoutN*** = L). This feature can be disabled by setting *RCLK_ctrlA* [3] = 0b, which allows *RCLK_ctrlA* [5] to either force an inhibit (1b) or to never inhibit (0b).

In some applications, the optimal data sampling point is not in the middle of the data eye. By default, the CDR/RCLK achieves phase lock very near the center of the eye. For optimal performance (jitter tolerance), the actual sampling point can be adjusted with *Phadj_ctrl* [3:0]. The adjustment range is from -122.5 mUI to +122.5 mUI with 17.5 mUI steps.

1.1.16 Multirate CDR Data Rate Selection

For multirate operation, the first step is to determine the desired data rate range. The input data range must be bracketed by $DF_{min} = F_{vco,\ min}/DRD_{max}$ to $DF_{max} = F_{vco,\ max}/DRD_{min}$. $DF_{max/min}$ are the maximum/minimum input data rate frequencies, $DRD_{max/min}$ are the maximum/minimum data rate divider settings using *CDR_ctrlB* [3:0], and $F_{vco,\ min}/F_{vco,\ max}$ are the minimum/maximum VCO frequencies, which are 2.0 GHz and 3.2 GHz respectively. The valid data rates are shown in Table 1-11.

Table 1-11. Valid Input Data Ranges

Parameter	DF_{min}	DF_{max}	Units
Data rate divider (DRD = 1): *CDR_ctrlB* [3:0] = 0000b	2.0	3.2	GHz
Data rate divider (DRD = 2): *CDR_ctrlB* [3:0] = 0001b	1.0	1.6	GHz
Data rate divider (DRD = 4): *CDR_ctrlB* [3:0] = 0010b	500	800	MHz
Data rate divider (DRD = 8): *CDR_ctrlB* [3:0] = 0011b	250	400	MHz
Data rate divider (DRD = 12): *CDR_ctrlB* [3:0] = 0100b	166.7	266.66	MHz
Data rate divider (DRD = 16): *CDR_ctrlB* [3:0] = 0101b	125	200	MHz
Data rate divider (DRD = 24): *CDR_ctrlB* [3:0] = 0110b	83.33	133.33	MHz
Data rate divider (DRD = 32): *CDR_ctrlB* [3:0] = 0111b	62.5	100	MHz
Data rate divider (DRD = 48): *CDR_ctrlB* [3:0] = 1000b	42	66.66	MHz

It is important to note the difference between the VCO frequency (F_{vco}), and the data rate frequency (DF). F_{vco} is always between 2 GHz to 3.2 GHz, while DF is the divided down F_{vco} that matches the input data rate.

1.1.17 Frequency Acquisition

Frequency acquisition is enabled by the LOLCir when LOL = H (*Alarm_LOL* = H or ***xLOL*** = L). A secondary FLL attempts to lock the VCO to a frequency derived from the external reference. When the frequency is close to the desired frequency, LOLCir sets LOL = L and disables the secondary FLL, thus, the main CDR/RCLK PLL is free to phase lock to the incoming data. Although the main CDR/RCLK PLL can achieve frequency lock, the VCO frequency tuning range typically exceeds the CDR/RCLK PLL inherent acquisition range. This implies that the FLL needs to get the VCO within the CDR/RCLK PLL range. The loss of lock circuitry (LOLCir) is used to determine when the secondary FLL is active. The LOLCir consists of window detectors that constantly compare a scaled VCO frequency, to a frequency related to the external reference. When LOL = H the loop is out of lock, the FLL is activated until the frequency difference is within the narrow reference window (NRW). When LOL = L, the FLL is not engaged until the frequency exceeds the wide reference window (WRW). If a signal is not present, the FLL circuit will drive the VCO frequency to the NRW and turn off. Without data present, the VCO would then drift until the frequency difference exceeds the WRW, and repeat this cycle. To prevent this, by default, the FLL is activated with LOL = H and de-activated with LOL = L.

Figure 1-8. Block Diagram of Frequency Acquisition Circuits

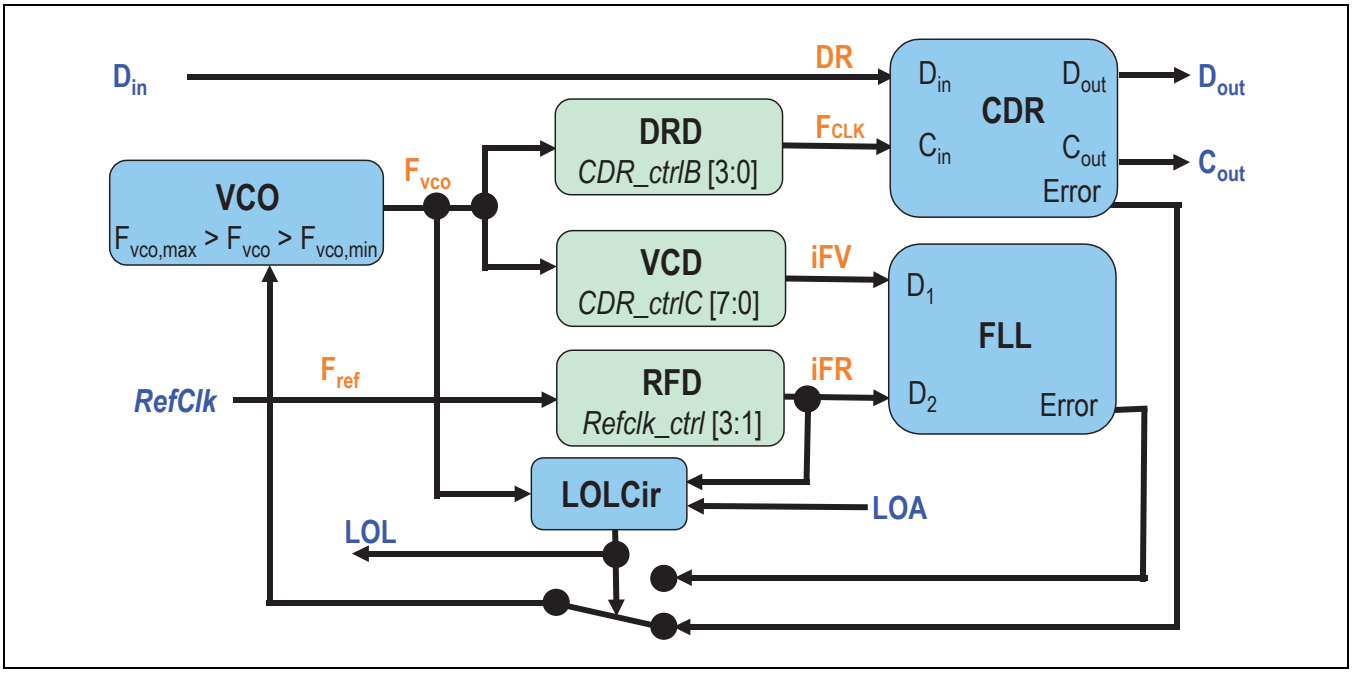


Figure 1-8 shows a block diagram of the frequency acquisition circuits. The secondary FLL compares a scaled version of the internal VCO frequency (iFV) with a scaled version of the reference clock frequency (iFR); iFR and iFV are limited to between 10 MHz and 25 MHz. The external reference clock frequency (F_{ref}) is applied to the ***RefClk*** [P/N] terminals. This reference frequency is scaled to the iFR by the reference frequency divider (RFD) [*Refclk_ctrl* [3:1]], which allows for an external reference clock in the range of 10 MHz to 800 MHz. The RFD level is a globally set value that applies to all CDR/RCLKs. Table 1-12 gives the divider ratio, along with the minimum and maximum F_{ref} values.

Table 1-12. Reference Clock Frequency Ranges

RFD Value	Minimum F_{ref} (MHz)	Maximum F_{ref} (MHz)
RFD (*Refclk_ctrl* [3:1] = 000b): divide by 1	10	25
RFD (*Refclk_ctrl* [3:1] = 001b): divide by 2	20	50
RFD (*Refclk_ctrl* [3:1] = 010b): divide by 4	40	100
RFD (*Refclk_ctrl* [3:1] = 011b): divide by 8	80	200
RFD (*Refclk_ctrl* [3:1] = 100b): divide by 12	120	300
RFD (*Refclk_ctrl* [3:1] = 101b): divide by 16	160	400
RFD (*Refclk_ctrl* [3:1] = 110b): divide by 32	320	800

The VCO frequency is scaled to the iFV by the VCO comparison divider (VCD) [*RCLK_ctrlC*_N [7:0]]. Table 1-13 provides DRD, RFD, and VCD values for common applications. For applications that only deal with SONET/SDH data rates, a 19.44 MHz reference clock frequency must be used. For applications where a combination of

SONET/SDH and other data rates are used, a 25 MHz reference clock frequency must be used. If either of these reference clock frequencies is not available, please contact MACOM Technologies Applications Engineering for other options.

Table 1-13. DRD/RFD/VCD Settings for Different Data Rates and Reference Frequencies (1 of 2)

Application	DR (Mbps)	Fref (MHz)	DRD	RFD	VCD	Notes
10GE - XAUI	3125	156.25	1	8	160	—
10GE - XAUI	3125	25	1	2	250	—
10GFC - XAUI	3187.5	159.375	1	8	160	—
10GFC - XAUI	3187.5	25	1	2	255	1
STS-48+FEC	2666.06	19.44	1	1	137	1
STS-48 + FEC	2666.06	25	1	2	213	1
STS-48	2488.32	155.52	1	8	128	—
STS-48	2488.32	19.44	1	1	128	—
STS-48	2488.32	25	1	2	199	1
2GFC	2125	106.25	1	8	160	—
2GFC	2125	25	1	2	170	—
GE	1250	125	2	8	160	—
GE	1250	25	2	2	200	—
FC	1062.5	106.25	2	8	160	—
FC	1062.5	25	2	2	170	1
STS-12	622.08	19.44	4	1	128	—
STS-12	622.08	25	4	2	199	1
FC	531	25	4	2	170	1
FC	266	25	12	2	255	1
ESCON	200	10	12	1	240	—
ESCON	200	25	12	2	192	—
STS-3	155.52	19.44	16	1	128	—
STS-3	155.52	25	16	2	199	1
FC	133	25	24	2	255	1
FE	125	12.5	16	1	160	—
FE	125	25	24	2	240	—
STS-1	51.84	25	48	2	199	1

Table 1-13. DRD/RFD/VCD Settings for Different Data Rates and Reference Frequencies (2 of 2)

Application	DR (Mbps)	Fref (MHz)	DRD	RFD	VCD	Notes
STS-1	51.84	19.44	48	1	128	1
DS3	44.736	25	48	2	172	1

NOTES:

1. Set *LOL_ctrl*_N[0] = 1b, all other bits at default values.

The FLL drives the iFV to iFR, and it is the primary function of the LOLCir to determine when to turn off the FLL, so the CDR/RCLK can achieve phase lock. The LOLCir uses the frequency difference between iFV and iFR to switch LOL, which turns on and off the secondary FLL. The thresholds where LOL makes a transition are defined as windows. These windows are fixed in the hardwired mode, and programmable in the two-wire interface mode. To prevent LOL from toggling at the thresholds, two windows are used for hysteresis. When LOL = L and the frequency difference exceeds the larger window (WRW), LOL L-to-H occurs to signal an out of lock case. When LOL = H (and LOA = L), the frequency difference is brought within the narrow reference window (NRW), after which LOL makes a H-to-L transition signaling in-lock. If LOA = H when LOL = L, the FLL remains on to keep the VCO locked to the reference, until a signal is present. N_{acq} is defined with *LOL_ctrl* [7:5], N_{narrow} is defined with *LOL_ctrl* [4:1], and N_{wide} is defined with *LOL_ctrl* [0]. The LOLCir averages a large number of transitions before making an LOL decision. This averaging time is referred to as the LOL decision time or DT_{LOL}.

Table 1-14 shows various window sizes for different applications, including the default value in both the hardwired and two-wire serial interface modes.

Table 1-14. LOL Window Size and Decision Time Examples

Condition	N_{acq}	N_{narrow}	N_{wide}	Narrow Window (ppm)	Wide Window (ppm)	Decision Time (µs)
Hardwired mode default	101b	0100b	0b	±1955	±2930	420
Two-wire serial interface mode default	101b	0100b	0b	±1955	±2930	420
iFV = iFR	111b	0010b	1b	±245	±975	1685
Fast lock	010b	0001b	0b	±5860	±7800	56

NOTES:

1. Decision time is calculated with iFR = 19.44 MHz; will scale proportionally with iFR range from 10 to 25 MHz.
2. Above are examples showing ability to tailor windows for data rates, reference frequencies, and acquisition times.

1.1.18 CDR/Reclocker Data Rate Programming (HD/SD-SDI data rates only)

If the automatic rate detection (ARD) algorithm developed by MACOM is used, it is not necessary for the user to manually program the registers of the reclockers to configure the reclockers for operation at a specific data rate. In applications where the ARD is not implemented and the device is used with software control, there are a few parameters that must be configured for the reclocker to correctly lock to the input data. The parameters that need to be programmed are the data rate divider (DRD) and the VCO frequency divider (VCD). The DRD is programmed

using bits [3:0] of register address 41h. The VCD is programmed using bits [7:0] of register address 42h. The following table shows the recommended values of DRD and VCD for standard video data rates.

Table 1-15. Recommended Values of DRD and VCD for Standard Video Data Rates

Data Rate (Mbps)	DRD Value	VCD Value	Fref (MHz)
143	05h	BFh	12
177	04h	B1h	12
270	03h	B4h	12
360	03h	F0h	12
540	02h	B4h	12
1483.5/1485	01h	F7h	12
2967/2970	00h	F7h	12

1.1.19 Ambient Temperature Range Limitations

Table 1-16 summarizes the supported ambient temperature range as a function of data rate, and indicates when it is required to center the VCO.

Table 1-16. Supported Ambient Temperature Range by Data Rate

F_{VCO} (GHz)	DR (Gbps)	T_a (°C)	VCO Centering Requirement
2.0–2.666	2.0/DRD–2.666/DRD	-40–85	N
2.7–2.97	2.7/DRD–2.97/DRD	0–70	N
2.7–2.97	2.7/DRD–2.97/DRD	-40–85	Y
3.0–3.2	3.0/DRD–3.2/DRD	0–70	Y

F_{VCO} is the VCO frequency, which always lies in the range 2.0–3.2 GHz. DR is the data rate of the input signal, and DRD is the data rate divider (1, 2, 4, 8, 12, 16, 24, 32, 48) set with *rclk_ctrlB*_N[3:0]. T_a is the ambient temperature supported, which decreases for F_{VCO} > 2.666 GHz. As an example, if the data rate is 800 Mbps DRD should be set to 4; to lock to this signal the VCO needs to operate at 3.2 GHz. Under these conditions the ambient temperature range supported is 0°C–70°C, and it is necessary to center the VCO in each of the four lanes.

The VCO tuning range is roughly the same bandwidth as the variation in VCO center frequency between the extremes of the operating temperature range. This issue can be resolved by centering the VCO frequency during the in-circuit testing (ICT) phase prior to shipment of the customer systems.

NOTE: The CDR/RCLK must be powered up and configured at 25°C–40°C ambient temperature during ICT.

1. Power up the device and configure the registers via the serial interface with the appropriate settings for the application of interest.
2. Read and store the VCO trim code from register MBh[4:0].
3. Every time the device is powered up, this trim code must be forced by setting M0h[0] = 0b then writing the code to MAh[4:0]. This can be done during the same write cycle as when the other registers are configured.

It should be noted that it is not possible to center the VCO in the hardwired mode, it is necessary to program the CDR/RCLK using the serial interface.

1.1.20 Loss of Activity

By default, the LOA detector is enabled and can be disabled by setting *CDR_ctrlA*_N [1] = 0b, where N is the channel number. Loss of activity measures the transition density of data to determine if the data is valid. With PRBS data, the transition density is typically 50%, averaged over long periods. During small time intervals, data transition density variations are due to data content, packet headers, stress patterns, etc. In some applications, when data is not present, noise produces rail-to-rail transitions that cause problems with level based detectors. These applications include cascaded reclockers, high-gain crosspoints, and other devices. The data transition density based LOA detector can separate data from random noise, determine false lock at the wrong integer and non-integer data rate, signal stuck high/low conditions, and determine false lock to retimed noise. Unlike level based detectors, it cannot determine false lock with low amplitude data.

1.1.21 Built-In Self Test (BIST) Overview

The M21262 contains a BIST test pattern generator as well as a test pattern receiver. Both the BIST transmitter (BIST Tx), and BIST receiver (BIST Rx) are designed to operate with fixed patterns. For PRBS evaluation, the PRBS 2^7-1, 2^{15}-1, 2^{23}-1, and 2^{31}-1 test patterns are provided. For 8b/10b testing, the fibre channel CRPAT and CJTPAT standard patterns are supported. In addition, an 8b/10b countdown pattern is also provided; this is the 8b/10b representation of a binary count from 255 to 0, while maintaining 8b/10b running disparity requirements. User programmable 16 bit (PRBS) and 20 bit (8b/10b) patterns are also provided; they are typically used to generate short patterns for debug, such as 1100b, as well as 8b/10b idle or control characters. The BIST is designed to reduce system development time, as well as product test costs, and can be used by both the equipment provider as well as the equipment end user.

When enabled, the BIST Rx allows one input from the M21262 to enter the BIST receiver. The desired channel to monitor is selected through a control register. The BIST Rx uses the recovered clock and data from the selected CDR/RCLK to drive the pattern checker. Every time a bit error is received, the error register is incremented. The maximum number of errors is FFh, and all subsequent errors will not be counted. At any time, the error register can be cleared. By keeping track of the time between a clear and a read, a rough BER number can be obtained.

When enabled, the BIST Tx can output a test pattern to the M21262 output (the BIST Tx and Rx can be used at the same time). The BIST Tx contains an internal clock multiplier (PLL), that can take its input from either the external reference frequency, or from the same CDR/RCLK that is driving the BIST Rx (only in full-rate mode, DRD = 1).

1.1.22 BIST Test Patterns

The test pattern is selected with *BISTtx_ctrl* [5:2] for the transmitter, and *BISTrx_ctrl* [5:2] for the receiver.

The PRBS patterns generated by the unit are ITU-T 0.151 compliant, and summarized in the table below.

Table 1-17. BIST PRBS Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**	**Polynomial**
0000b	PRBS 2^7-1	2^7+2^6+1
0001b	PRBS 2^{15}-1	$2^{15}+2^{14}+1$
0010b	PRBS 2^{23}-1	$2^{23}+2^{18}+1$
0011b	PRBS 2^{31}-1	$2^{31}+2^{28}+1$

For 8b/10b data, three patterns are available. The CJTPAT and CRPAT comply with the Fibre Channel T11.2/ Project 1230/Rev10 specifications.

Table 1-18. BIST 8b/10b Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**
0100b	CJTPAT
0101b	CRPAT
0110b	Countdown

Two user programmable patterns that are 16 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 0111b) and 20 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 1000b) are determined with *BIST_pattern0*, *BIST_pattern1, BIST_pattern2*. Note that the contents of these registers is used by both the BIST Tx and the BIST Rx, if they are setup in this mode.

1.1.23 BIST Receiver (BIST Rx) Operation

The BIST Rx is enabled and powered up by setting *BISTrx_ctrl* [1] = 1b (off by default), resetting the BIST Rx block with *BISTrx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTrx_ctrl* [5:2]. The signal to the BIST Rx is routed from the input of the device, and the BIST Rx can only check one channel at a time. The desired channel to monitor is selected with *BISTrx_chsel* [2:0]. The BIST Rx uses the recovered clock from the CDR/RCLK to drive the BIST state machine, thus the CDR/RCLK must be enabled and locked to data for proper operation. When the data is valid, *BISTrx_ctrl* [6] = 1b is used to clear the error register, and all subsequent errors can be read back through *BISTrx_error*. The BIST Rx automatically synchronizes the input data with the pattern.

1.1.24 BIST Transmitter (BIST Tx) Operation

The BIST Tx is enabled and powered up by setting *BISTtx_ctrl* [1] = 1b (off by default), resetting the BIST Tx block with *BISTtx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTtx_ctrl* [5:2]. The high-speed clock of the BIST Tx is generated from its own frequency multiplier PLL, that uses a selectable frequency reference determined by *BISTtx_ctrl* [6]. With *BISTtx_ctrl* [6] = 0b (default), the external reference clock is used and typically gives the lowest jitter output. With *BISTtx_ctrl* [6] = 1b the reference clock is derived from the same CDR/RCLK used to drive the BIST Rx (this feature only works with DRD = 1 for that CDR/RCLK). In this mode, the BIST Tx output is synchronous with the CDR/RCLK used in the BIST Rx, however, it contains the low-frequency jitter from the input data. In either case, the BIST Tx PLL needs to be configured for the proper data rate. When the PLL is properly