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M21350-15/M21355-15

3G/HD/SD-SDI Multi-rate Video Quad Reclocker

Rev V6

Applications

- 3G/HD/SD-SDI Video Switchers
- 3G/HD/SD-SDI Video Routers
- 3G/HD/SD-SDI Video Distribution Amplifiers
- DVB-ASI Equipment

Features

- Independent, quad channel, multi-rate reclocker
- SMPTE 259M-C, 292, 424M, and DVB ASI Compliant
- Greater than 0.6 UI Input Jitter Tolerance
- Integrated 50 Ω input termination
- 16x4 Input Crosspoint (M21355)
- Quad 4:1 Mux (M21350)
- Common reference clock for all channels
- Input equalization and output de-emphasis for 40" of FR4 trace
- 135 mW power consumption per channel (1.2 V operation)
- Integrated regulators for multi-voltage operation (1.2 V - 3.3 V)
- Electrically independent input, output, and core supply rails
- Recovered serial clock output option
- Output enable/disable and configurable auto or manual bypass mode
- Automatic and manual modes for rate indication and selection
- Loss of Lock (LOL), Loss of Signal (LOS) and data rate indication
- Two-wire and four-wire serial control interfaces
- Industrial operating temperature range (-40 °C to +85 °C)

The M21350 and M21355 are quad serial digital video reclockers with integrated trace equalization, and automatic rate detect (ARD) circuitry. The M21350 has a 4:1 mux on the input of each reclocker channel whereas the M21355 has a common 16x4 crosspoint switch at the input to all four channels. It operates at SDI data rates ranging from 270 Mbps to 2970 Mbps and is compliant to SMPTE 424M, SMPTE292, and SMPTE 259M-C. At 270 Mbps, it also supports DVB-ASI.

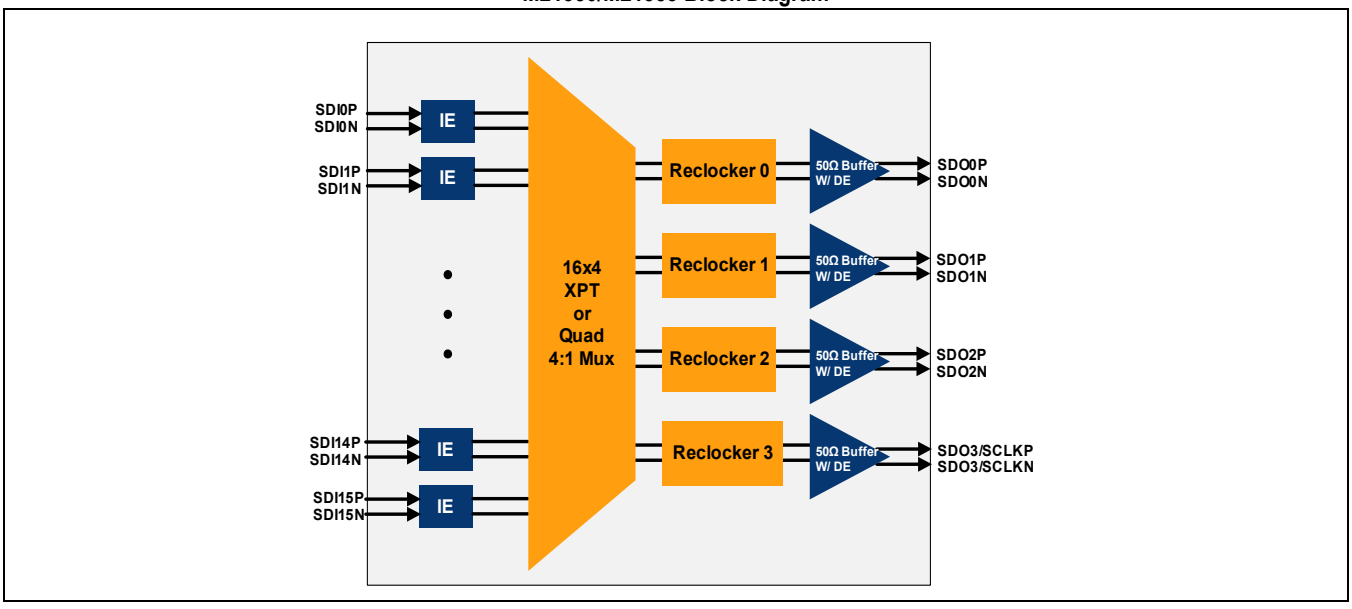
The M21350 and M21355 have an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial data outputs with very low alignment jitter. The quad reclockers require a single, external, 27 MHz crystal, which is used as the reference clock for all four channels. The devices also include per lane analog input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

These devices feature integrated supply regulators, allowing it to be powered from 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.2 V, it consumes only 135 mW per channel at 3G-SDI. Furthermore, the power rails for the core, input, and output circuitry are electrically independent and as such may be connected to different voltage rails on the board. This feature enables the M21350/M21355 to be DC coupled to any upstream or downstream device regardless of its input/output voltage level.

Each of the M21350's quad input MUXes allow any of the four inputs to be switched to the respective reclocker channel. The M21355's 16x4 input crosspoint allows any of the 16 inputs to be routed to any of the four integrated reclockers. The devices can be configured by setting the internal registers though standard two-wire and four-wire interfaces. Limited configuration is also possible through hardware pin settings.

The M21350 and M21355 are offered in a green and RoHS-compliant, 10 mm x 10 mm, 72-pin QFN packaging.

M21350/M21355 Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M21350G-15*	10 x 10 mm, 72-pin QFN package	-40 °C to 85 °C
M21355G-15*	10 x 10 mm, 72-pin QFN package	-40 °C to 85 °C
* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
V6	Release	December 2015	Updated package drawing, Figure 3-12 and Figure 3-13. Package effective as of August 2014.
V5	Release	June 2015	Updated logos and page layout. No content changes.
I (V4)	Release	June 2012	Section 4.6.2: Revised 4 wire interface. Revised register address 0Bh default to 08h.
H (V3)	Release	December 2011	Figure 3-1: Typo fixed in Pin 66, Pin 11 changed from DIN2P to SDI2P, Pin 12 changed from DIN2N to SDI2N. Table 4-2: Function description for pins MF4 and MF5 modified to make *low* equivalent to *floating*. Table 1-8: Added 2-state input to VIH and VIL. Section 4.7.1: Renamed SDOA to SDO0. Section 4.9.2: Inserted a note to add a 10 kΩ pull to AV_{DDIO}.

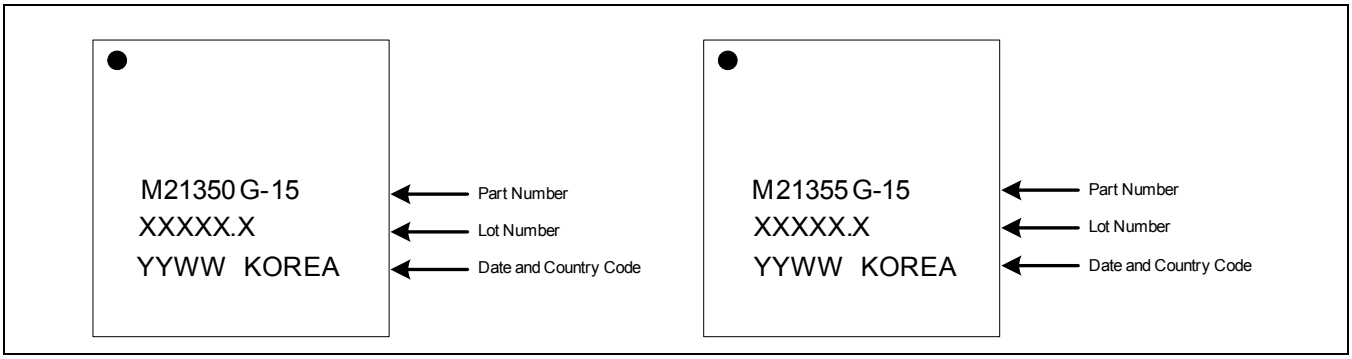
Revision History

Revision	Level	Date	Description
G (V2)	Released	February 2011	In the previous revision of this device, M21355/50G-14, the Loss of Lock (LOL) alarm would be erroneously triggered when pathological signals were used. As a workaround, MACOM recommended masking the faulty LOL alarm by setting register 96h bit[6] to 1b. In the latest version, M21355/50G-15, the faulty algorithm has been corrected. Therefore, the requirement to mask the LOL alarm has been removed from this data sheet. Please note that this change has been made to be fully backwards compatible, so setting register 96h bit[6] to 1b, while unnecessary, will not affect the function or performance of the device. Ordering Information: Updated part number from -14 to 15. Table 1-7: Updated XTAL and reference clock electrical specifications, input Impedance typical from to 400 kΩ to 200 Ω, input amplitude range from 1.6 V-2.0 V to 0.8 V to 1.2 V and max rise/fall times from 1 ns max to 2 ns typical and 6 ns max. Table 1-8: Updated V_{OH} from 0.75 to 0.80 x DV_{DDIO} and I_{OL} from 24 mA to 3 mA. Figure 3-1: Updated the pinout diagram to reflect new pin naming convention. Table 3-1: Updated table to reflect new pin naming convention. Table 5-1: Updated register map table. Added all registers needed to perform EEPROM checksum. Register 0Eh: Modified Interrupt mode xAlarm pulse widths to reflect their true value with respect to a 10K Ω pull up resistor. Register 82h: Updated chip version from 03h to 04h. Section 4.2: Included conditions necessary for self biased mode. Figure 4-4: Updated self bias diagram to reflect conditions necessary for self biased mode. Section 4.6.2: Updated to include the detailed timing description for four-wire interface when conducting a write operation followed by a read operation. Table 4-6: Updated the EEPROM addresses. Table 4-7: Updated the EEPROM addresses. Section 4.7.1: Clock Recovery: Updated the data to clock delay to 60 ps. Status for floating logic state for pin MF4 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Status for floating logic state for pin MF5 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Corrected pins 59, 58 to SDO3/SCLKP/N in Table 3-1. Changed MF4 and MF5 levels in Table 3-1. Added note to Figure 4-4. Changed MF4 and MF5 levels in Table 4-2. Changed MF3 function description in Table 4-5.
F (V1)	Released	May 2010	Revised all power consumption specifications in Table 1-3. Revised minimum and maximum values for V_{OUT} in Table 1-5. Revised typical and maximum values for t_R/t_F in Table 1-5. Revised typical and maximum values for J_{OUT} in Table 1-6. Revised bit values for 11h (Group Rate CTRL) register in Table 5-1. Revised bit values for 88h (Reclocker ALARMS) register in Table 5-1. Revised description field in Section 4.2. Revised bit 4 description for 11h (Reclocker Configuration). Revised description field 83h (LOS Status 0). Revised description field 84h (LOS Status 1). Revised description field 85h (Alarm Clear). Revised description field 88h (Reclocker Status Register). Revised bit 4 and 5 descriptions for 88h (Reclocker Status Register).
E (V1P)	Preliminary	March 2010	Refer to prior revision for details.
D (V4A)	Advance	November 2009	Combined M21350 and M21355 data sheets. Added M21350 register details in Section 5.0. Minimum input swing increased to 300 mV.
C (V3A)	Advance	May 2009	Removed M21350 and updated all sections.
B (V2A)	Advance	October 2008	Added chip outline and crystal capacitance.

Revision History

Revision	Level	Date	Description
A (V1A)	Advance	August 2008	Initial release.

M21350/M21355 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with DV_{DDO} = 1.2 V, AV_{DDCORE} = 1.2 V, DV_{DDCORE} = 1.2 V, AV_{DDI} = 1.2 V, CML inputs/outputs at 800 mV differential (R_{LOAD} = 50 Ω), and PRBS 2^{10} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	1, 3	-0.5	3.6	V
AV_{DDO}	Analog supply for output circuitry	1, 3	-0.5	3.6	V
DV_{DDIO}	Digital supply for input/output circuitry	1, 3	-0.5	3.6	V
DV_{DDCORE}	Digital core positive supply	1, 3	-0.5	1.5	V
AV_{DDCORE}	Analog core positive supply	1, 3	-0.5	1.5	V
T_{STORE}	Storage Temperature	1, 3	-65	150	°C
$V_{IN, CMOS}$	DC input voltage (CMOS)	1, 3	-0.5	DV_{DDIO}+0.5	V
V_{IN}	DC input voltage (PCML)	1, 3	-0.5	AV_{DDI}+0.5	V
$V_{ESD, HBM}$	Human Body Model (HBM)	1, 2, 3	-2	2	kV
$V_{ESD, CDM}$	Charge Device Model (CDM)	1, 2, 3	-500	500	V
LU	Latch Up @ 85 °C	1, 3	-150	150	mA
V_{IN}	Maximum High-speed input current	1, 3	-100	100	mA
$I_{OUT, PCML}$	Maximum High-speed output short circuit current	1, 3	-0.5	100	mA

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV_{DDIO}	Digital I/O positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDI}	Analog input positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDO}	Analog output positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDCORE}	Analog core positive supply	—	1.14	1.2	1.26	V
DV_{DDCORE}	Digital core positive supply	—	1.14	1.2	1.26	V
T_{CASE}	Case Temperature	—	-40	25	+85	°C

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Typical	Maximum	Unit
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 1	1	540	750	mW
		AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = 1.2V AV_{DDCORE}= 1.2 V SDO Swing Level 2	1	550	780	mW
		AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = 1.2V AV_{DDCORE}= 1.2 V AV_{DDO}= 1.8 V SDO Swing Level 3	1	650	880	mW
		AV_{DDI} = DV_{DDIO}= AV_{DDO}= 3.3 V AV_{DDCORE}/DV_{DDCORE} = N/A Internal regulators enabled SDO Swing Level 3	2	1740	2130	mW
θ_{JA}	Junction to Ambient Thermal Resistance		3	25	—	°C/W

NOTE:

1. Internal regulators disabled.
2. Internal regulators enabled.
3. Airflow = 0 m/s.

Table 1-4. SDI High Speed (Positive Current Mode Logic) Input Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDI input data rate	SD Operation (SMPTE 259M-C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	Mbps
		3G Operation (SMPTE 424M)		—	2970, 2967	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
V_{IN}	Differential input voltage	At the chip input (point blank) Input equalization disabled LOS enabled (80/90 setting)	1, 3	300	800	1600	mV_{PPD}
V_{ICM}	Input common mode voltage	At the chip input (point blank) Input equalization disabled LOS enabled		AV_{DDI}-0.6	—	AV_{DDI}+0.1	V
R_{IN}	Input Termination to AV_{DDI}			40	50	60	Ω
IE	Input Equalization		2	—	0, 2, 4, 6	—	dB

NOTE:

1. For example, 1200 mV_{PP} differential = 600 mV_{PP} for each single-ended terminal.
2. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
3. When using long traces and input equalization enabled, MACOM recommends a minimum input swing of 400 mV_{PPD}. With pathological patterns, DC coupling produces the best results.

Table 1-5. SDO High Speed (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDO output data rate	SD Operation (SMPTE 259M-C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	
		3G Operation (SMPTE 424M)		—	2970, 2967	—	
		Reclocker bypassed		18	—	3400	
F_{CLOCK}	Serial clock output frequency	SD Operation (SMPTE 259M-C)	1, 6	—	270	—	MHz
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	
		3G Operation (SMPTE 424M)		—	2970, 2967	—	
V_{OUT}	Differential Output Swing (peak to peak, differential)	Swing Level 1	2	470	600	720	mV_{PPD}
		Swing Level 2	2	600	800	970	
		Swing Level 3	2,3	960	1200	1500	
V_{OCM}	Output common mode voltage	DC coupled	2	—	AV_{DDO}-V_{OUT}/4	—	
t_R/t_F	SDO output Rise/Fall Time	From 20%-80% of the swing for all levels		—	85	130	ps
$t_R/t_{F\ DIFF}$	Rise/Fall Time Mismatch	From 20%-80% of the swing for all levels		—	—	30	ps
DCD_{DATA}	Output duty cycle distortion	For all data rates	4	—	—	15	ps
R_{OUT}	Output Termination to AV_{DDO}			40	50	60	Ω
DE	Output De-Emphasis		5	—	0, 2, 4, 6	—	dB

NOTE:

1. Serial clock output enabled.
2. Differential swing is maximum output level (De-emphasis is disabled or max level when de-emphasis is enabled), max level includes overshoot.
3. 1200 mV swing level requires AV_{DDO} to be 1.8 V or higher.
4. Measured in reclocked mode.
5. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
6. See Section 4.7 for information on clock data alignment.

Table 1-6. Reclocker Specifications *(See note below for Level B format)*

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
t_{LOCK}	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBWPEAK}$	Loop bandwidth peaking		1	—	0.1	—	dB
F_{LBW}	Loop bandwidth (nominal setting)	3G operation (2.97 Gbps)	1	—	1.7	—	MHz
		HD operation (1.485 Gbps)	1	—	0.85	—	
		SD operation (270 Mbps)	1	—	0.17	—	
J_{TOL}	Input jitter tolerance	3G, HD, and SD operation	2	>0.6	—	—	UI p-p
J_{GEN}	Total Output jitter	3G operation (2.97 Gbps)	2, 3	—	0.07	0.11	UI p-p
		HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

NOTE:

1. 0.2 UI input jitter applied at SDI input.
2. Measured with $PRBS2^{10}$-1.
3. Input jitter = 20 ps p-p.

Table 1-7. XTALP/N and Reference Clock Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
F_{REF}	XTAL/Ref clock frequency	3	—	27	—	MHz
$F_{REF, PPM}$	XTAL/Ref clock frequency accuracy	—	-100	0	100	ppm
C_{LOAD}	XTAL load capacitance	1	—	20	25	pF
$CLOCK_{JITT}$	Jitter (RMS)	2, 4	—	—	1	ps
$CLOCK_{DCT}$	Reference clock duty cycle tolerance	2	40	—	60	%
R_{IN}	Input impedance	2, 5	0.2	0.75	1.2	kΩ
V_{IN}	Input amplitude	2	0.8	—	1.2	V
t_R/t_F	Rise/Fall time	2, 6	—	2	6	ns

NOTE:

1. This capacitance is supplied internally (no external cap is required).
2. When using an external reference clock source, this should be AC coupled through a 0.1 µF capacitor.
3. When using an external clock a small increase in jitter may be seen. For best performance a crystal is recommended.
4. Jitter Bandwidth 12 kHz to 20 MHz.
5. Measured with Agilent TDR module.
6. 10% to 90% rise and fall times.

Table 1-8. Digital Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Output Logic High	1	0.80 x DV_{DDIO}	DV_{DDIO}	—	V
V_{OL}	Output Logic Low	2	—	—	0.2 x DV_{DDIO}	V
V_{IH}	Input Logic High	3, 5	0.85 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IF}	Input Logic Floating	3, 5	0.25 x DV_{DDIO}	—	0.75 x DV_{DDIO}	V
V_{IL}	Input Logic Low	3, 5	0	—	0.15 x DV_{DDIO}	V
V_{IH}	Input Logic High	4, 5	0.75 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IL}	Input Logic Low	4, 5	0	—	0.25 x DV_{DDIO}	V

NOTE:

1. I_{OH} = -3 mA
2. I_{OL} = 3 mA
3. 3- state input
4. 2- state input
5. Some inputs can be 2 or 3 state. Depending on which mode is selected the threshold levels will change accordingly.

2.0 Typical Performance Characteristics

Figure 2-1. Eye Diagram at Reclocker Input PRBS15 pattern@ 3 Gbps

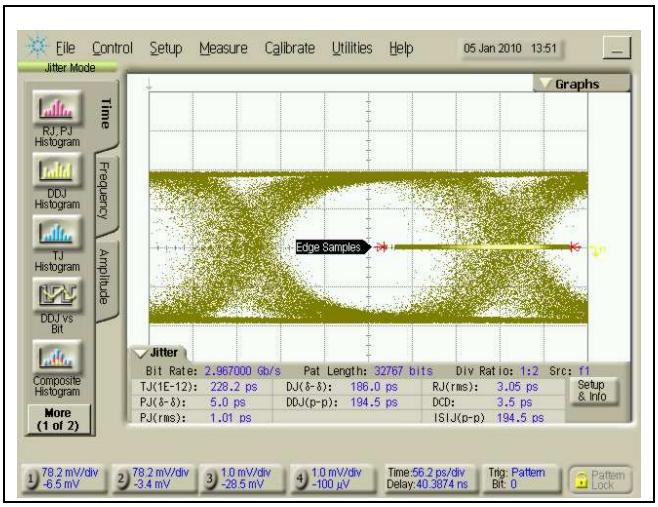
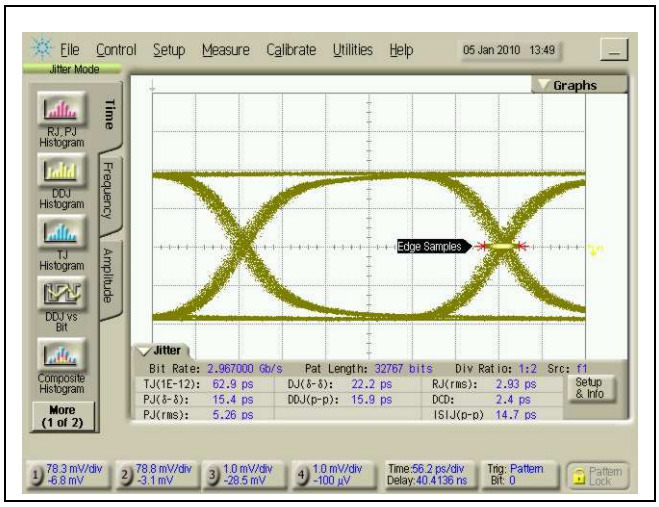


Figure 2-2. Eye Diagram at Reclocker Output PRBS15 pattern@ 3 Gbps



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

Figure 3-1. M21350/M21355 Pinout Diagram

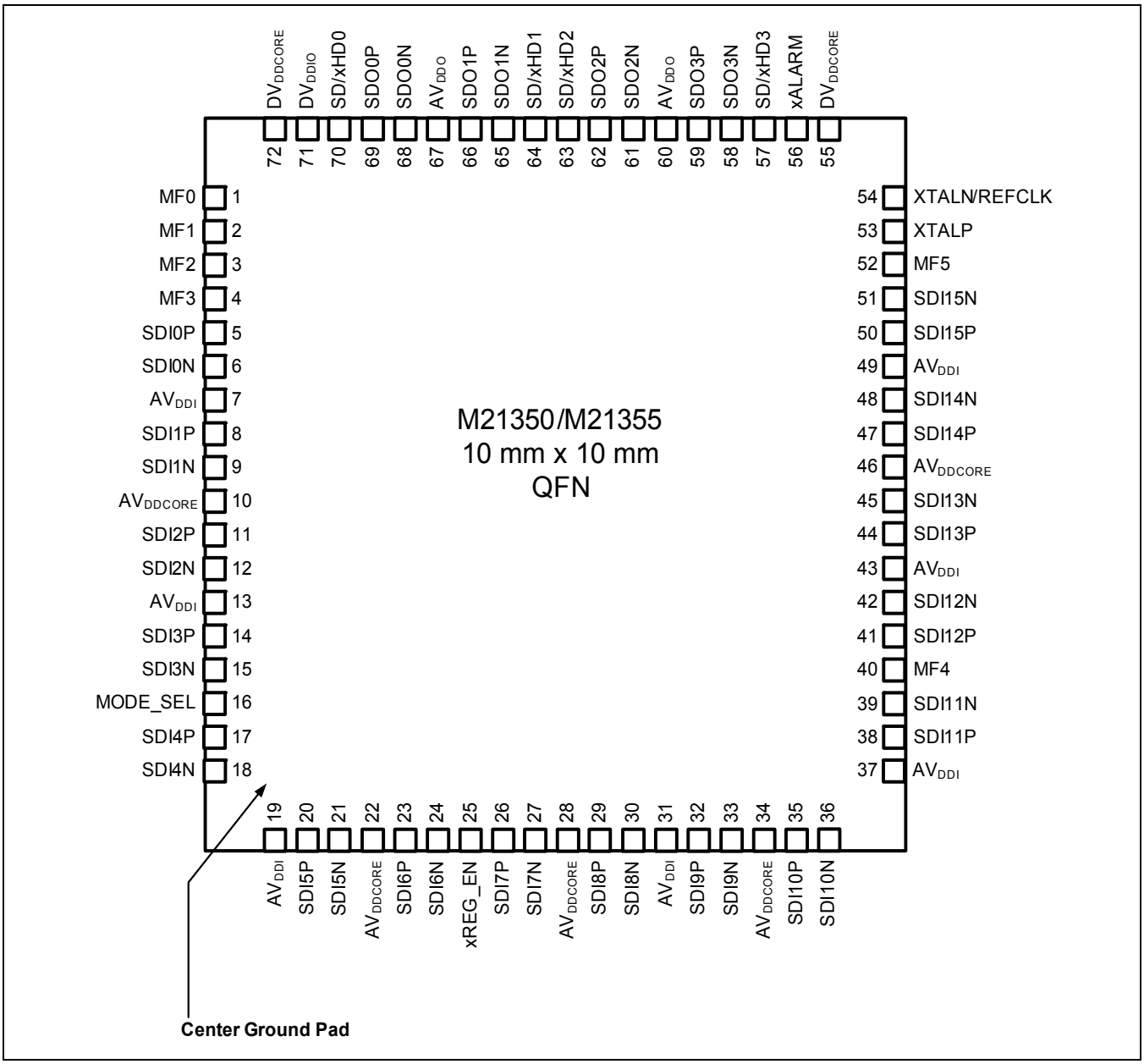


Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
AV_{DDCORE}	10, 22, 28, 34, 46	Power	Analog positive supply
AV_{DDI}	7, 13, 19, 31, 37, 43, 49	Power	Analog positive supply
AV_{DDO}	60, 67	Power	Analog positive supply
DV_{DDCORE}	55, 72	Power	Digital Core Positive Supply
DV_{DDIO}	71	Power	Digital Core Positive Supply
AV_{SS}	Center Ground Pad	Power	Ground
SDI0P, SDI0N	5, 6	PCML input	Data Input Lane0; true/complement
SDI1P, SDI1N	8, 9	PCML input	Data Input Lane1; true/complement
SDI2P, SDI2N	11, 12	PCML input	Data Input Lane2; true/complement
SDI3P, SDI3N	14, 15	PCML input	Data Input Lane3; true/complement
SDI4P, SDI4N	17, 18	PCML input	Data Input Lane4; true/complement
SDI5P, SDI5N	20, 21	PCML input	Data Input Lane5; true/complement
SDI6P, SDI6N	23, 24	PCML input	Data Input Lane6; true/complement
SDI7P, SDI7N	26, 27	PCML input	Data Input Lane7; true/complement
SDI8P, SDI8N	29, 30	PCML input	Data Input Lane8; true/complement
SDI9P, SDI9N	32, 33	PCML input	Data Input Lane9; true/complement
SDI10P, SDI10N	35, 36	PCML input	Data Input Lane10; true/complement
SDI11P, SDI11N	38, 39	PCML input	Data Input Lane11; true/complement
SDI12P, SDI12N	41, 42	PCML input	Data Input Lane12; true/complement
SDI12P, SDI13N	44, 45	PCML input	Data Input Lane12; true/complement
SDI14P, SDI14N	47, 48	PCML input	Data Input Lane14; true/complement
SDI15P, SDI15N	50, 51	PCML input	Data Input Lane15; true/complement
SDO0P, SDO0N	69, 68	PCML output	Data Output Lane0; true/complement
SDO1P, SDO1N	66, 65	PCML output	Data Output Lane1; true/complement
SDO2P, SDO2N	62, 61	PCML output	Data Output Lane2; true/complement
SDO3P/SCLKP, SDO3N/ SCLKN	59, 58	PCML output	Data Output Lane3; true/complement
XTALP	53	Reference Clock	27 MHz reference XTAL connection
XTALN/REFCLK	54	Reference Clock	27 MHz reference XTAL connection or 27 MHz reference clock input

Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
MODE_SEL	16	CMOS Control Input	Sets the device control/configuration mode: L = Device is in register access mode with two-wire serial control (SIC2) F = Device is in hardware control mode (Hardware Mode) H = Device is in register access mode with four-wire serial control (SIC4) Termination - F
xREG_EN	25	CMOS Control Input	Regulator enable control, as in Figure 3-6, but pull up resistor is to AV_{DDI}. L = Integrated regulators enabled F = Integrated regulators disabled Termination - H, 100 kΩ pull up to AV_{DDI}
SD/xHD0	70	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD1	64	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD2	63	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD3	57	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
xALARM	56	Output (Open Drain)	Alarm indicator for all channels (Logical OR of all individual channel alarms). Termination - Open L = Alarm asserted H = Normal operation Serial Control Mode (two-wire/four-wire) Mode: Reg0E = 00h, xALARM in interrupt mode Reg0Eh=08b, xALARM in status mode Hardware Mode: xALARM is in status mode
MF0	1	CMOS Control Input	Four-wire serial control Mode: Serial clock input (SCLK) Two-wire serial control Mode: Clock input from master host (SCL) Hardware Mode: Unused
MF1	2	CMOS Control Input	Four-wire serial control Mode: Serial data output (SO) Two-wire serial control Mode: Serial data I/O (SDA) Hardware Mode: Unused

Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
MF2	3	CMOS Control Input	Four-wire serial control Mode: Serial data in (SI) Two-wire serial control Mode: Address bit 0 (ADD0) Hardware Mode: Input trace equalization control for all SDI inputs (IE_CTRL) H = Large Input EQ F = Medium Input EQ L = Input EQ disabled
MF3	4	CMOS Control Input	Four-wire serial control Mode: Active low chip select (xCS) Two-wire serial control Mode: Address bit 1 (ADD1) Hardware Mode: Output de-emphasis (DE) control for SDO outputs (DE_CTRL) H = Large Output DE F = Medium Output DE L = DE disabled
MF4	40	CMOS Control Input	Four-wire serial control Mode: Not used. Tie to DV_{DDIO} or leave floating Two-wire serial control Mode: Address bit 2 (ADD2) Hardware Mode: Reclocker bypass control (RC_BYPASS) L/F = Normal operation, Reclocker not bypassed H = Reclocker bypassed
MF5	52	CMOS Control Input	Four-wire serial control Mode: Not used. Tie to AVSS or leave floating Two-wire serial control Mode: Address bit 3 (ADD3) Hardware Mode: SDO disable control for all outputs (SDO_DIS) H = SDO disabled output logic high L/F = SDO enabled

Figure 3-2. I-Analog

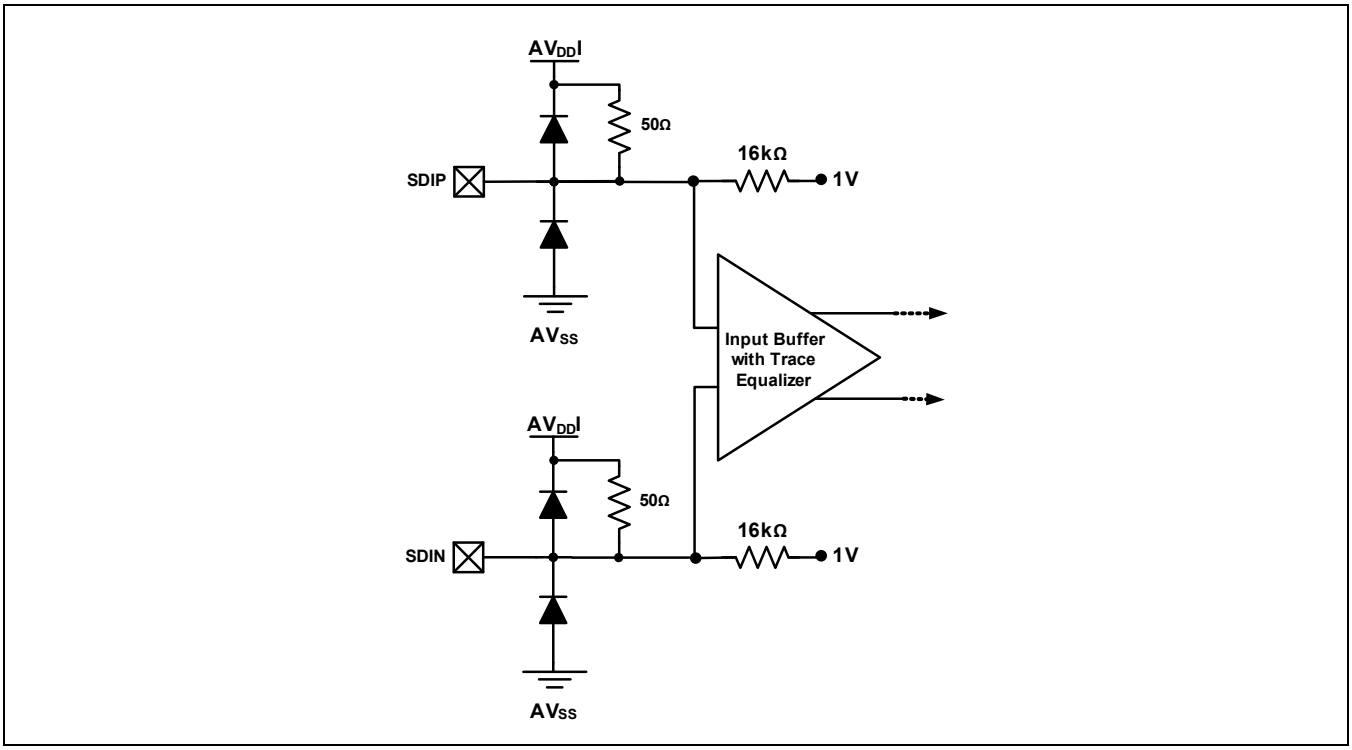


Figure 3-3. O-Analog

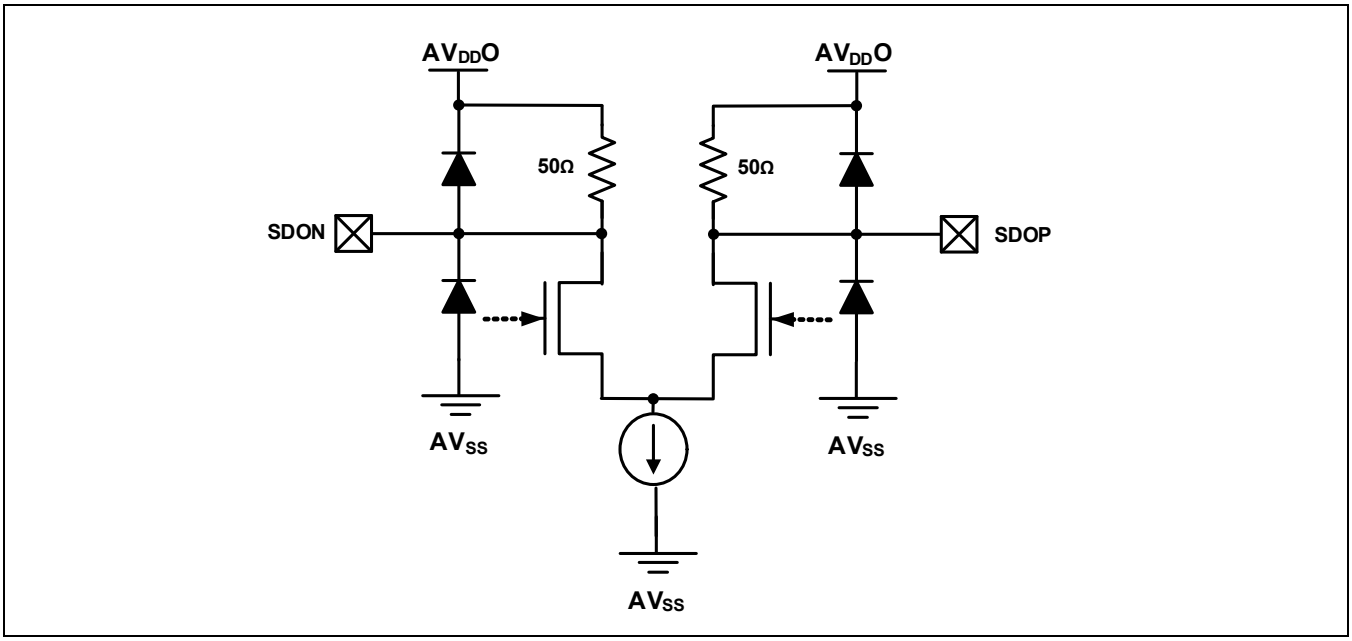


Figure 3-4. Ref Clock

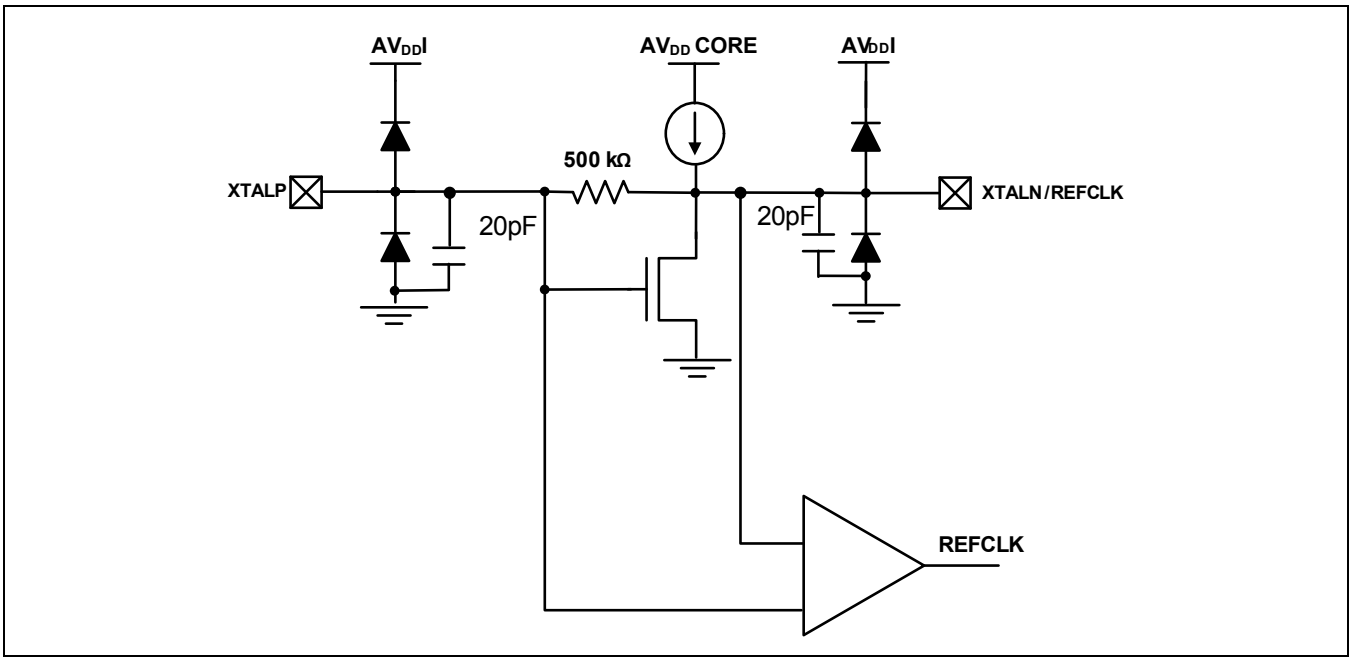


Figure 3-5. I-Digital With No Pull-up

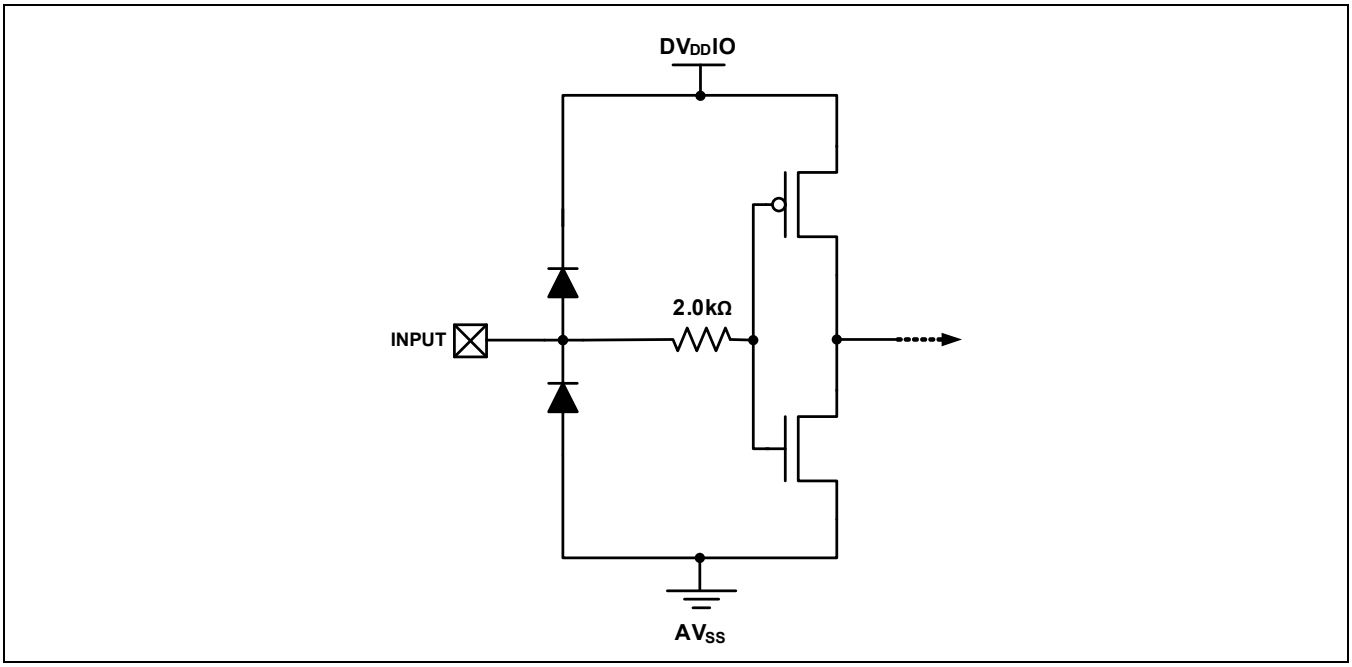


Figure 3-6. I-Digital With Pull-up

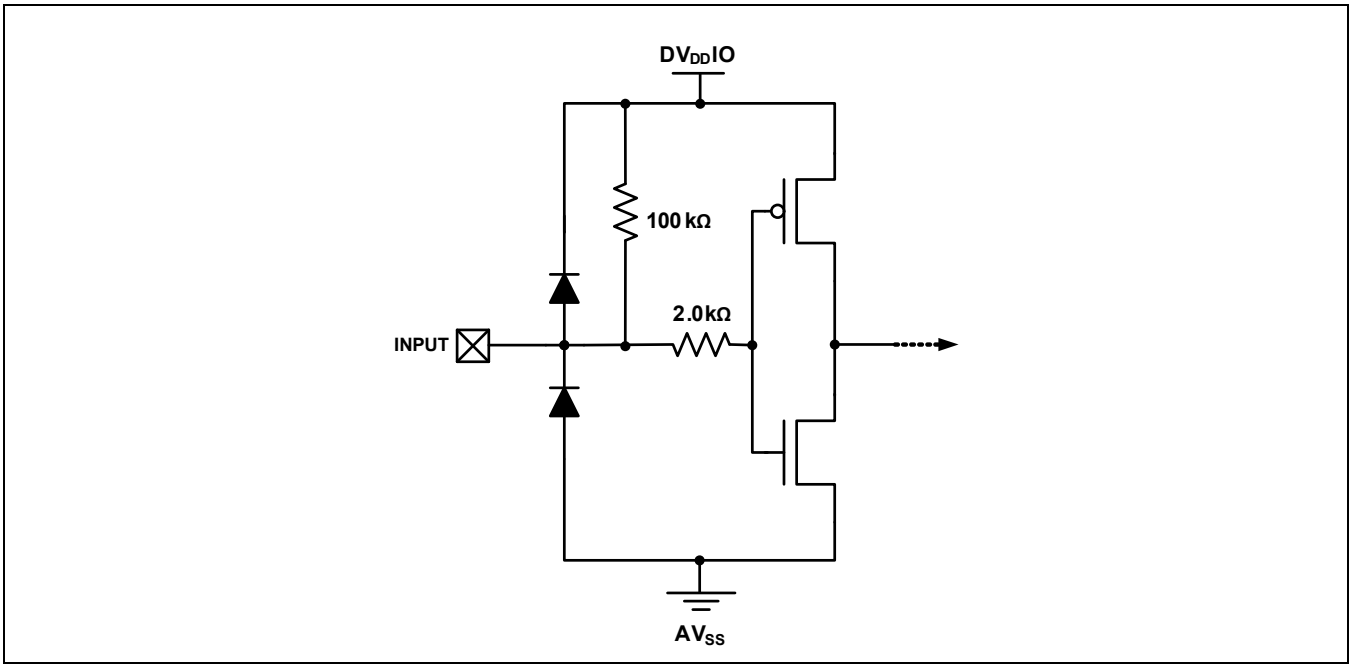


Figure 3-7. I-Digital With Pull-down

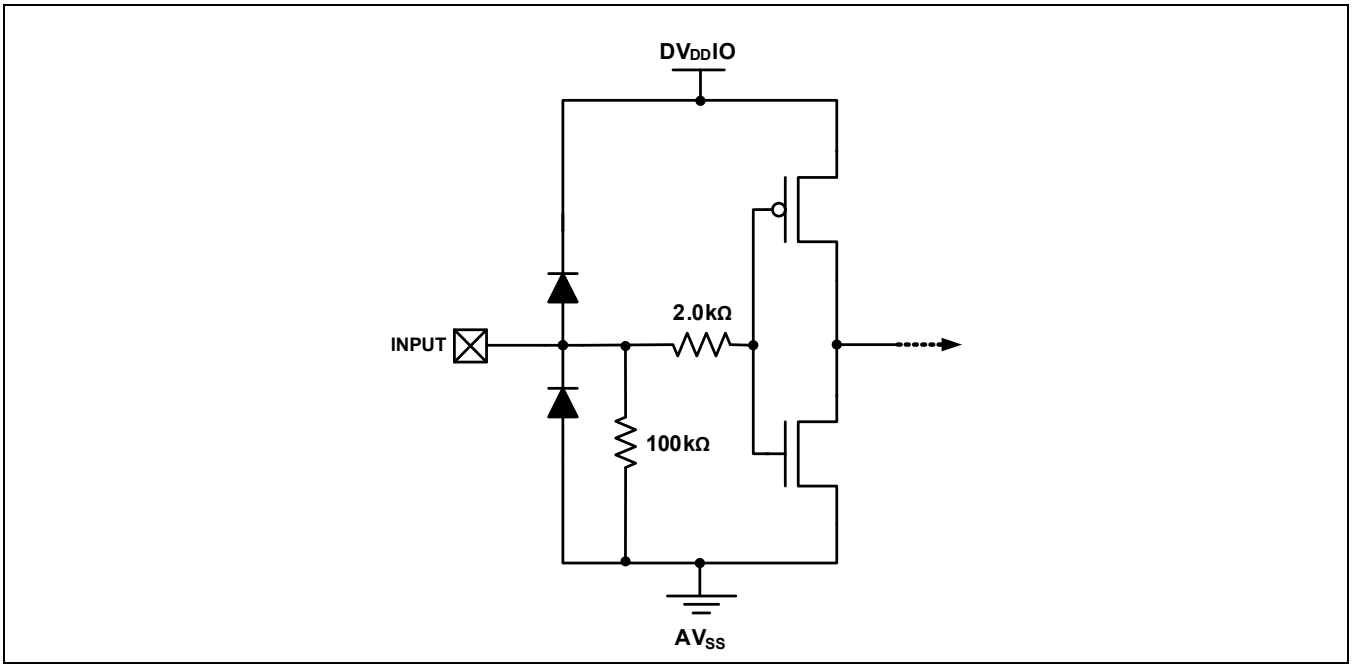


Figure 3-8. 3-State/I-Digital

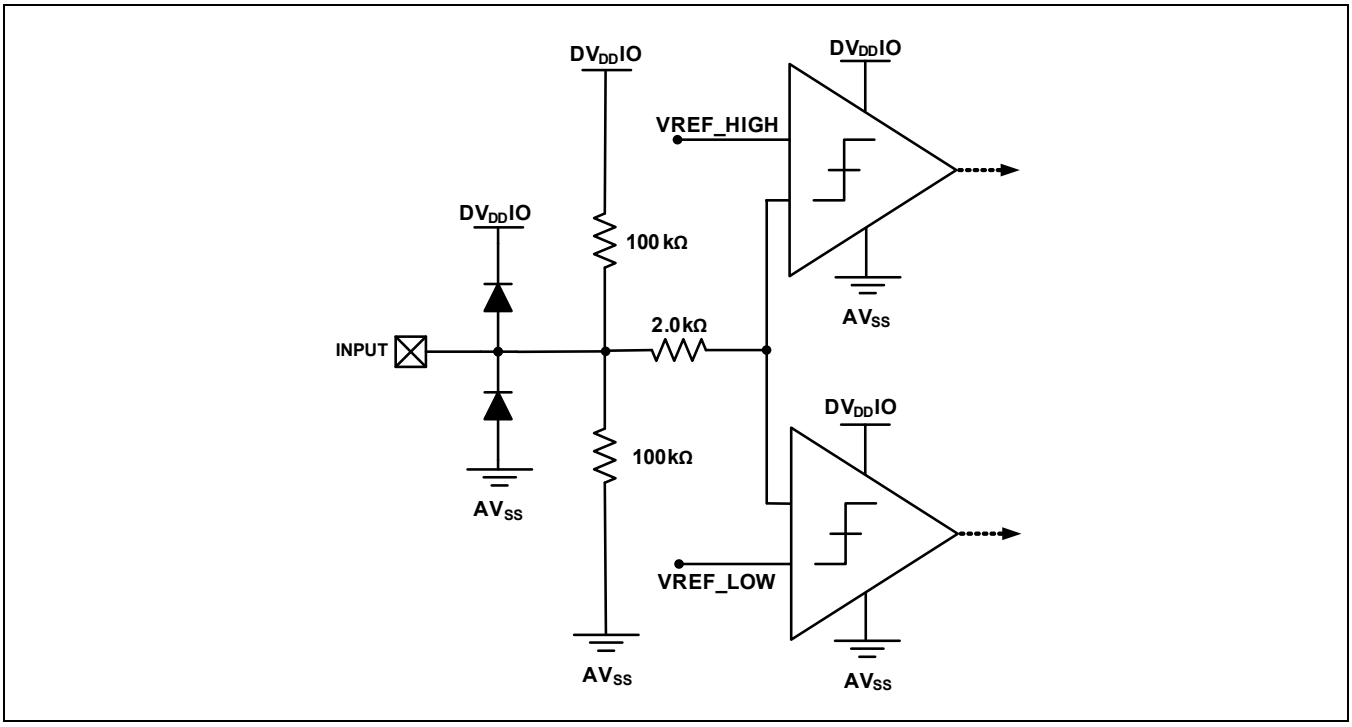


Figure 3-9. O-Digital

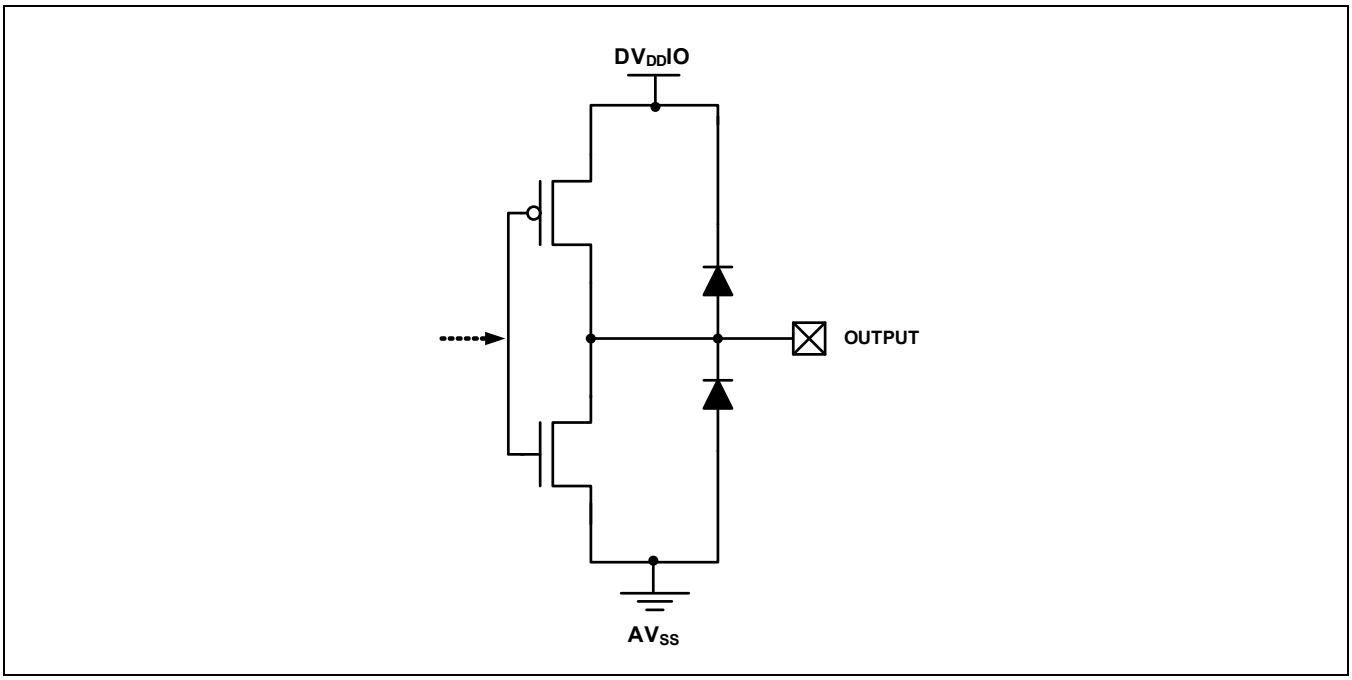
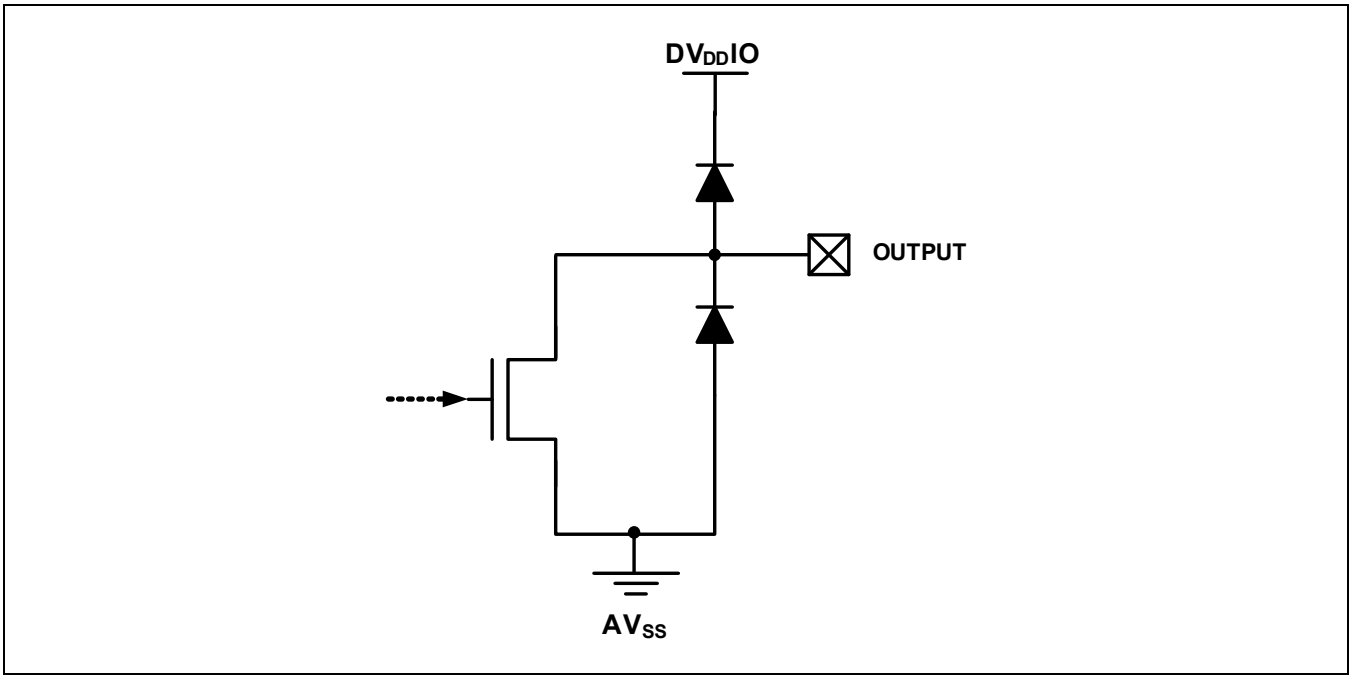


Figure 3-10. O-Open Drain



The M21350/M21355 is assembled in a 72-pin, 10 mm x 10 mm Quad Flat No-Lead (QFN) package. The exposed paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This paddle should be soldered to the PCB. A cross-section of the QFN package is shown below.

Figure 3-11. QFN Package Cross Section

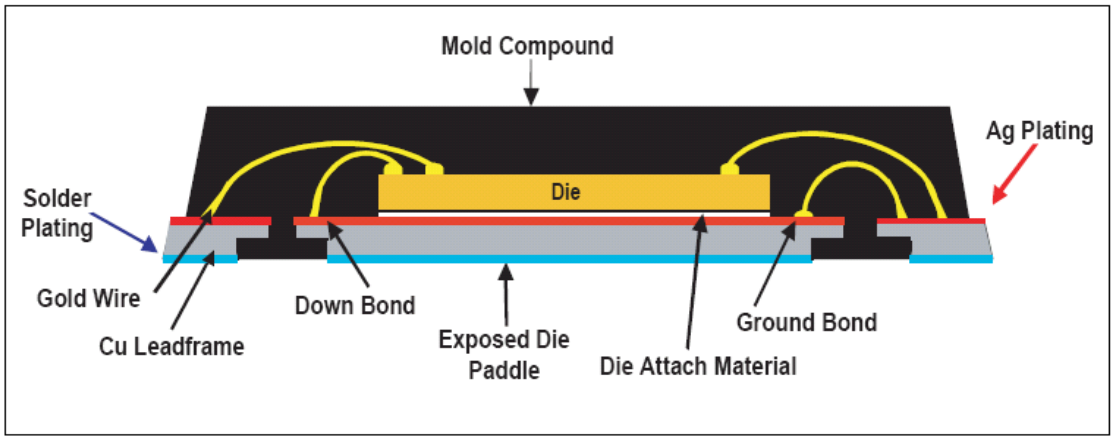
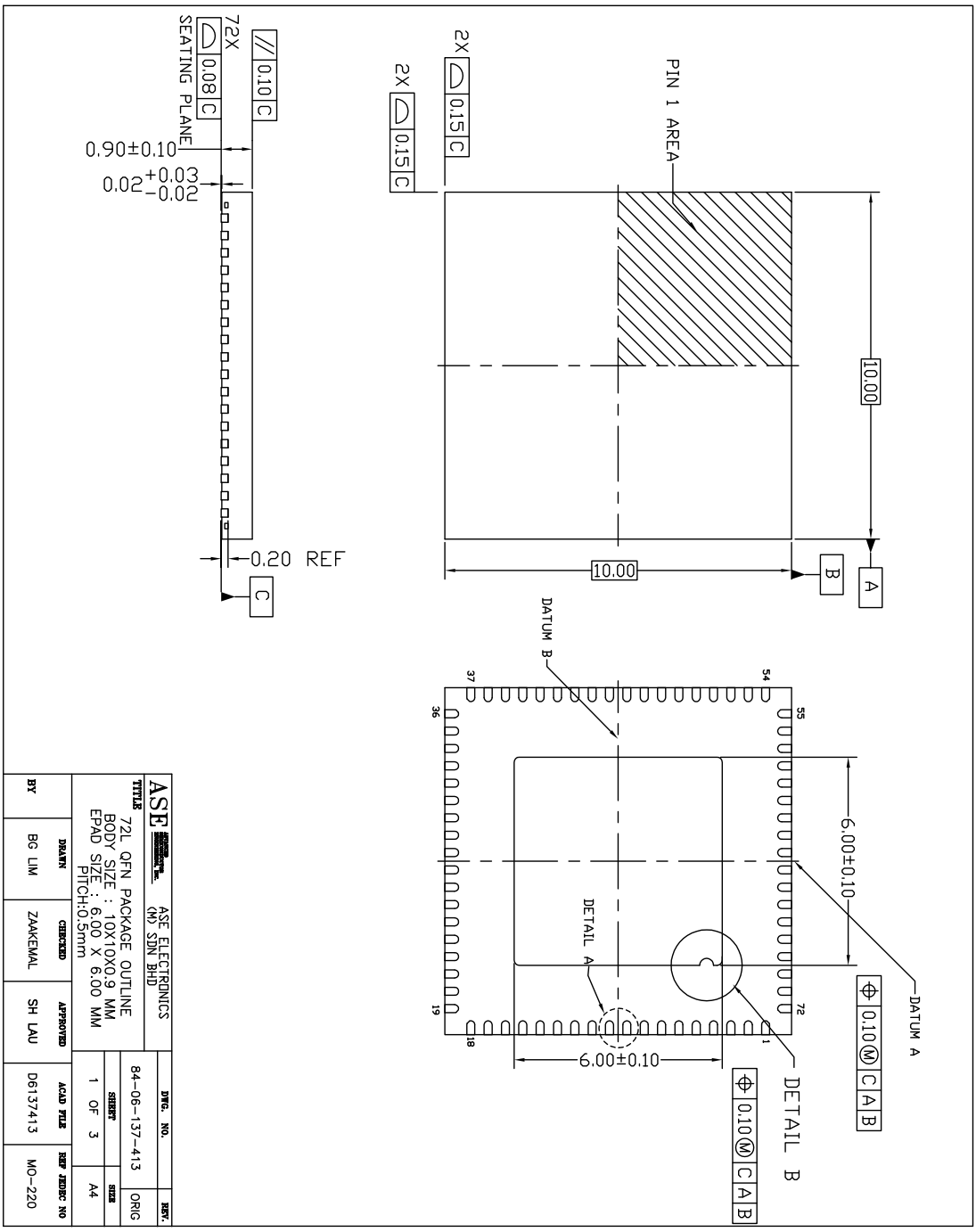
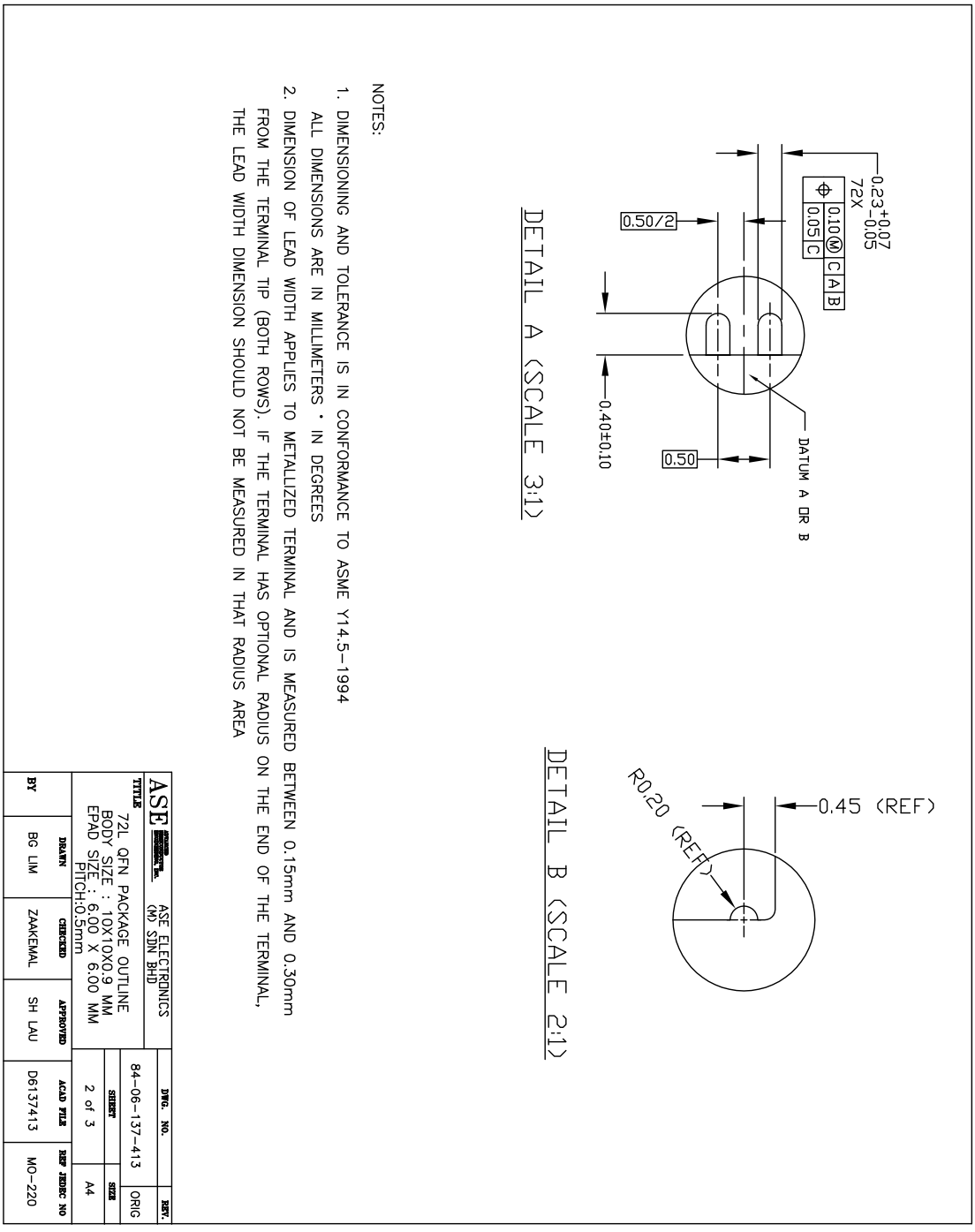


Figure 3-12. Package Outline Drawing



1. New Unisem package and old Amkor package have the same footprint dimensions.

Figure 3-13. 72-Pin QFN Package Dimensions



1. New Unisem package and old Amkor package have the same footprint dimensions.

4.0 Functional Description

4.1 Functional Block Diagram

Figure 4-1and Figure 4-2 illustrate the M21350 and M21355 block diagrams respectively. The subsequent sections provide additional detail on the operation of the devices.

Figure 4-1. M21350 Block Diagram

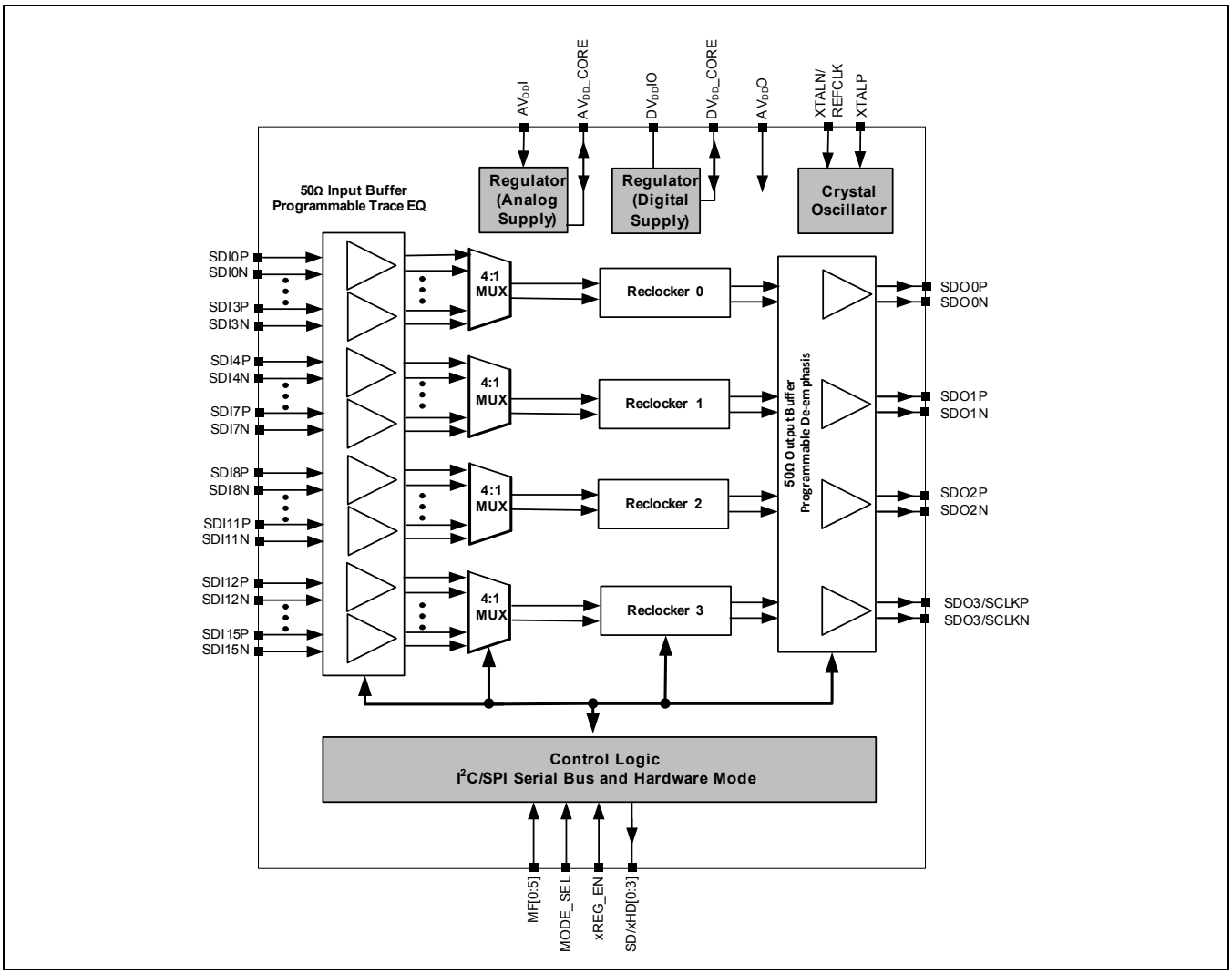


Figure 4-2. M21355 Block Diagram