Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

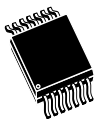
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

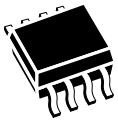
M24C04-DRE

4-Kbit serial I²C bus EEPROM - 105°C operation

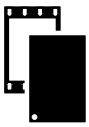
Datasheet - production data



TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width



WFDFPN8 (MF)
DFN8 - 2 x 3 mm

Features

- Compatible with all I^2C bus modes
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array
  - 4 Kbits (512 bytes) of EEPROM
  - Page size: 16 bytes
  - Additional Write lockable page (Identification page)
- Extended temperature and voltage range
  - -40 °C to 105 °C; 1.7 V to 5.5 V
- Schmitt trigger inputs for noise filtering
- Short Write cycle time
  - Byte Write within 4 ms
  - Page Write within 4 ms
- Write cycle endurance
  - 4 million Write cycles at 25 °C
  - 1.2 million Write cycles at 85 °C
  - 900 k Write cycles at 105 °C
- Data retention
  - more than 50 years at 105 °C
  - 200 years at 55 °C
- ESD Protection (Human Body Model)
  - 4000 V
- Packages
  - RoHS compliant and halogen-free (ECOPACK2®)

Contents

List of tables

List of figures

1 Description

The M24C04-DRE is a 4-Kbit serial EEPROM device operating up to 105 °C. The M24C04-DRE is compliant with the level of reliability defined by the AEC-Q100 grade 2.

The device is accessed by a simple serial I^2C compatible interface running up to 1 MHz.

The memory array is based on advanced true EEPROM technology (electrically erasable programmable memory). The M24C04-DRE is a byte-alterable memory (512 × 8 bits) organized as 32 pages of 16 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The M24C04-DRE offers an additional Identification Page (16 bytes) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

Figure 1. Logic diagram

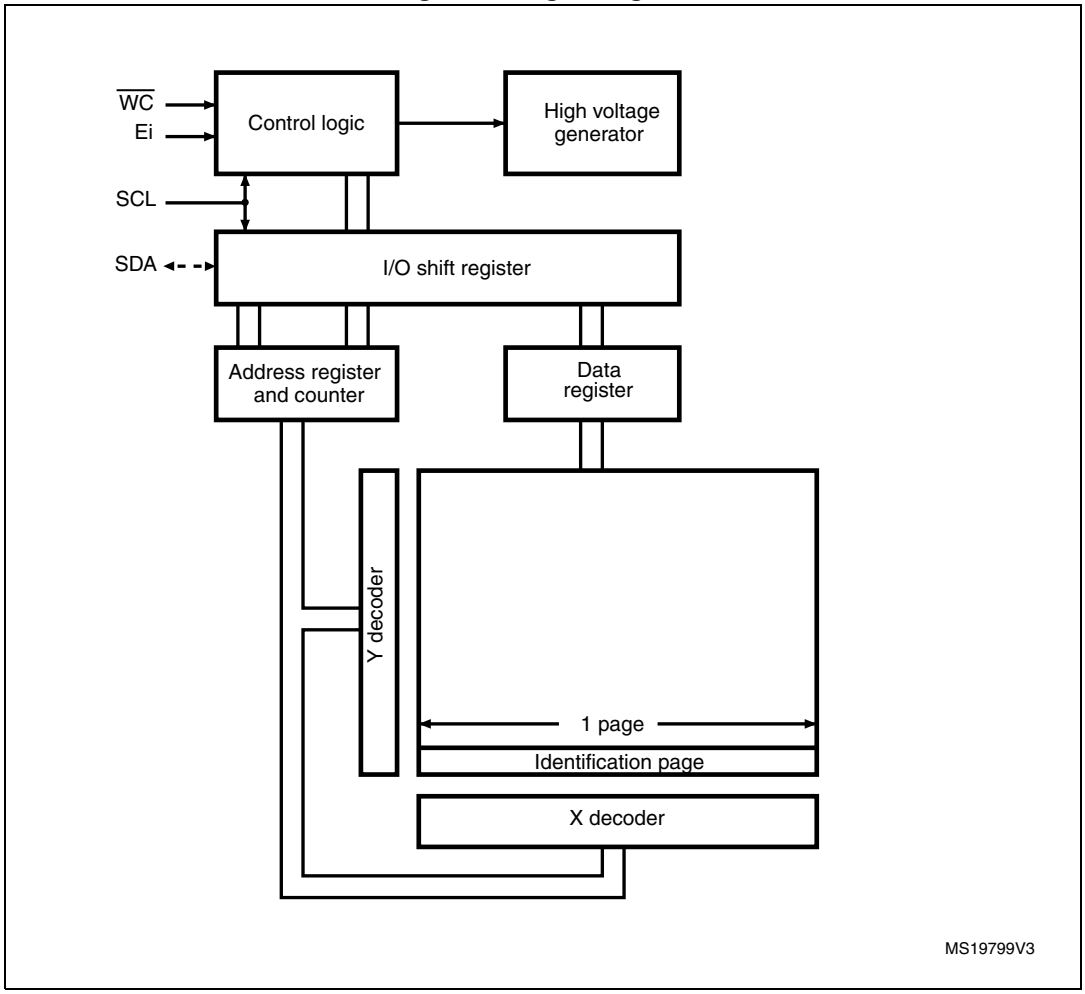
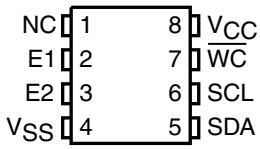


Table 1. Signal names

Signal name	Function	Direction
E2, E1	Chip enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connection



MS30991V1

1. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial Clock (SCL)

The signal applied on this input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

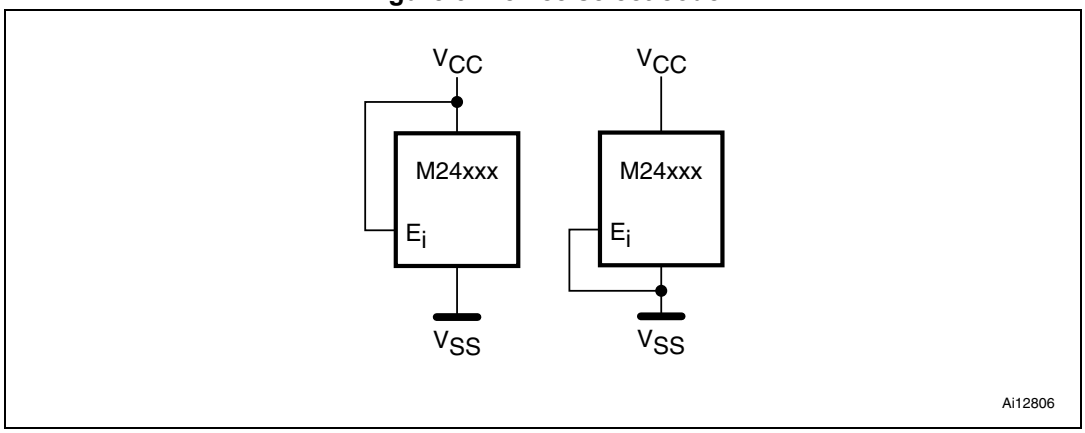
2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected between SDA and V_{CC} (*Figure 10* and *Figure 11* indicate how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1)

This input signals are used to set the value that is to be looked for on the two bits (b3, b2) of the 7-bit device select code (see *Table 2*). These inputs must be tied to V_{CC} or V_{SS} to establish the device select code, as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

V_{CC} is the supply voltage pin.

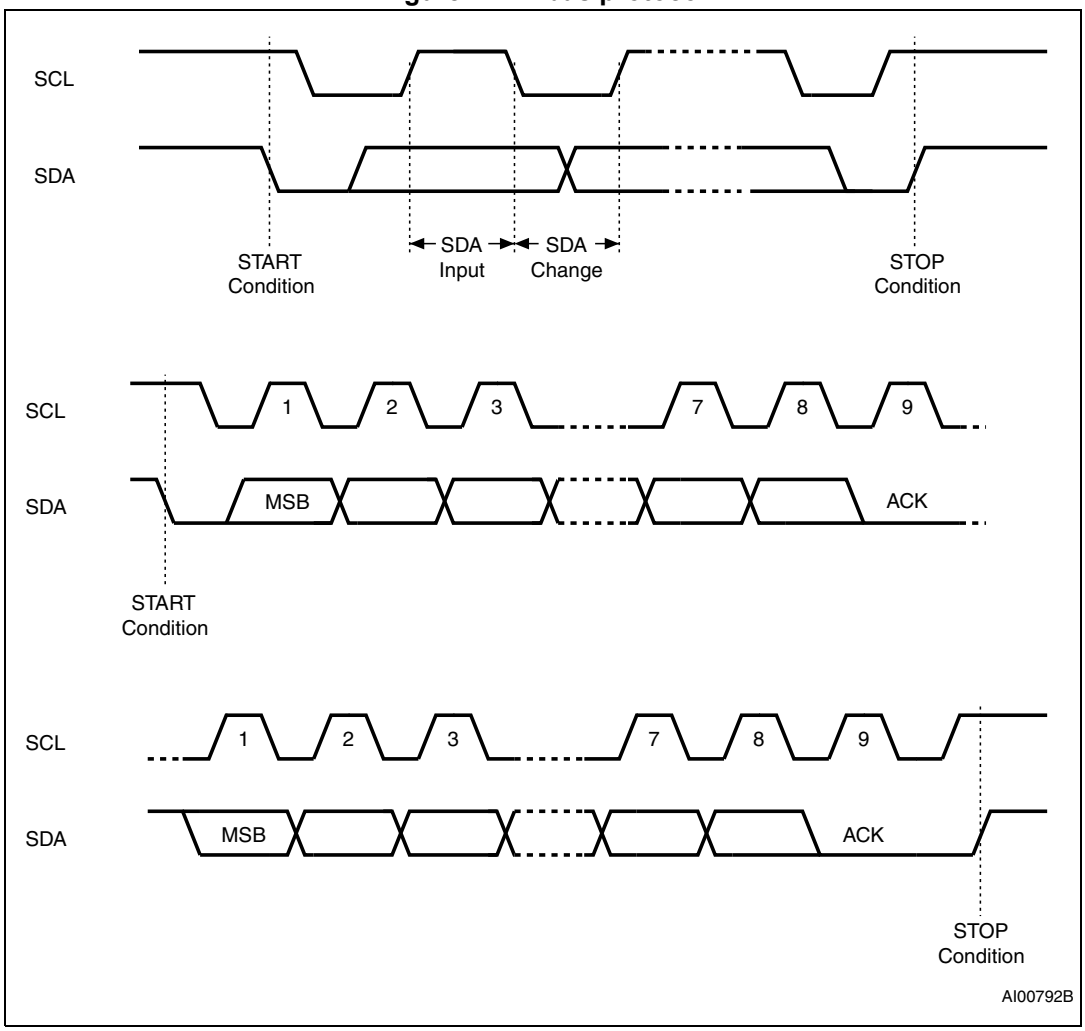
3 Device operation

The device supports the I^2C protocol (see *Figure 4*).

The I^2C bus is controlled by the bus master and the device is always a slave in all communications.

The device (bus master or a slave) that sends data on to the bus is defined as a transmitter; the device (bus master or a slave) is defined as a receiver when reading the data.

Figure 4. I^2C bus protocol



3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

3.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

3.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

3.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, as shown in *Table 2*.

The device select code consists of a 4-bit device type identifier and a 2-bit Chip Enable address (E2, E1). A device select code handling any value other than 1010b (to select the memory) or 1011b (to select the Identification page) is not acknowledged by the memory device.

Up to four memory devices can be connected on a single I^2C bus. Each one is given a unique 2-bit code on the Chip Enable (E2, E1) inputs. When the device select code is received, the memory device only responds if the Chip Enable Address is the same as the value decoded on the E2, E1 inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

Table 2. Device select code

	Device type identifier (1)				Chip Enable address(2)			$\overline{\text{RW}}$
	b7	b6	b5	b4	b3	b2	b1	b0
When accessing the memory	1	0	1	0	E2	E1	A8	$\overline{\text{RW}}$
When accessing the identification page	1	0	1	1	E2	E1	X	$\overline{\text{RW}}$

1. The most significant bit, b7, is sent first.
2. X bit is a Don't Care bit

If the memory device does not match the device select code, it deselects itself from the bus, and enters the Standby mode.

If the memory device matches the device select code, the corresponding memory device gives an acknowledgment on Serial Data (SDA) during the 9th SCL clock period. Once the memory device has acknowledged the device select code, the memory device waits for the master to send the address byte. The memory device responds to the address byte with an acknowledge bit.

Table 3. Significant address bits

		Memory (Device type identifier = 1010b)		Identification page (Device type identifier = 1011b)			
		Random Address Read	Write	Read Identification page	Write Identification page	Lock Identification page	Read lock status
Most significant address bits	b1(1)	A8	A8	X	X	X	see *Section 4.2.5*
Address byte	b7	A7	A7	0	0	1	
	b6	A6	A6	X	X	X	
	b5	A5	A5	X	X	X	
	b4	A4	A4	X	X	X	
	b3	A3	A3	A3	A3	X	
	b2	A2	A2	A2	A2	X	
	b1	A1	A1	A1	A1	X	
	b0	A0	A0	A0	A0	X	

1. Address bits defined inside the DeviceSelect code (see *Table 2*).

Note: A: significant address bit.
X: bit is Don't Care.

3.6 Identification page

The M24C04-DRE offers an Identification Page (16 bytes) in addition to the 4-Kbit memory.

The Identification page contains two fields:

- Device identification code: the first three bytes are programmed by STMicroelectronics with the Device identification code, as shown in *Table 4*.
- Application parameters: the bytes after the Device identification code are available for application specific data.

Note: If the end application does not need to read the Device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the Identification page, the whole Identification page should be permanently locked in Read-only mode.

The instructions Read, Write and Lock Identification Page are detailed in *Section 4: Instructions*.

Table 4. Device identification code

Address in Identification page	Content	Value
00h	ST manufacturer code	20h
01h	I^2C family code	E0h
02h	Memory density code	09h (4-Kbit)

4 Instructions

4.1 Write operations

For a Write operation, the bus master sends a Start condition followed by a device select code with the R/W bit reset to 0. The device acknowledges this, as shown in *Figure 5*, and waits for the master to send the address bytes with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is then triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

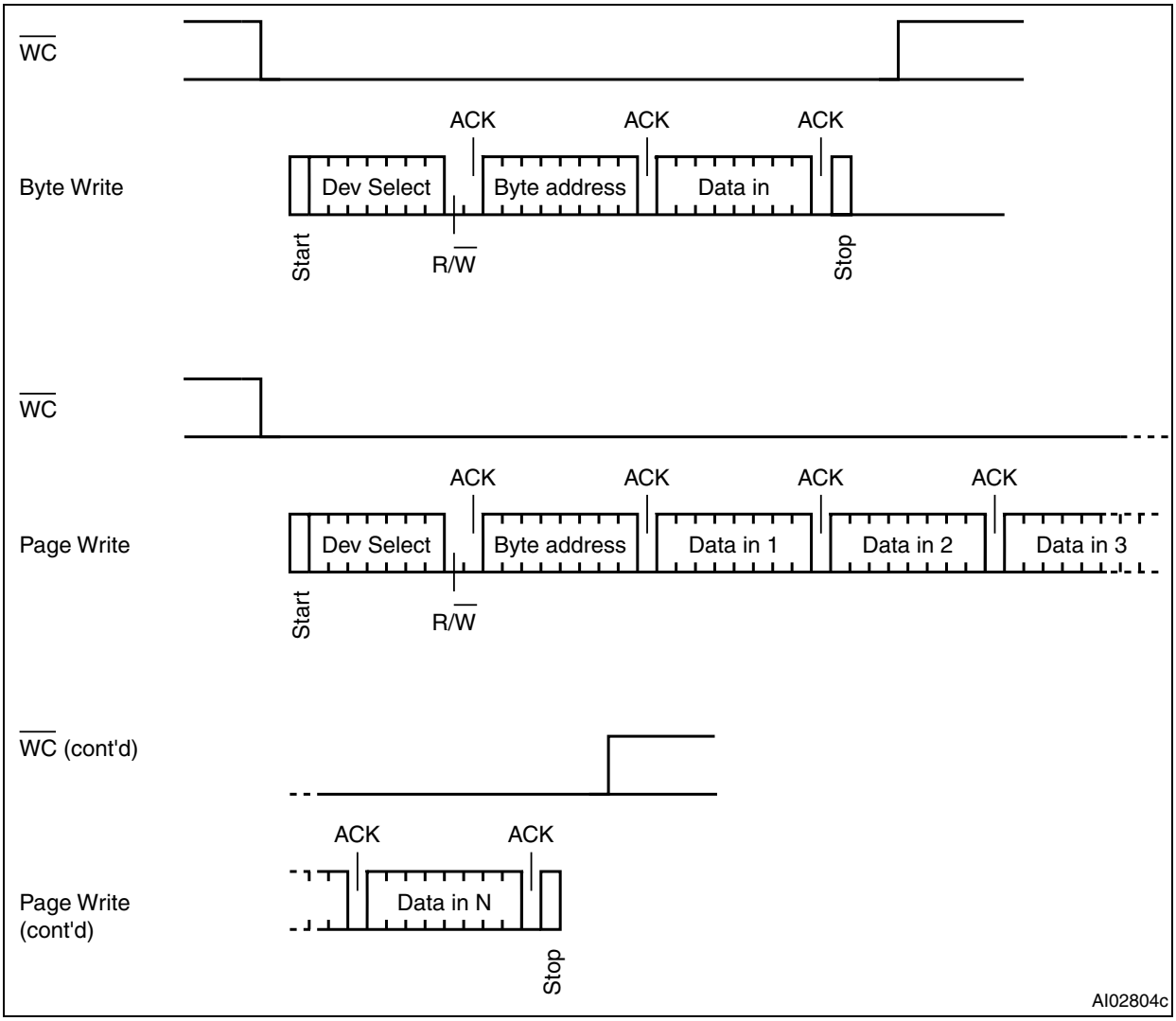
After the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 6*.

4.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck on the received data byte, and the location is not modified (see *Figure 6*). If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 5*.

Figure 5. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)

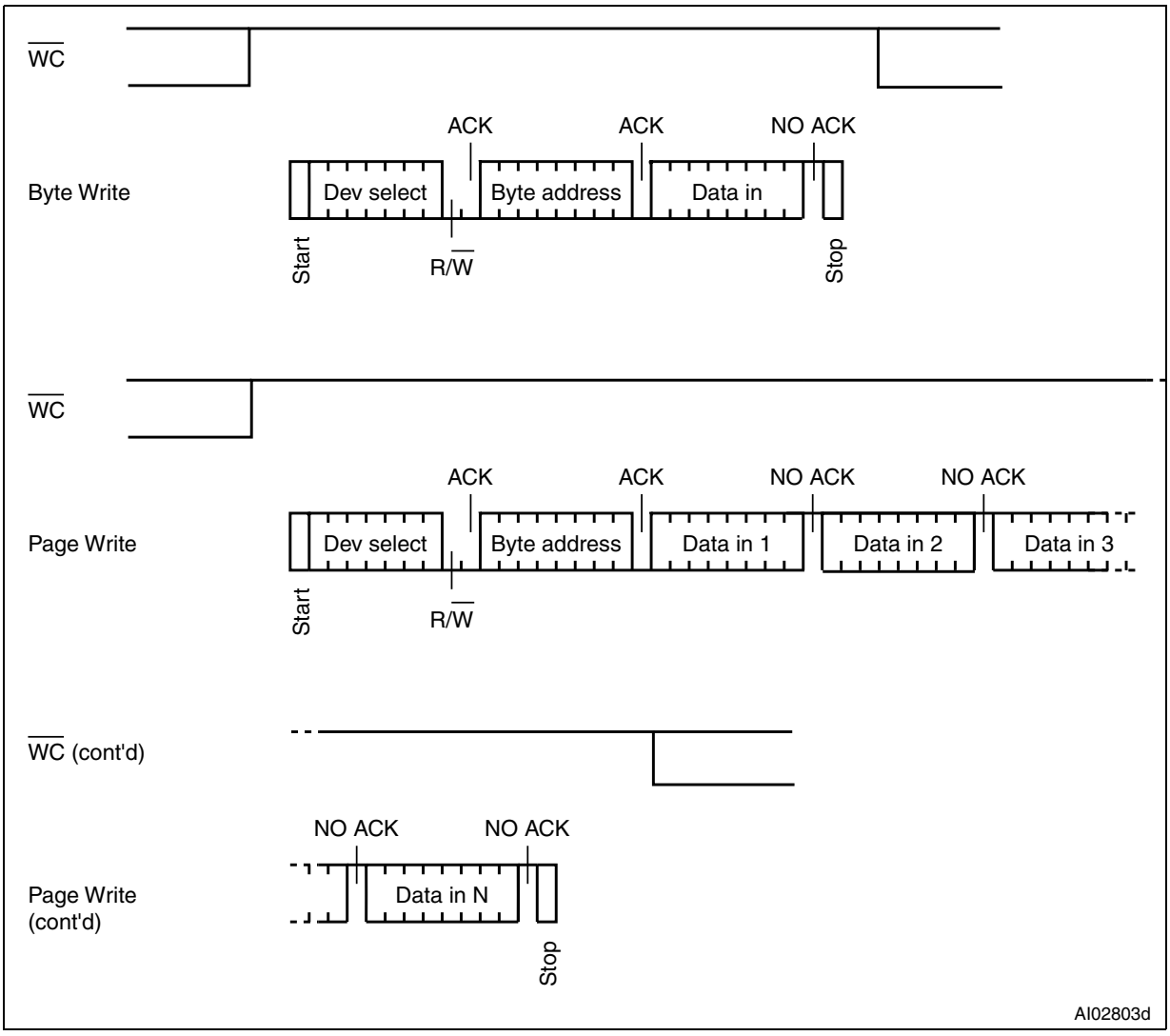


4.1.2 Page Write

The Page Write mode allows up to N(1) bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A8/A4, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the first bytes of the page are overwritten.

Note: The bus master sends from 1 to N(1) bytes of data, each of which is acknowledged by the device if Write Control (WC) is low. If Write Control (WC) is high, the contents of the addressed memory location are not modified, and each data byte received by the device is not acknowledged, as shown in Figure 6. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 6. Write mode sequences with WC = 1 (data write inhibited)



1. N is the number of bytes in a page.

4.1.3 Write Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Most significant address bits A8/A4 are don't care, except for address bit A7 which must be “0”. Least significant address bits A3/A0 define the byte location inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

4.1.4 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A7 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

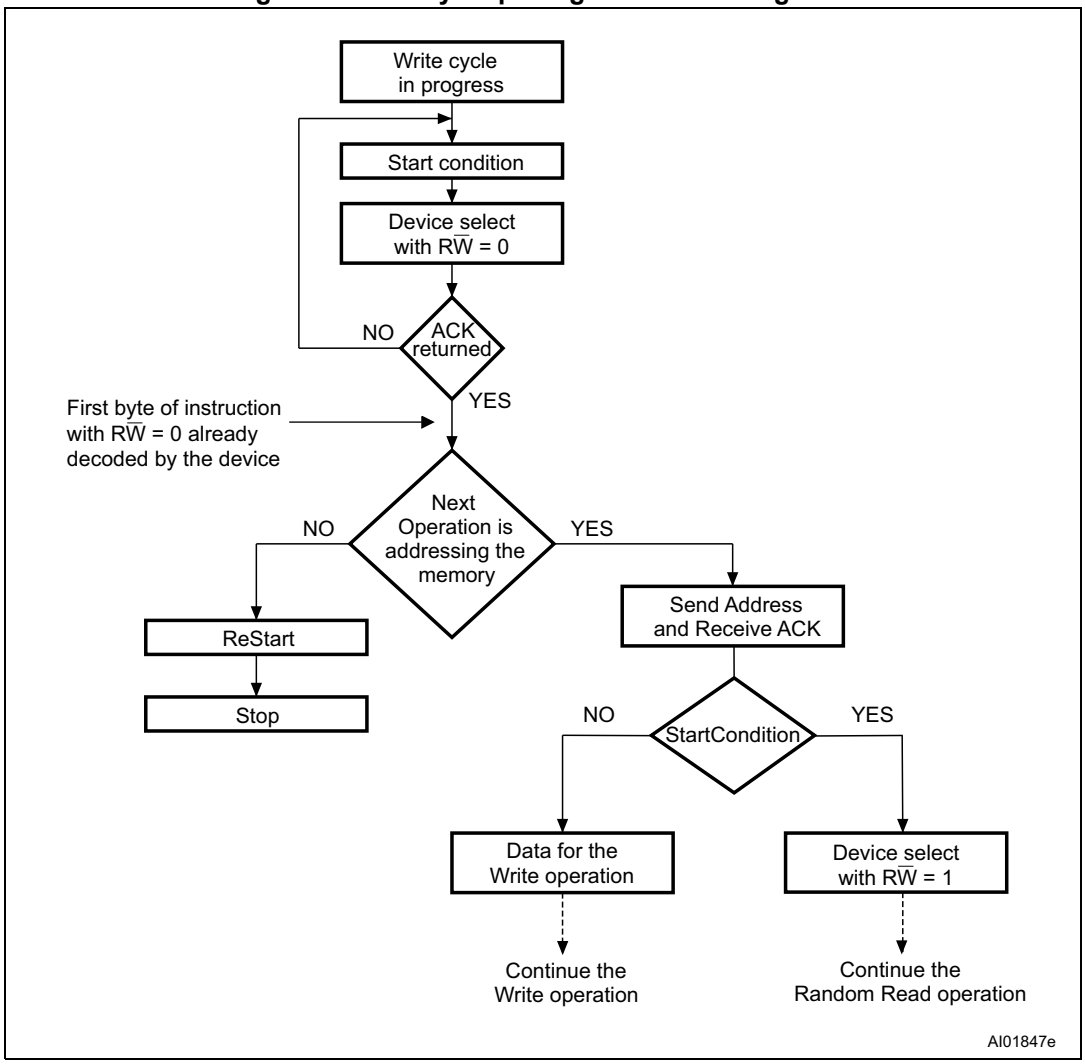
4.1.5 Minimizing Write delays by polling on ACK

The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 7*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 7. Write cycle polling flowchart using ACK

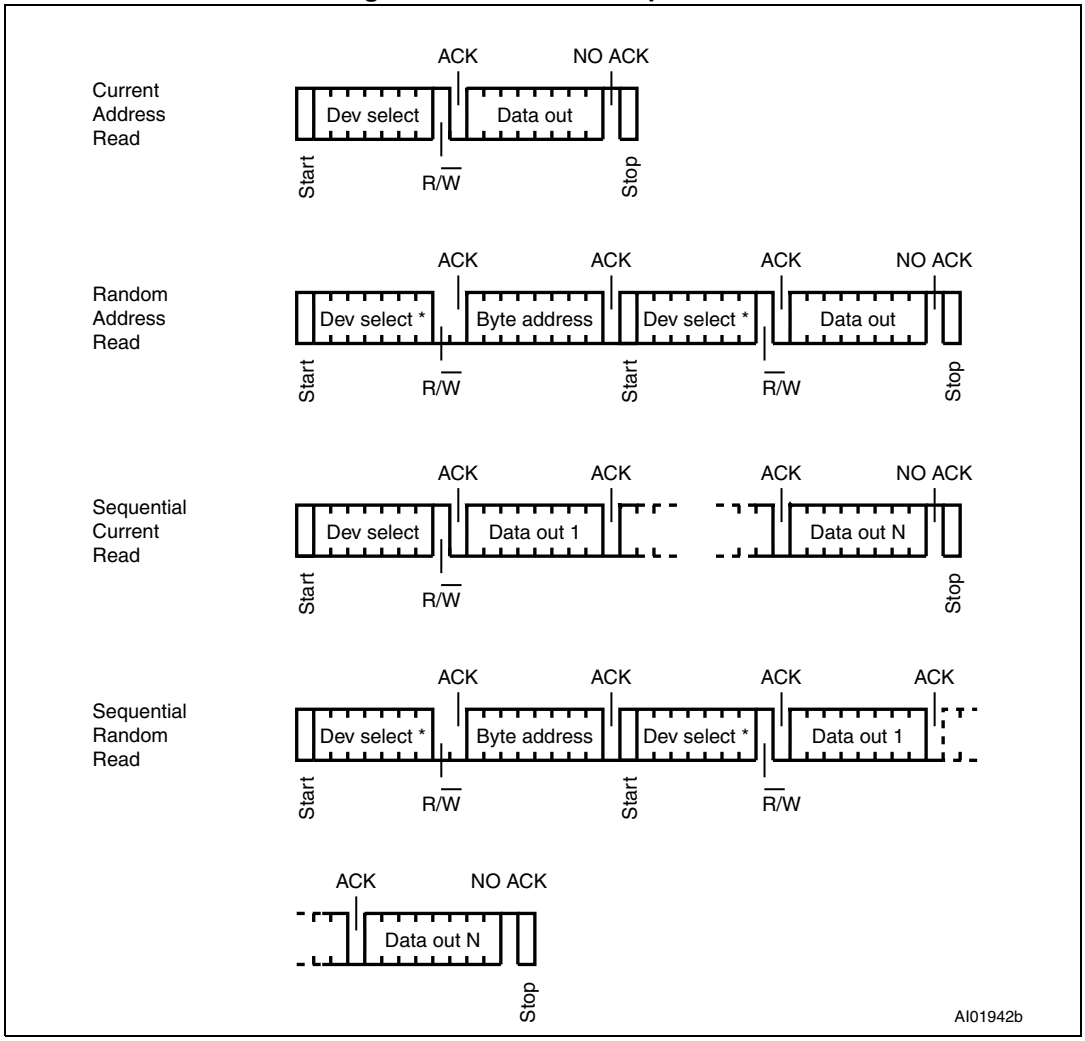


4.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

Figure 8. Read mode sequences



4.2.1 Random Address Read

The Random Address Read is a sequence composed of a truncated Write sequence (to define a new address pointer value, see *Table 1*) followed by a current Read.

The Random Address Read sequence is therefore the sum of [Start + Device Select code with R/W=0 + address bytes] (without Stop condition, as shown in *Figure 8*) and [Start condition + Device Select code with R/W=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data transfer, the bus master does not acknowledge the last data byte and then issues a Stop condition.

4.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte pointed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 8*, *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the Identification page byte location, when accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the Current Address Read instruction.

4.2.3 Sequential Read

A sequential Read can be used after a Current Address Read or a Random Address Read.

After a Read instruction, the device can continue to output the next byte(s) in sequence if the bus master sends additional clock pulses and if the bus master does acknowledge each transmitted data byte. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in *Figure 8*.

The sequential read is controlled with the device internal address counter which is automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

4.2.4 Read Identification Page

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The most significant address bits A8/A4 are don't care except bit A7 which must be 0, the least significant address bits A3/A0 define the byte location inside the Identification page. The number of bytes to read in the ID page must not exceed the page boundary.

4.2.5 Read the lock status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit after the data byte if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

4.2.6 Acknowledge in Read mode

For all Read instructions, the device waits, after each byte sent out, for an acknowledgment from the bus master during the “9th bit” time slot. If the bus master does not send the Acknowledge (the master drives SDA high during the 9th bit time), the device terminates the data transfer and enters its Standby mode.

5 Application design recommendations

5.1 Supply voltage

5.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 6*).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

5.1.2 Power-up conditions

When the power supply is turned on, the V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 6*.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in the DC characteristic *Table 10* as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the Standby power mode
- deselected

As soon as the V_{CC} voltage has reached a stable value within the [V_{CC}(min), V_{CC}(max)] range (defined in *Table 6*), the device is ready for operation.

5.1.3 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 6*), the device must be in Standby power mode (that is after a STOP condition or after the completion of the Write cycle t_W if an internal Write cycle is in progress).

5.2 Error Correction Code (ECC x 1)

The error correction code (ECC x 1) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC x 1 logic is implemented on each byte of the memory array . If a single bit out of the byte happens to be erroneous during a Read operation, the ECC x 1 detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

6 Delivery state

The device is delivered as follows:

- The memory array is set to all 1s (each byte = FFh).
- Identification page: the first three bytes define the Device identification code (value defined in *Table 4*). The content of the following bytes is Don't Care.