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# M24C16-DFCU

## 16-Kbit serial I²C bus EEPROM 4 balls CSP

WLCSP (CU)
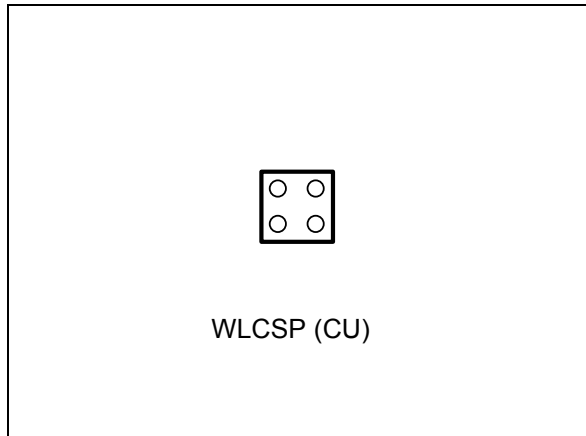
## Features

- Package:
  - RoHS compliant and halogen free WLCSP(ECOPACK2$^®$)
- Compatible with all I2C bus modes
  - 1 MHz
  - 400 kHz
- Memory array:
  - 16 Kbits (2 Kbytes) of EEPROM
  - Page size: 16 bytes
  - Additional Write lockable page(Identification page)
- Supply voltage range:
  - 1.6 V to 5.5 V
- Operating temperature range
  - $V_{CC}$ = 1.7 V : -40°C / +85°C
  - $V_{CC}$ = 1.6 V : -40°C (Read) / 0°C (Write) / +85°C
- Schmitt trigger inputs for noise filtering
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential read modes
- ESD protection
  - Human Body Model: 4 kV
- Write cycle endurance
  - 4 million Write cycles at 25 °C
  - 1.2 million Write cycles at 85 °C
- More than 200-years data retention

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# 1 Description

The M24C16-DFCU is a 16-Kbit I2C-compatible EEPROM assembled in a four balls ultra thin chip scale package (WLCSP).

The device is accessed by a simple serial I2C compatible interface running up to 1 MHz.

The M24C16-DFCU memory array is based on advanced true EEPROM technology (Electrically Erasable Programmable Memory), organized as 128 pages of 16 bytes, with a data integrity improved with an embedded Error Correction Code logic.

The M24C16-DFCU offers an additional Identification Page (16 bytes) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

**Figure 1. Logic diagram**
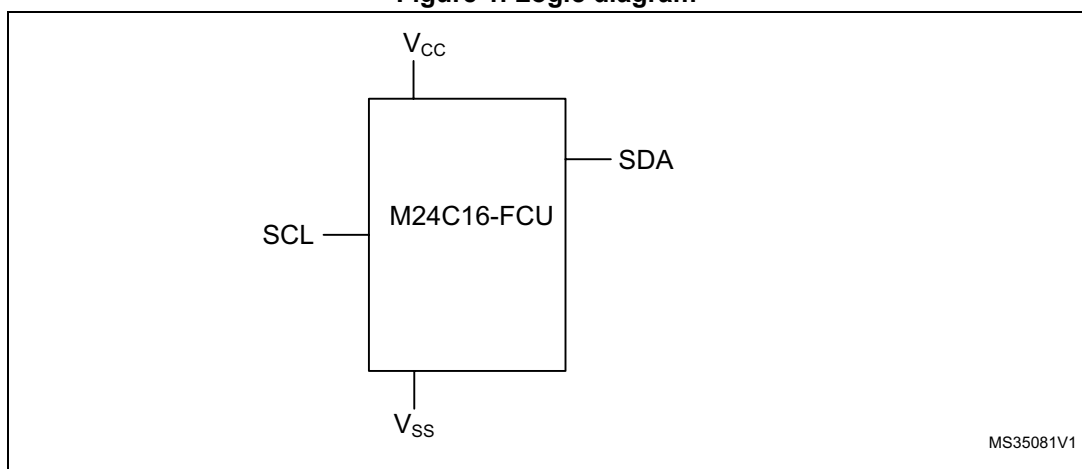


**Table 1. Signal names**

| Signal name | Function | Direction |
|---|---|---|
| SDA | Serial Data | I/O |
| SCL | Serial Clock | Input |
| $V_{CC}$ | Supply voltage | |
| $V_{SS}$ | Ground | |

**Figure 2. WLCSP connections**
**(top view, marking side, with balls on the underside)**
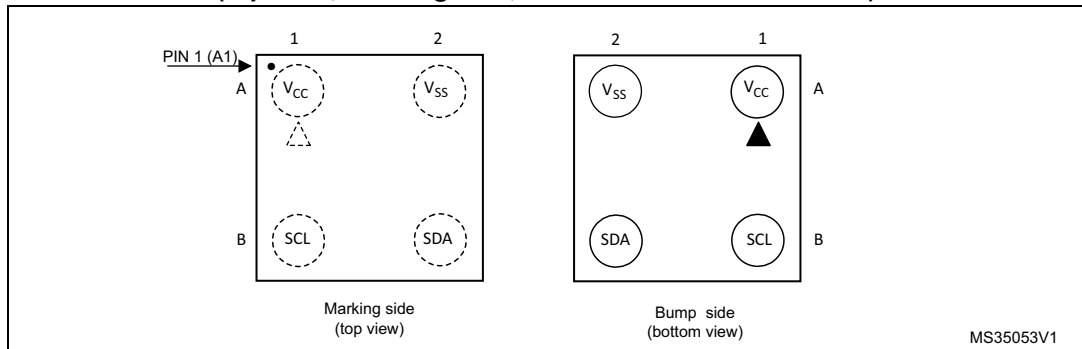
# 2 Signal description

## 2.1 Serial Clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

## 2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to $V_{CC}$ (*Figure 9* indicates how to calculate the value of the pull-up resistor).

## 2.3 $V_{SS}$ (ground)

$V_{SS}$ is the reference for the $V_{CC}$ supply voltage.

## 2.4 Supply voltage ($V_{CC}$)

### 2.4.1 Operating supply voltage ($V_{CC}$)

Prior to selecting the memory and issuing instructions to it, a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied (see Operating conditions in *Section 9: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the $V_{CC}$ line with a suitable capacitor (usually from 10 nF to 100 nF) close to the $V_{CC}$/$V_{SS}$ package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle ($t_W$).

### 2.4.2 Power-up conditions

The $V_{CC}$ voltage has to rise continuously from 0 V up to the minimum $V_{CC}$ operating voltage (see Operating conditions in *Section 9: DC and AC parameters)* and the rise time must not vary faster than 1 V/μs.

### 2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until $V_{CC}$ has reached the internal reset threshold voltage. This threshold is lower than the minimum $V_{CC}$ operating voltage (see Operating conditions in *Section 9: DC and AC parameters*). When $V_{CC}$ passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until $V_{CC}$ reaches a valid and stable DC voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range (see Operating conditions in *Section 9: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in $V_{CC}$), the device must not be accessed when $V_{CC}$ drops below $V_{CC}$(min). When $V_{CC}$ drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

## 2.4.4    Power-down conditions

During power-down (continuous decrease in $V_{CC}$), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

# 3 Memory organization

The memory is organized as shown below.

**Figure 3. Block diagram**
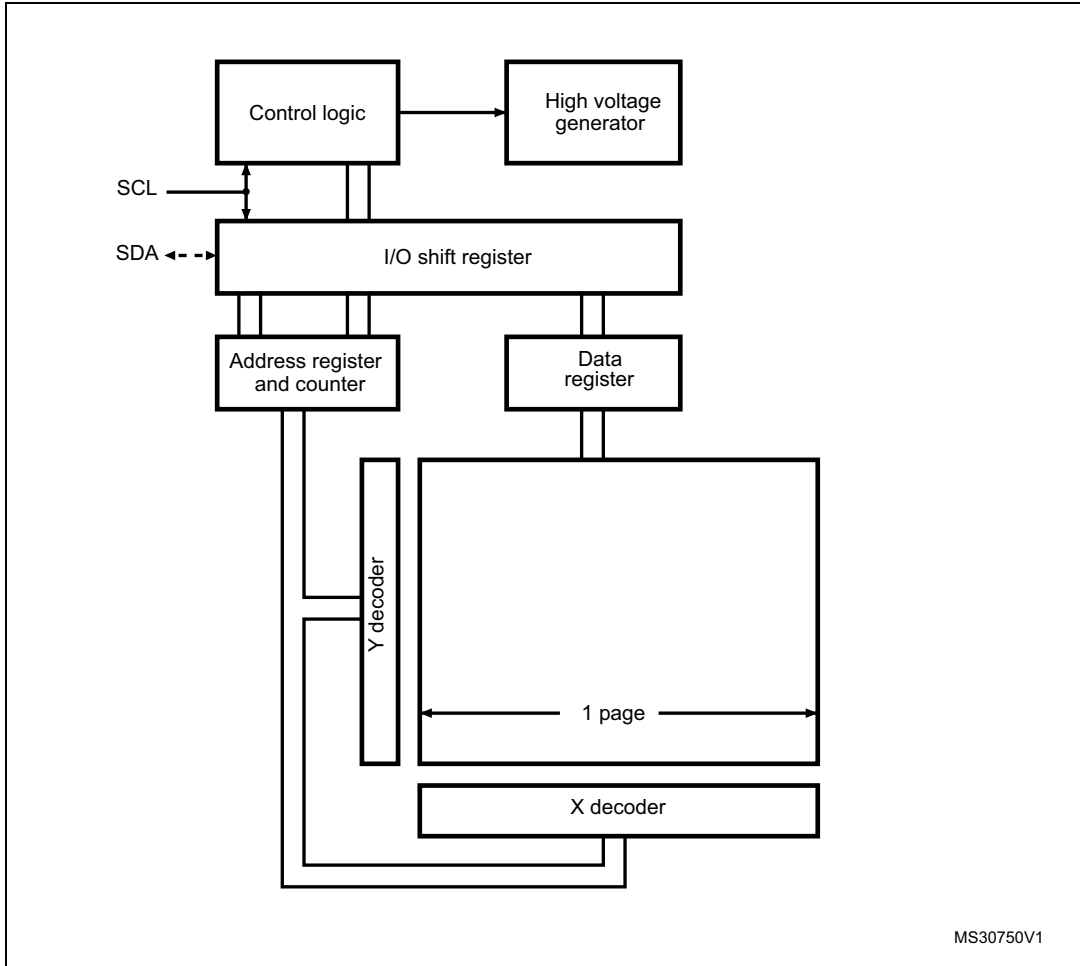
# 4      Device operation

The device supports the I²C protocol. This is summarized in *Figure 4*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

**Figure 4. I²C bus protocol**
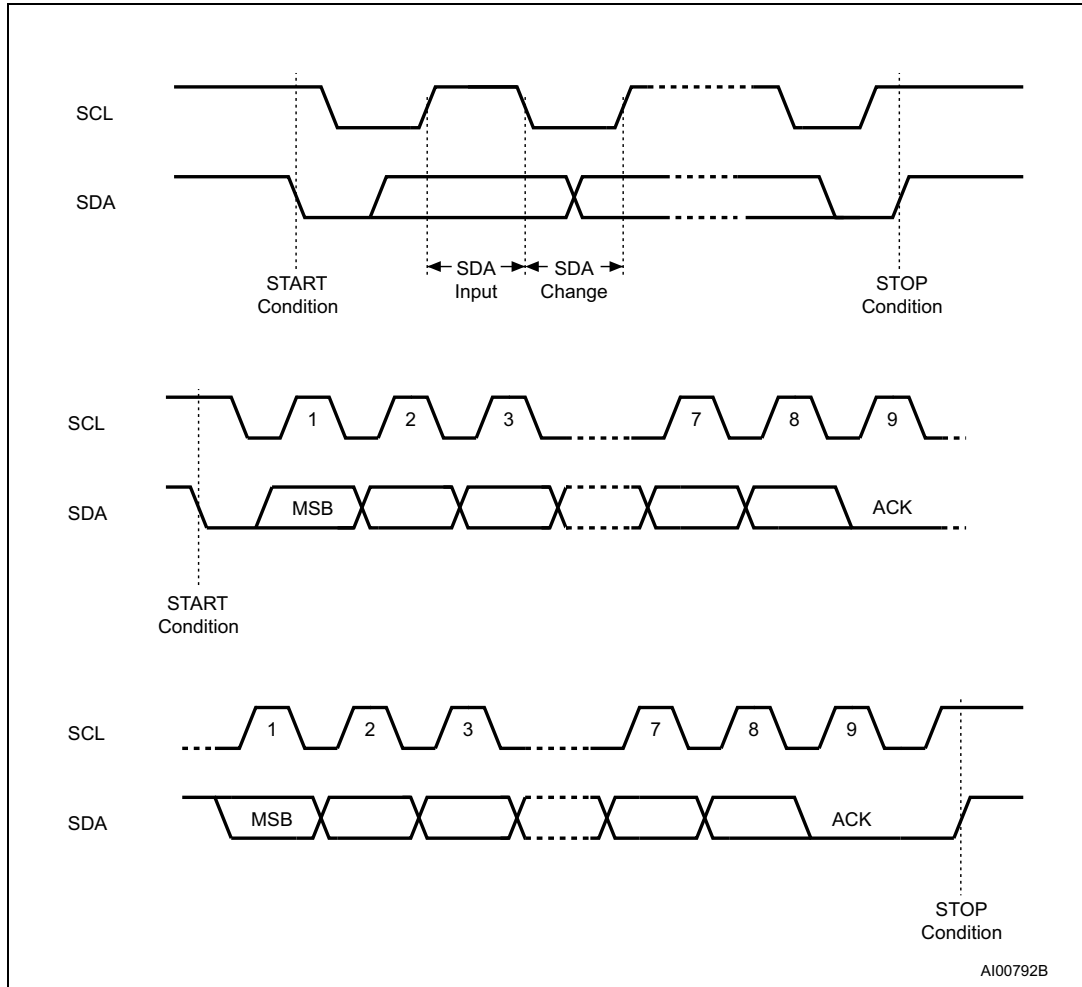
## 4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

## 4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

## 4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

## 4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

**Table 2. Device select code**

| | Device type identifier[1] | | | | Chip Enable address | | | |
|---|---|---|---|---|---|---|---|---|
| | **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| When accessing the memory | 1 | 0 | 1 | 0 | A10 | A9 | A8 | $R\overline{W}$ |
| When accessing the identification page | 1 | 0 | 1 | 1 | X | X | X | $R\overline{W}$ |

1. The most significant bit, b7, is sent first.

The 8$^{th}$ bit is the Read/$\overline{Write}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9$^{th}$ bit time.

If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode (therefore will not acknowledge the device select code).

**Table 3. Significant address bits**

| | | Memory (Device type identifier = 1010b) | | Identification page (Device type identifier = 1011b) | | | |
|---|---|---|---|---|---|---|---|
| | | **Random Address Read** | **Write** | **Read Identification page** | **Write Identification page** | **Lock Identification page** | **Read lock status** |
| Most significant address bits | b3 [1] | A10 | A10 | X | X | X | |
| | b2 [1] | A9 | A9 | X | X | X | |
| | b1 [1] | A8 | A8 | X | X | X | |
| Address byte | b7 | A7 | A7 | 0 | 0 | 1 | |
| | b6 | A6 | A6 | X | X | X | |
| | b5 | A5 | A5 | X | X | X | see *Chapter 5.2.4* |
| | b4 | A4 | A4 | X | X | X | |
| | b3 | A3 | A3 | A3 | A3 | X | |
| | b2 | A2 | A2 | A2 | A2 | X | |
| | b1 | A1 | A1 | A1 | A1 | X | |
| | b0 | A0 | A0 | A0 | A0 | X | |

1. Address bits defined inside the DeviceSelect code (see *Table 2*).

## 4.6 Identification page

The M24C16-DFCU offers an Identification Page (16 bytes) in addition to the 16-Kbit memory. The Identification page contains two fields:

- Device identification code: the first three bytes are programmed by STMicroelectronics with the Device identification code, as shown in *Table 4*.

- Application parameters: the bytes after the Device identification code are available for application specific data.

*Note:* *If the end application does not need to read the Device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the Identification page, the whole Identification page should be permanently locked in Read-only mode.*

The instructions Read, Write and Lock Identification Page are detailed in *Section 5*:

**Table 4. Device identification code**

| Address in Identification page | Content | Value |
|:---:|:---|:---:|
| 00h | ST manufacturer code | 20h |
| 01h | I$^2$C family code | E0h |
| 02h | Memory density code | 0Bh(16-Kbit) |

# 5 Instructions

## 5.1 Write operations

For a Write operation, the bus master sends a Start condition followed by a device select code with the R/W bit reset to 0. The device acknowledges this, as shown in *Figure 5*, and waits for the master to send the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle $t_W$ is then triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

After the successful completion of an internal Write cycle ($t_W$), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

### 5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. The device replies with Ack, as shown in . The bus master shall terminate the transfer by generating a Stop condition.

**Figure 5. Write mode sequence (data write enabled)**
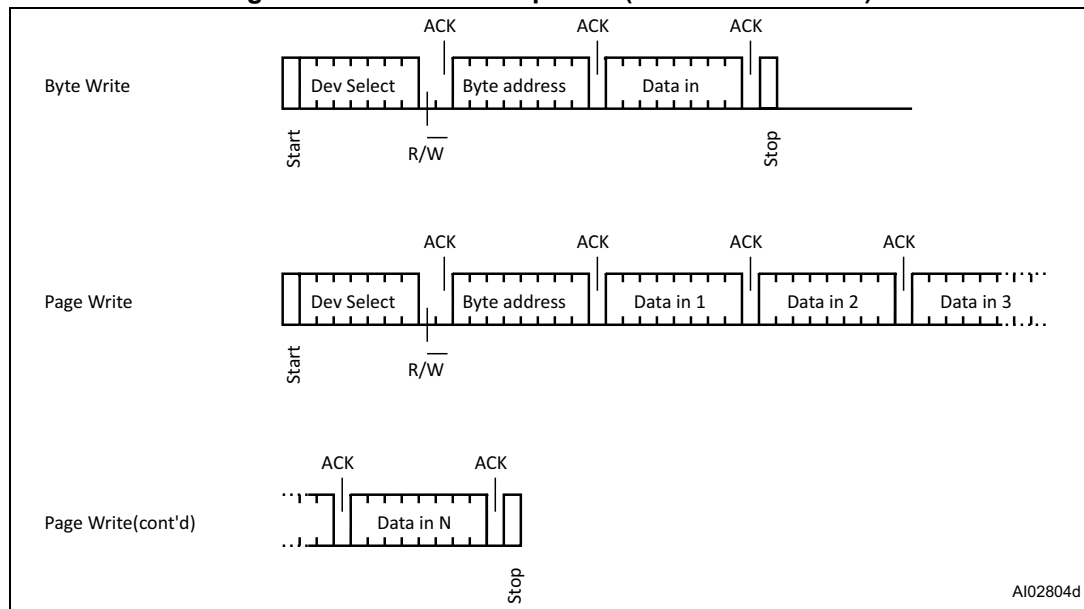
### 5.1.2 Page Write

The Page Write mode allows up to N(a) bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A10/A4, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over" occurs. In case of roll-over, the first bytes of the page are overwritten.

*Note:* *After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.*

### 5.1.3 Write Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Most significant address bits A10/A4 are don't care, except for address bit A7 which must be "0". Least significant address bits A3/A0 define the byte location inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

### 5.1.4 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A7 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

## 5.1.5 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time ($t_w$) is shown in AC characteristics tables in *Section 9: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 6*, is:

*   Initial condition: a Write cycle is in progress.
*   Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
*   Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

**Figure 6. Write cycle polling flowchart using ACK**
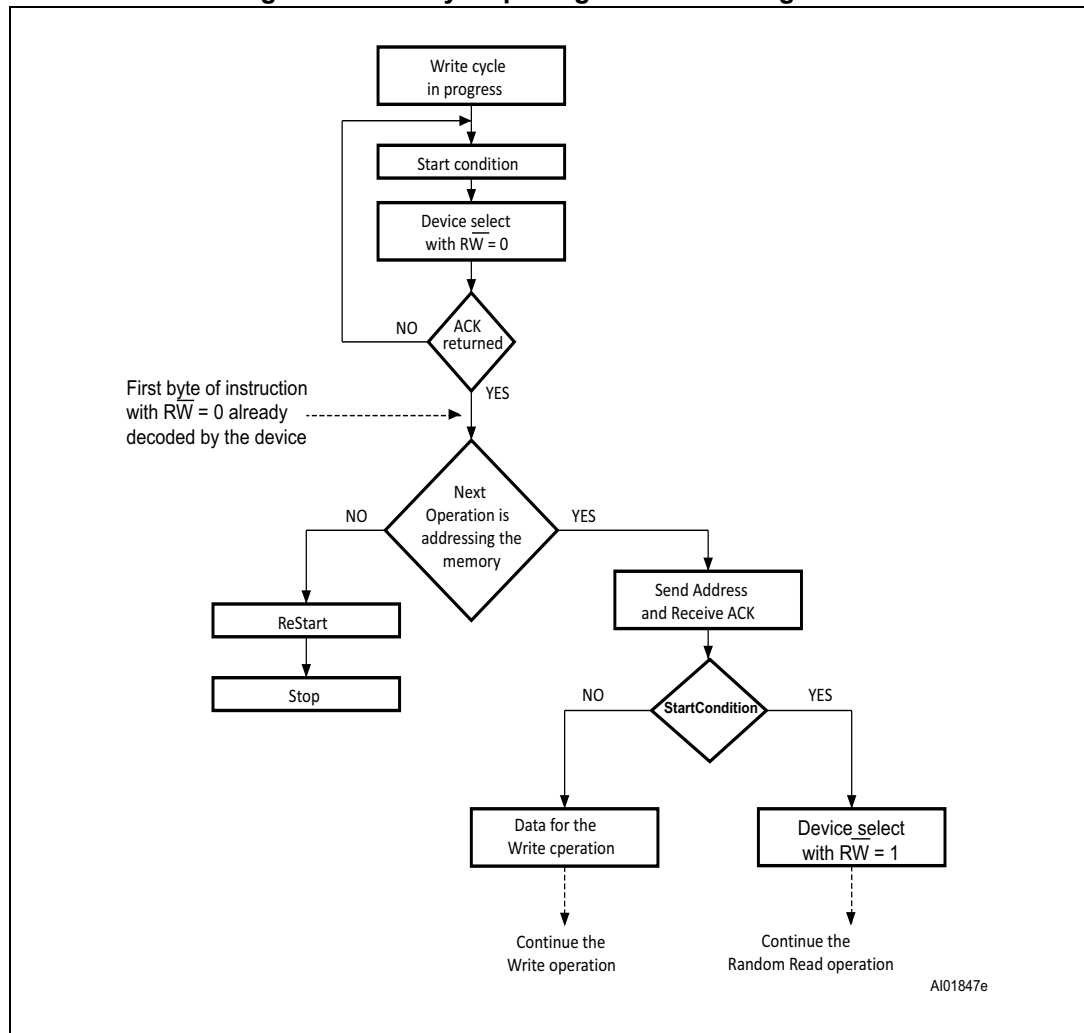


1.  The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

## 5.2 Read operations

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

**Figure 7. Read mode sequences**
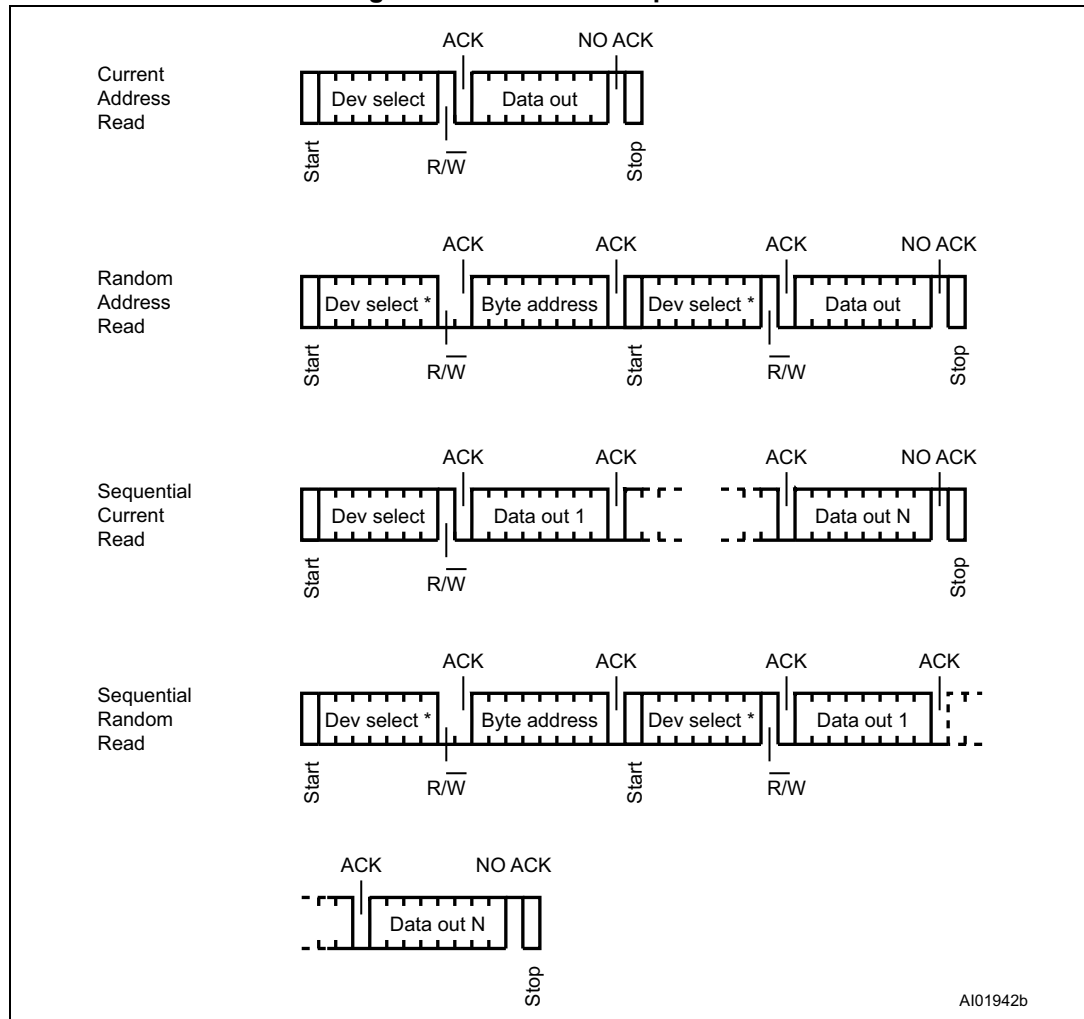


### 5.2.1 Random Address Read

The Random Address Read is a sequence composed of a truncated Write sequence (to define a new address pointer value, see *Table 3*) followed by a current Read.

Therefore the Random Address Read sequence is the sum of [Start + Device Select code with R/W=0 + address byte] (without Stop condition, as shown in *Figure 7*) and [Start condition + Device Select code with R/W=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data

transfer, the bus master does not acknowledge the last data byte and then issues a Stop condition.

### 5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/W̄ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the Identification page byte location, when accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the Current Address Read instruction.

### 5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter "rolls-over", and the device continues to output data from memory address 00h.

### 5.2.4 Read Identification Page

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The most significant address bits A10/A4 are don't care except bit A7 which must be 0, the least significant address bits A3/A0 define the byte location inside the Identification page. The number of bytes to read in the ID page must not exceed the page boundary.

### 5.2.5 Read the lock status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction plus one data byte] to the device. The device returns an acknowledge bit after the data byte if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked. After this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

* Start: the truncated command is not executed because the Start condition resets the device internal logic,
* Stop: the device is then set back into Standby mode by the Stop condition.

### 5.2.6 Acknowledge in Read mode

For all Read instructions, after each byte sent out, the device waits for an acknowledgment from the bus master during the "9th bit" time slot. If the bus master does not send the Acknowledge (the master drives SDA high during the 9th bit time), the device terminates the data transfer and enters its Standby mode.

# 6 Application design recommendations

## 6.1 Supply voltage

### 6.1.1 Operating supply voltage (VCC)

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see *Table 6*).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write cycle (tW). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the VCC/VSS package pins.

### 6.1.2 Power-up conditions

When the power supply is turned on, the VCC voltage has to rise continuously from 0 V up to the minimum VCC operating voltage defined in see *Table 6*.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until VCC reaches the internal threshold voltage (this threshold is defined in the DC characteristic *Table 11* as VRES).

When VCC passes over the POR threshold, the device is reset and in the following state:
- in the Standby power mode
- deselected

As soon as the VCC voltage has reached a stable value within the [VCC(min), VCC(max)] range (defined in *Table 6*), the device is ready for operation.

### 6.1.3 Power-down

During power-down (continuous decrease in the VCC supply voltage below the minimum VCC operating voltage defined in *Table 6*), the device must be in Standby power mode (that is after a STOP condition or after the completion of the Write cycle $t_W$ if an internal Write cycle is in progress).

## 6.2 Error correction code (ECC x 1)

The error correction code (ECC x 1) is an internal logic function which is transparent for the I2C communication protocol.

The ECC x 1 logic is implemented on each byte of the memory array. If a single bit out of the byte happens to be erroneous during a Read operation, the ECC x 1 detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

# 7 Initial delivery state

The device is delivered as follows:

• The memory array is set to all 1s (each byte = FFh).

• Identification page: the first three bytes define the Device identification code (value defined in *Table 4*). The content of the following bytes is Don't Care.

# 8 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute maximum ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| | Ambient operating temperature | –40 | 130 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_{LEAD}$ | Lead temperature during soldering | see note[1] | | °C |
| $V_{IO}$ | Input or output range | –0.50 | 6 | V |
| $I_{OL}$ | DC output current (SDA = 0) | - | 5 | mA |
| $V_{CC}$ | Supply voltage | –0.50 | 6 | V |
| $V_{ESD}$ | Electrostatic pulse (Human Body model)[2] | - | 4000 | V |

1. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).

2. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).

# 9      DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

**Table 6. Operating conditions**

| Symbol | Parameter | Min. | | Max. | Unit |
|--------|-----------|------|------|------|------|
| $V_{CC}$ | Supply voltage | 1.6 | 1.7 | 5.5 | V |
| $T_A$ | Ambient operating temperature: Read | –40 | -40 | 85 | °C |
|  | Ambient operating temperature: Write | 0 | -40 | | |
| $f_C$ | Operating clock frequency @1.6 V | | - | 400 | kHz |
|  | Operating clock frequency @1.7 V | | - | 1000 | |

**Table 7. AC measurement conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| $C_{bus}$ | Load capacitance | 100 | | pF |
| - | SCL input rise/fall time, SDA input fall time | - | 50 | ns |
| - | Input levels | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| - | Input and output timing reference levels | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |

**Figure 8. AC measurement I/O waveform**
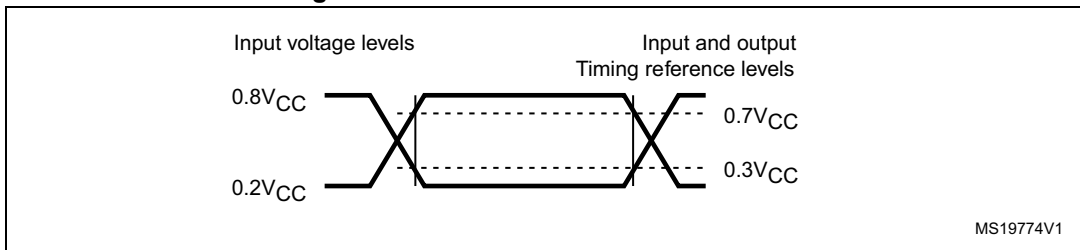


**Table 8. Input parameters**

| Symbol | Parameter [1] | Test condition | Min. | Max. | Unit |
|--------|---------------|----------------|------|------|------|
| $C_{IN}$ | Input capacitance (SDA) | - | - | 8 | pF |
| $C_{IN}$ | Input capacitance (other pins) | - | - | 6 | pF |
| $Z_L$ | Input impedance ($\overline{WC}$) | $V_{IN} < 0.3\ V_{CC}$ | 30 | - | kΩ |
| $Z_H$ | | $V_{IN} > 0.7\ V_{CC}$ | 500 | - | kΩ |

1. Characterized only, not tested in production.

**Table 9. Cycling performance**

| Symbol | Parameter | Test condition | Max. | Unit |
|--------|-----------|----------------|------|------|
| Ncycle | Write cycle endurance | $T_A \leq$ 25 °C, $V_{CC}$(min) < $V_{CC}$ < $V_{CC}$(max) | 4,000,000 | Write cycles |
| | | $T_A$ = 85°C, $V_{CC}$(min) < $V_{CC}$ < $V_{CC}$(max) | 1,000,000 | |

**Table 10. Memory cell data retention**

| Parameter | Test condition | Min. | Unit |
|-----------|----------------|------|------|
| Data retention | $T_A$ = 55 °C | 200 | Years |