Chipsmall
深圳市津利帝科技有限公司
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采购部

IS25LQ080

8M-BIT
3V- QUAD SERIAL FLASH MEMORY WITH
MULTI-I/O SPI

DATA SHEET

8M-BIT
3V- QUAD SERIAL FLASH MEMORY MULTI- I/O SPI

FEATURES

- **Industry Standard Serial Interface**
  - IS25LQ080: 8M-bit/ 1M-byte
  - 256-bytes per Programmable Page Standard
  - Standard SPI/ Dual SPI/ Quad SPI
- **High Performance Serial Flash (SPI)**
  - 104 MHz SPI/ Dual SPI/ or Quad SPI
  - 416 MHz equivalent Quad SPI
  - 52MB/S Continuous Data Throughput
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles[1]
  - More than 20-year data retention
- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous data read with Byte Wrap around
  - Allows XIP operations (execute in place)
  - Outperforms X16 Parallel Flash
- **Flexible & Cost Efficient Memory Architecture**
  - Uniform 4K-byte Sector Erase
  - Uniform 64K-byte Block Erase
  - Program from 1 to 256 bytes
  - Program/Erase Suspend and Resume
- **Low Power with Wide Temp. Ranges**
  - Single 2.3V to 3.6V Voltage Supply
  - 10 mA Active Read Current
  - 5 µA Standby Current
  - Temp Grades: -40°C to +105°C
- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - 256-Byte dedicated area, user-lockable, One Time Programmable Memory (OTP)
- **Industry Standard Pin-out & Pb-Free Packages**
  - JB = 8-pin SOIC 208mil
  - JN = 8-pin SOIC 150mil
  - JK= 8-pin WSON 6x5 mm
  - JV = 8-pin VVSOP 150mil
  - KGD (call factory)

GENERAL DESCRIPTION

The IS25LQ080 (8M-bit) Serial Flash memory offers a storage solution with flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" is for systems that have limited space, pins, and power. The IS25LQ080 are accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which also serve as multi-function I/O pins in Dual and Quad modes (see pin descriptions). The IS25xQ series of flash is ideal for code shadowing to RAM, execute in place (XIP) operations, and storing non-volatile data.

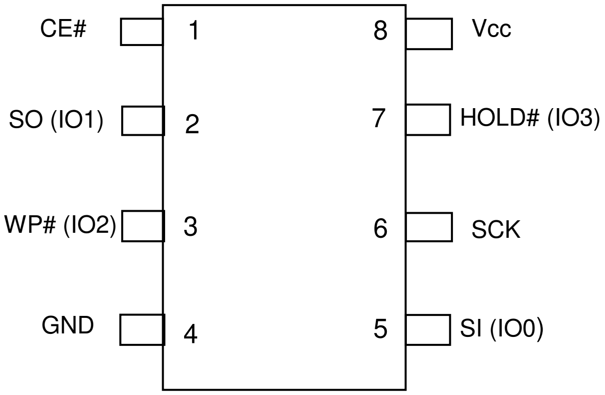
The memory array is organized into programmable pages of 256-bytes each. The IS25LQ080 supports page program mode where 1 to 256 bytes of data can be programmed into the memory with one command. Pages can be erased in groups of 4K-byte sectors, 64K-byte blocks, and/or the entire chip. The uniform 4K-byte sectors and 64K-byte blocks allow greater flexibility for a variety of applications requiring solid data retention.

The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad output (SPI), and Dual/Quad I/O (SPI). Clock frequencies of up to 104MHz in SPI/Dual/Quad I/O modes allow for equivalent clock rates of up to 416MHz (104MHz x 4) allowing up to 52MB/S of throughput. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access for a XIP (execute in place) operation.

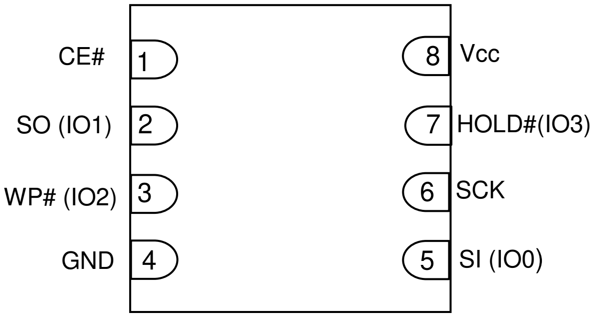
The IS25LQ080 is manufactured using industry leading non-volatile memory technology. The devices are offered in industry standard lead-free packages. See Ordering Information for the density and package combinations available.

[1] 100,000 Continuous Chip and Block cycling, 100,000 Continuous Sector cycling

Connection Diagrams



8-pin SOIC 208mil (Package: JB)
8-pin SOIC 150mil (Package: JN)
8-pin VVSOP 150mil (Package: JV)



8-pin WSON 6x5mm (Package: JK)

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitries power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect**: The WP# pin protects the Status Register from being written. When the WP# is low the status registers are write-protected and vice-versa for high. When the QE bit is set to “1”, the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3)	INPUT/OUTPUT	**Hold:** Pauses serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set to “1”, HOLD# pin is not available since it becomes IO3. The HOLD# pin allows the device to be paused while it is selected. The HOLD# pin is active low. When HOLD# is in a low state, and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. When the QE bit of Status Register is set for Quad I/O, the HOLD# pin function is not available and becomes IO3 for Multi-I/O SPI mode.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left uncommitted.

Table 1. Pin Descriptions

BLOCK DIAGRAM

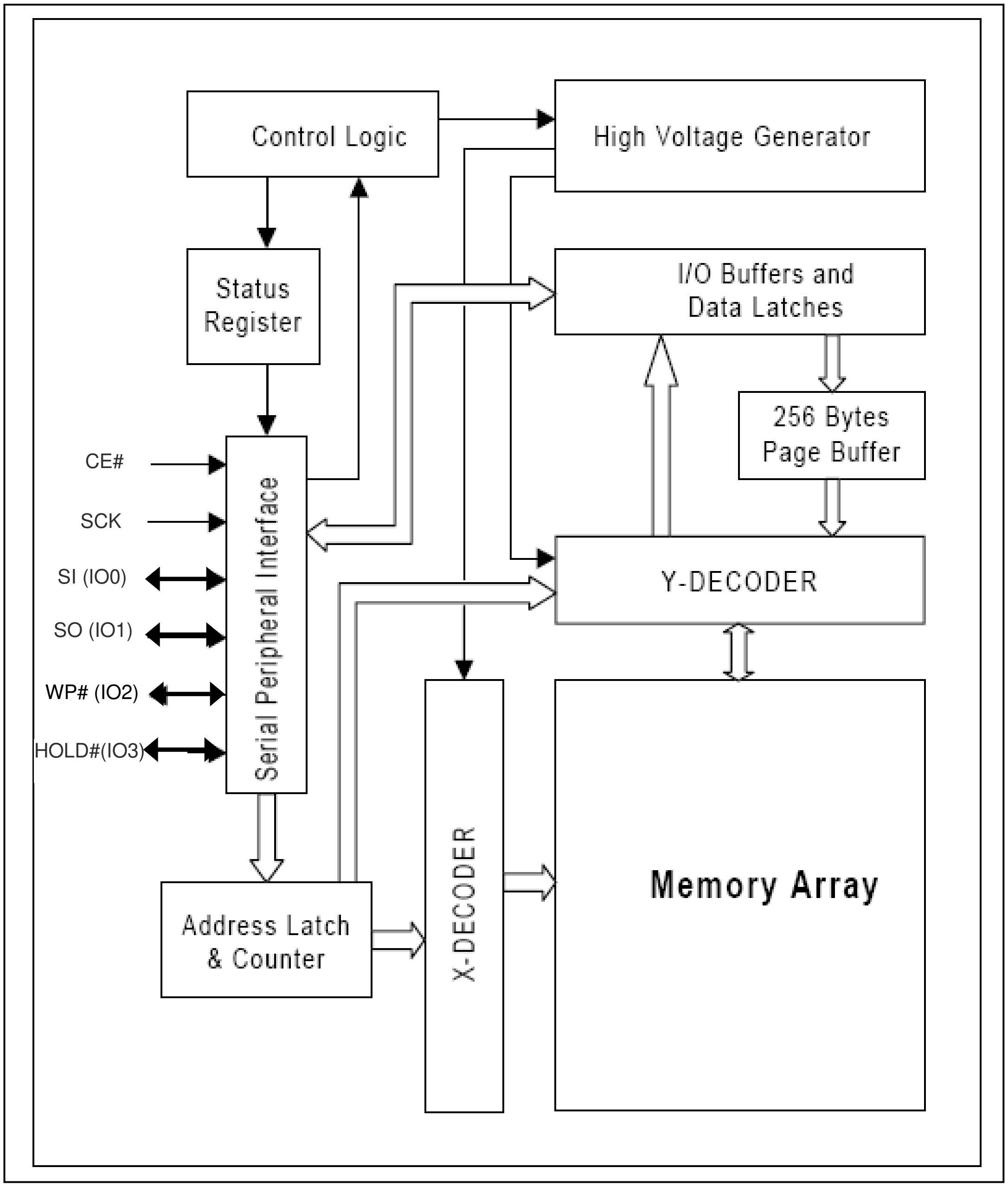


Figure 1. Flash Block Diagram

MEMORY CONFIGURATION

Table 2 below illustrates the memory architecture of the device and its block and sector addresses.

Memory Density	Block No.	Block Size (Kbytes)	Sector No.	Sector Size (Kbytes)	Address Range
8Mbit	Block 0	64	Sector 0	4	000000h - 000FFFh
			Sector 1	4	001000h - 001FFFh
			:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	64	Sector 16	4	010000h - 010FFFh
			Sector 17	4	011000h - 011FFFh
			:	:	:
			Sector 31	4	01F000h - 01FFFFh
	:	:	:	:	:
	Block 7	64	Sector 127	4	070000h – 07FFFFh
	Block 8	64	Sector 128	4	080000h – 08FFFFh
	:	:	:	:	:
	:	:	:	:	:
	Block 15	64	Sector 255	4	0F0000h – 0FFFFFh

Table 2. Block/Sector Addresses of IS25LQ080

REGISTERS

STATUS REGISTER

Refer to Tables 3 and 4 for Status Register Format and Status Register Bit Definitions.

The BP3, BP2, BP1, BP0, QE, and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP3, BP2, BP1, BP0, QE and SRWD bits are set to “0” from the factory. The Status Register can be read by the Read Status Register (RDSR). Refer to Table 8 for the Instruction Set.

The function of Status Register bits are described as follows:

WIP bit: The Write in Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for a write status register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled, and all write operations, including write status register, page program, sector erase, block and chip erase operations are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of a write instruction.

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define which memory portion of the entire memory area should be protected. Refer to Table 5 for the Block Write Protection bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operations to that area will be inhibited.

Note: Chip Erase (CHIP_ER) instruction can be executed only if the Block Protection Bits are not set and locked

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SRWD bit: The Status Register Write Disable (SRWD) bits operate in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to “0”, the Status Register is not write-protected. When the SRWD is set to “1” and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to “1” and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the status register that allows Quad operation. When the QE bit is set to “0”, the pin WP# and HOLD# are enable. When the QE bit is set to “1”, the pin IO2 and IO3 are enable.

WARNING: The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground.

Status Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default values	0	0	0	0	0	0	0	0

* The default value of the SRWD, QE, BP3, BP2, BP1, and BP0 are set to “0” from the factory.

Table 3. Status Register Format

Bit	Name	Definition	Read/Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates a write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No
Bit 2	BP0	Block Protection Bit: (Table 5) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function is disabled (default) “1” indicates the Quad output function is enabled	R/W	Yes
Bit 7	SRWD	Status Register Write Disable: (See Table 3) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Yes

Table 4. Status Register Bit Definition

Status Register Bits				8 Mbit- Protected Memory Area	
BP3	**BP2**	**BP1**	**BP0**	**Protected Blocks**	**Protected Portion**
0	0	0	0	None	None
0	0	0	1	15	Upper 1/16
0	0	1	0	14 to 15	Upper 2/16
0	0	1	1	12 to 15	Upper 1/4
0	1	0	0	8 to 15	Upper 1/2
0	1	0	1	All blocks	All
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1	0 to 7	Lower 1/2
1	1	0	0	0 to 11	Lower 3/4
1	1	0	1	0 to 13	Lower 7/8
1	1	1	0	0 to 14	Lower 15/16
1	1	1	1	All blocks	All

Table 5. Block Write Protect Bits for IS25LQ080

PROTECTION MODE

There are two types of write-protection mechanisms: hardware and software. Both are used to prevent incorrect operation in a possibly noisy environment where data integrity cannot be guaranteed.

HARDWARE WRITE-PROTECTION

The devices provide two hardware write-protection features:

a. When inputting a program, erase or write status register instruction, the number of clock pulses is checked to determine whether it is a multiple of eight before executing. Any incomplete instruction command sequence will be ignored.

b. Write inhibit is 2.1V, all write sequence will be ignored when Vcc drops below 2.1V.

c. The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0 and SRWD in the Status Register. Refer to the STATUS REGISTER description.

SOFTWARE WRITE PROTECTION

There are two types of software write protection features:

a. Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.

b. The Block Protection (BP3, BP2, BP1, BP0) bits can control whether the entire memory area or just a partial portion is write-protected.

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Table 6. Hardware Write Protection on Status Register

SPI INSTRUCTIONS AND DEVICE OPERATION

The instruction set for controlling the device is located in table 8 and can be fully controlled through the SPI bus. Instructions can be initiated with the falling edge of Chip Enable (CE#). The first byte of data clocked into the SI pin provides the instruction code. Data on the SI pin is sampled by SCKs (serial clock) rising edge with the most significant bit (MSB) read first.

Instructions vary in length (bytes) and may be followed by address bytes, data bytes, and or dummy bytes (don’t care). Sometimes the instruction will require a combination of commands to perform the function.

Instructions are read on the rising edge of SCK. A full 8-bits must be clocked with CE# pulled high at the byte boundary before any command is accepted (expect for read).

Read instructions can be completed after any clocked bit. This design feature protects the device from unwanted writes. The timing for each instruction is illustrated in the following figures.

Table 7 contains the Manufacturing and Device IDs.

Product Identification		Hex Code
Manufacturer ID	Manufacture ID1	9Dh
	Manufacture ID2	7Fh
Device ID: IS25LQ080	Device ID1	13h
	Device ID2	44h

Table 7. Manufacture and Device Identification

Instruction Name	Hex Code	Operation	Command Cycle*	Maximum Frequency
RDID	ABh	Read Device ID and Release from power down	4 Bytes	104 MHz
JEDEC ID READ	9Fh	JEDEC ID Read- Manufacturer and Device ID	1 Byte	104 MHz
RDMDID	90h	Read Manufacturer and Device ID	4 Bytes	104 MHz
WREN	06h	Write Enable	1 Byte	104 MHz
WRDI	04h	Write Disable	1 Byte	104 MHz
RDSR	05h	Read Status Register	1 Byte	104 MHz
WRSR	01h	Write Status Register	2 Bytes	104 MHz
READ	03h	Read Data Bytes from Memory at Normal Read Mode	4 Bytes	33 MHz
FAST_READ	0Bh	Read Data Bytes from Memory at Fast Read Mode	5 Bytes	104 MHz
FRDO	3Bh	Fast Read Dual Output	5 Bytes	104 MHz
FRDIO	BBh	Fast Read Dual I/O	3 Bytes	104MHz
FRQO	6Bh	Fast Read Quad Output	5 Bytes	104 MHz
FRQIO	EBh	Fast Read Quad I/O	2 Bytes	104MHz
MR	FFh	Mode Reset	2 Byte	104MHz
PAGE_ PROG	02h	Page Program Data Bytes Into Memory	4 Bytes + 256B	104 MHz
SECTOR_ER	D7h/20h	Sector Erase	4 Bytes	104 MHz
BLOCK_ER	D8h	Block Erase	4 Bytes	104 MHz
CHIP_ER	C7h/60h	Chip Erase	1 Byte	104 MHz
Quad page program	32h	Page Program Data Bytes Into Memory with Quad interface	4 Bytes + 256B	104 MHz
Program/Erase suspend	75h/B0h	Interrupts the system to pause an program/erase CMD	1 Byte	104 MHz
Program/Erase resume	7Ah/30h	Resumes the program/erase CMD	1 Byte	104 MHz
PSIR	B1h	Program One Time Programmable Area (OTP)	4 Bytes + 265B	104 MHz
RSIR	4Bh	Read One Time Programmable Area (OTP)	4 Bytes	33 MHz

Table 8. Instruction Set

*Note 1. Command Cycle includes Instruction Byte

HOLD OPERATION

The HOLD# pin In SPI and Dual SPI mode allow an operation to be paused while it is actively selected (CE# is low).

The HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. See example below, Configuring Multiple SPI Devices and Modes (0 or 3).

The HOLD function is only available for SPI and Dual SPI operations. To initiate a HOLD operation, the device must be selected (CE# set low) and HOLD# pin pulled low. The HOLD operation will activate on the falling edge of the HOLD# signal if SCK is already low. If the SCK is not already low the HOLD condition will begin at the next falling edge of SCK. Inputs to SI will be ignored and SO will be in a high impedance state. The HOLD condition will terminate on the rising edge of the HOLD# signal if SCK signal is already low, if not, HOLD condition will terminate at the next SCK falling edge. The paused operation can now continue.

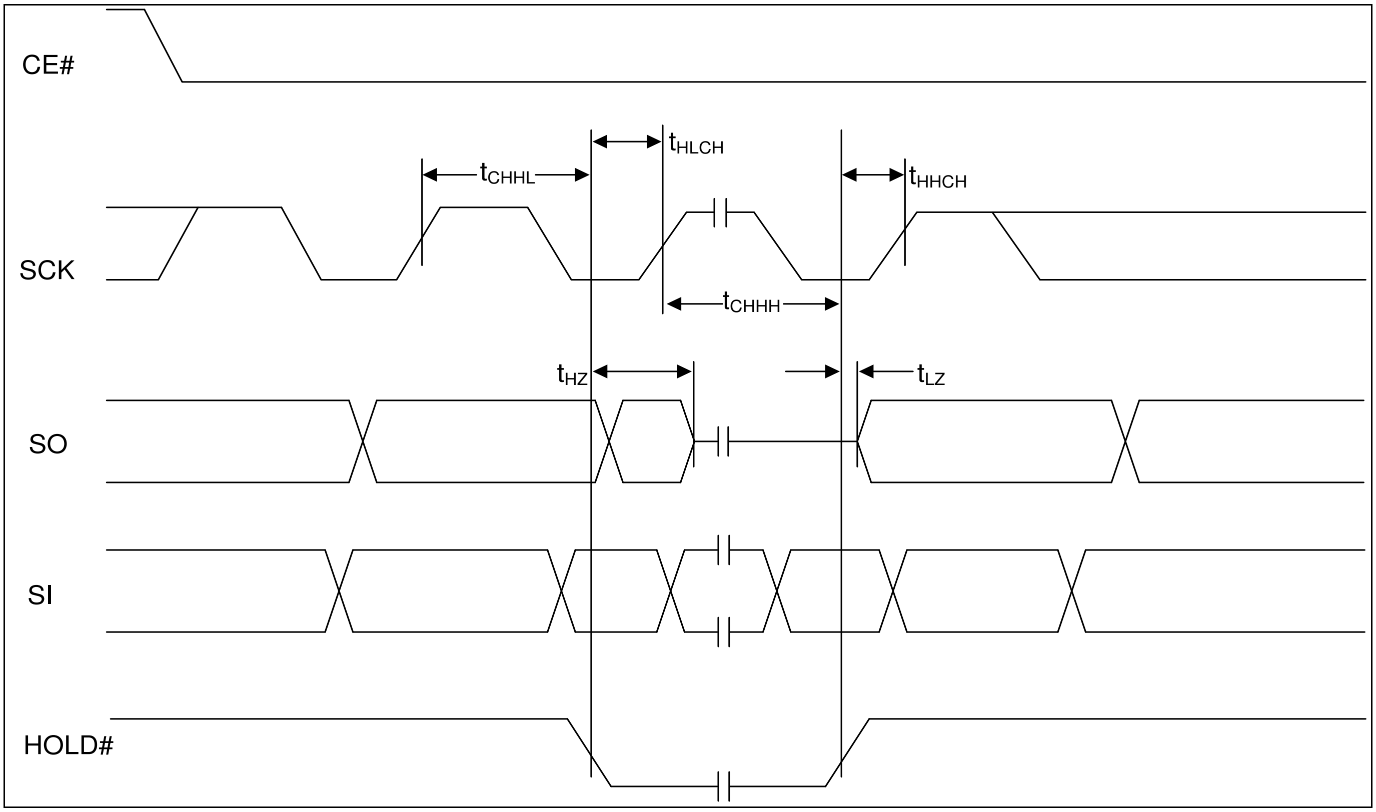


Figure 2. HOLD Timing Diagram

CONFIGURING MULTIPLE SPI DEVICES & MODE 0 AND 3 COMPATIBLE

Multiple devices can be connected together on the SPI serial bus and controlled by a SPI Master controller. Figures 3 and 4 shows how a microcontroller can be connected to control multiple SPI devices.

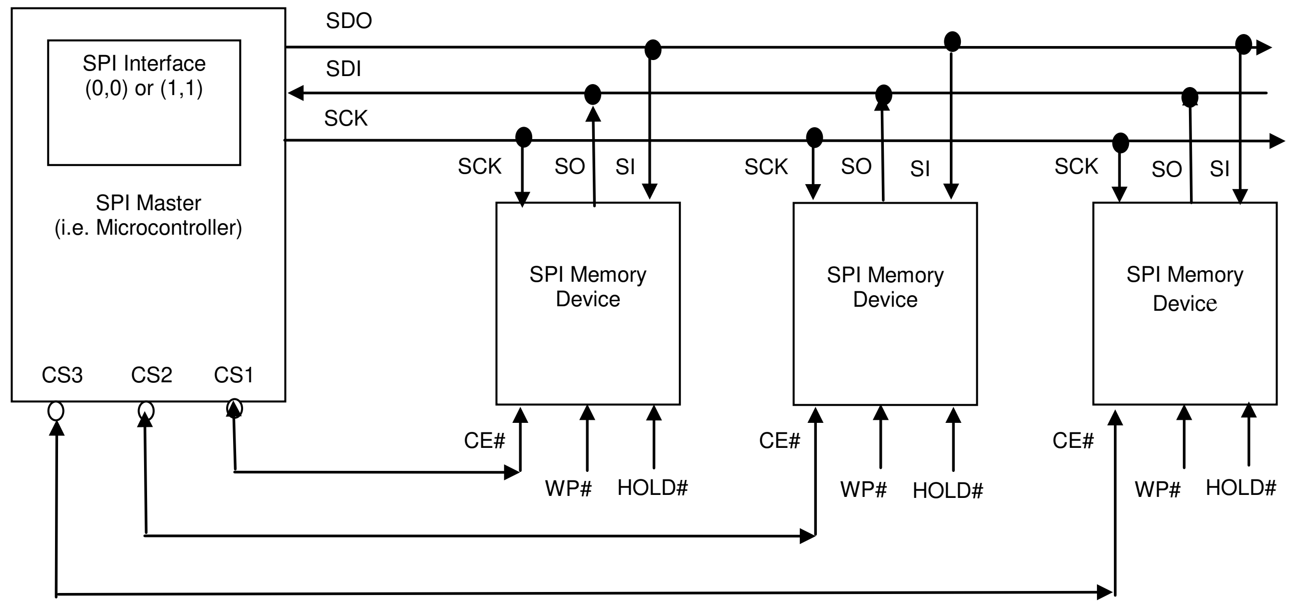
SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash.

For Mode 0 the CLK signal is normally low on the falling and rising edges of CE#. For Mode 3 the CLK signal is normally high on the falling and rising edges of CE#.

The serial clock remains at “0” (SCK = 0) for Mode 0 and for Mode 3 the clock remains at “1” (SCK = 1). Refer to Figure 3 and 4.

In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

These devices are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of any controller equipped with a SPI interface.



Note: 1. The Write Protect (WP #) and Hold (HOLD #) signals should be driven high or low as necessary.

Figure 3. Conceptual Diagram using an SPI Master with Multiple SPI Flash Memory Devices

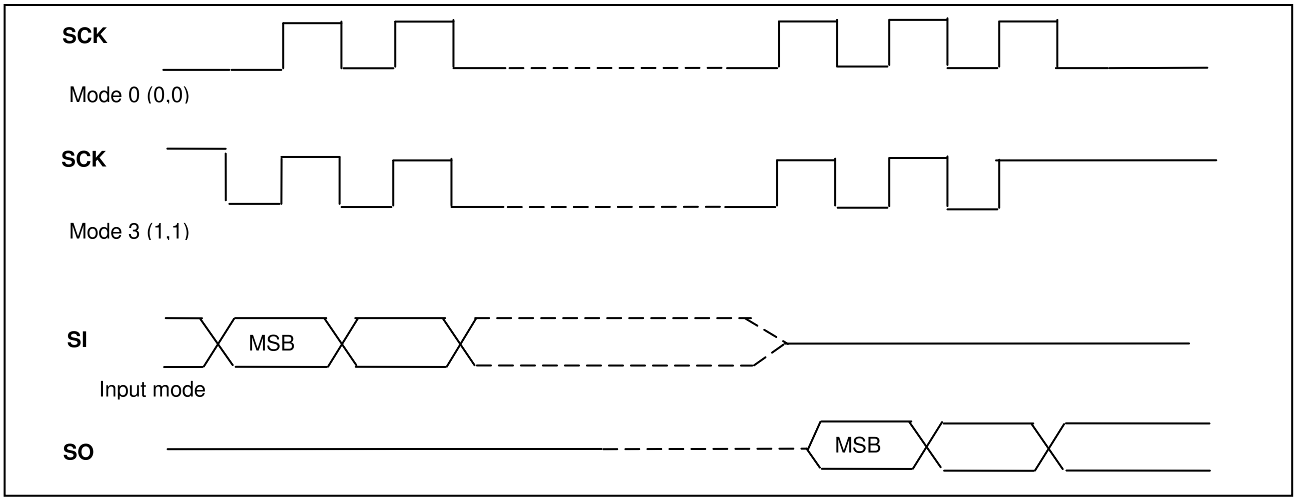


Figure 4. SPI Mode 0 and 3

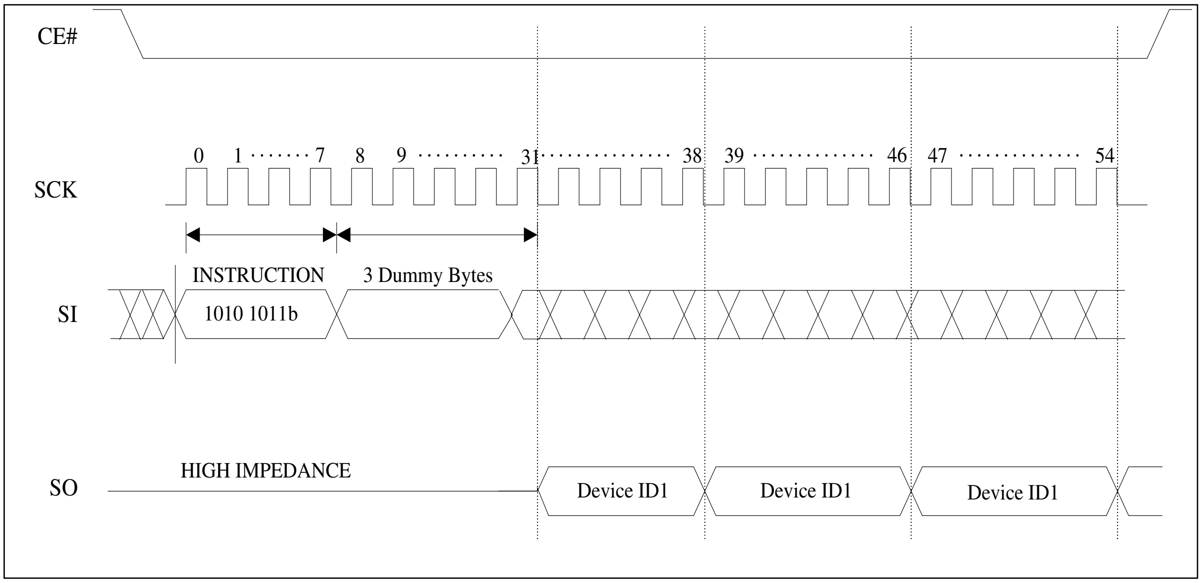
RDID (ABh): READ DEVICE ID AND RELEASE FROM POWER-DOWN

The read device identification (RDID) instruction is for reading out an 8-bit Electronic Signature whose value is shown in Table 7 as Device ID1. The RDID instruction code is followed by three dummy bytes, for a total of four command cycles, each bit being latched-in on SI during the rising edge of SCK. Then Device ID1 is shifted out on SO with the MSB first, each bit being shifted out during the falling edge of SCK. The RDID instruction is ended when CE# goes high. Device ID1 outputs repeatedly if clock cycles continue on SCK and CE# is held low. To release the device from the RDID instruction, drive CE# high as shown in figure 5.

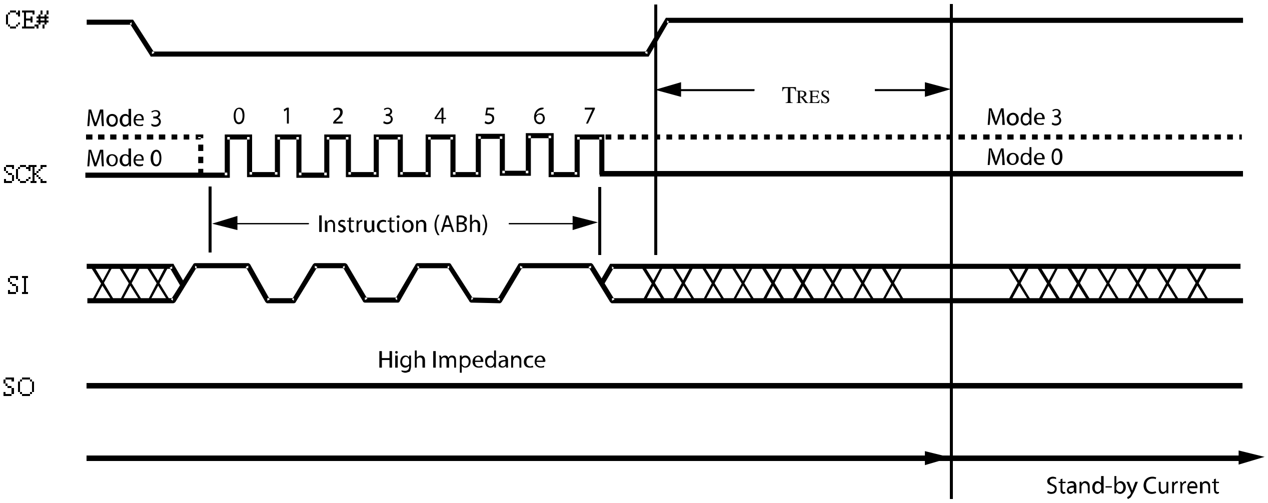
The RDID instruction can also release the device from the power-down state. It is a multi-purpose instruction. To release the device from the power-down state, the instruction is issued by driving the CE# pin low and shifting the instruction code “ABh” and driving CE# high. The CE# pin must remain high during the t_{RES} time duration before the device will resume normal operation and other instructions are accepted.

If the Release from Power-down instruction is issued while an Erase, Program or Write cycle is in process the instruction is ignored and will not have any effects on the current cycle.

The JEDEC ID read instruction is recommended for new designs.



Read Device ID



Release from Power-Down

Figure 5. Read Device ID (Top Diagram) and Release from Power-Down (Bottom Diagram)

JEDEC ID READ (9Fh): Read Manufacture Product Identification by JEDEC ID

For compatibility reasons several instructions are available for electronically obtaining the identity of the device. The JEDEC ID read command was adopted to allow compatibility and identification.

This instruction is initiated by driving the CE# pin low and shifting the instruction code “9Fh”. The JEDEC ID READ instruction allows the user to read Manufacturer ID1, Device ID1, and Device ID2.

The command shifts out the most significant bit on the falling edge of SCK.

If CE# stays low after the last bit of Device ID2 the electronic identification is repeated continuously until CE# is pulled high.

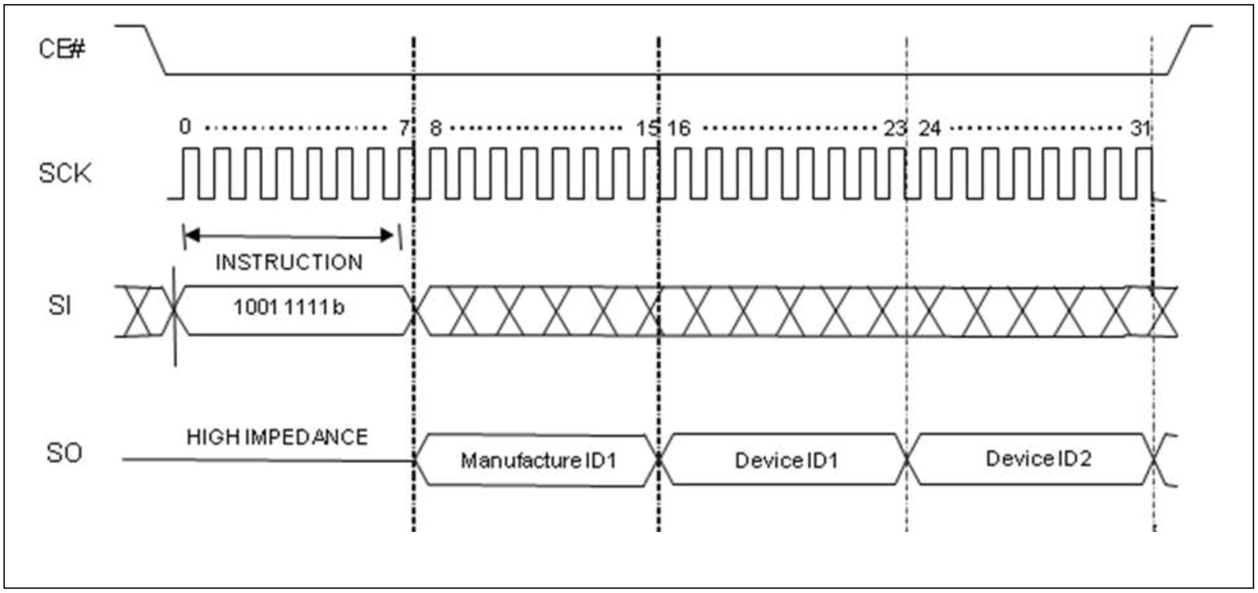


Figure 6. Read Product Identification by JEDEC ID READ Sequence

RDMDID (90h): READ DEVICE MANUFACTURER AND DEVICE ID OPERATION

The Read Device Manufacturer and Device ID instruction is very similar to the RDID instruction. The RDMDID instruction is initiated by driving the CE# pin low and shifting the instruction code “90h” followed by three bytes. Two dummy bytes plus one address byte (A7~A0), each bit being latched-in on SI during the rising edge of SCK.

The Manufacture and Device ID can be read continuously, alternating from one to the others. The instruction is completed by driving CE# high.

If the last bit (A7~A0) is initially set to 0, then Manufacture ID1 -> Device ID1 -> Manufacture ID2 is shifted out on SO with the MSB first. Each bit shifted out during the falling edge of SCK. If A0 = 1, then the output sequence becomes Device ID1 -> Manufacture ID1 -> Manufacture ID2.

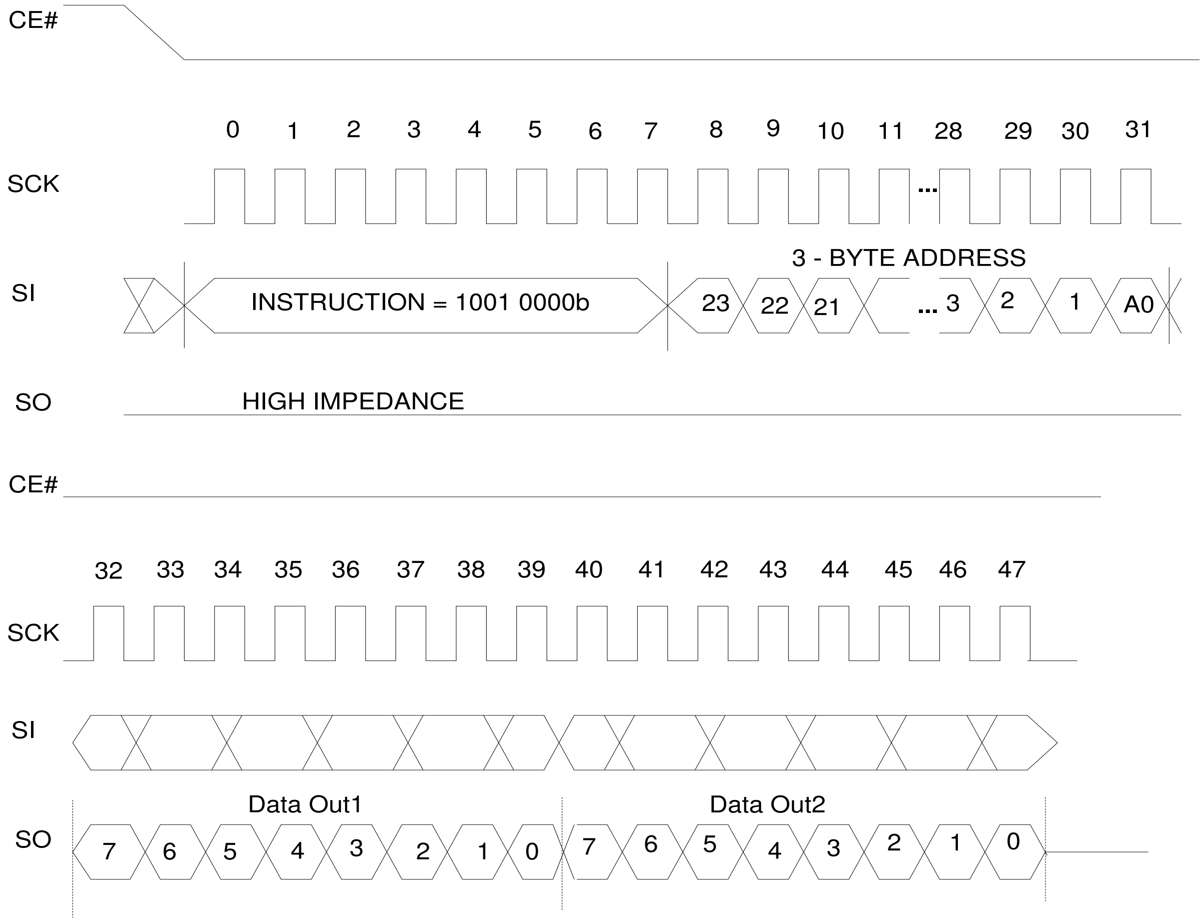


Figure 7. Read Product Identification by RDMDID READ Sequence

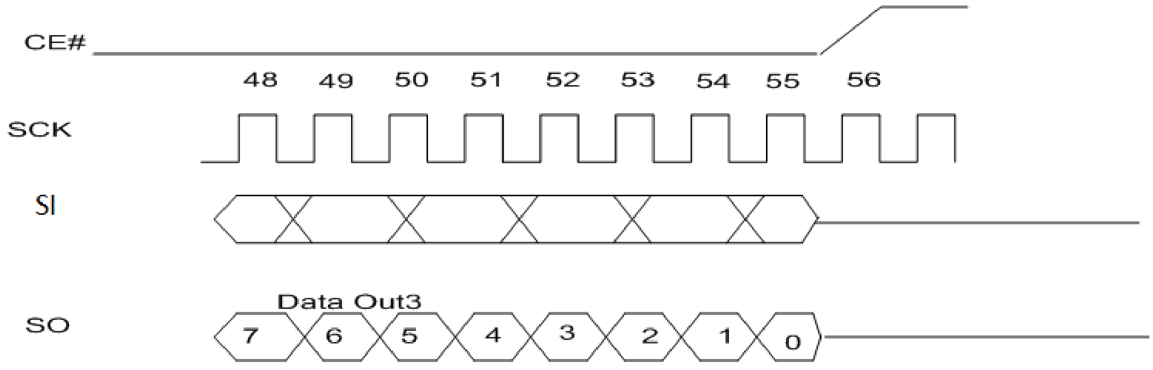


Figure 7. (cont.) Read Product Identification by RDMDID READ Sequence

Note : 1. ADDRESS A0 = 0, will output the Manufacture ID1 -> Device ID1 -> Manufacture ID2
2. ADDRESS A0 = 1, will output the Device ID1 -> Manufacture ID1 -> Manufacture ID2

WREN (06h): WRITE ENABLE OPERATION

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit is reset to the write protected state after power-up. The WEL bit must be write enabled before any write operation, including sector, block erase, chip erase, page program, and write status register. The WEL bit will be reset to the write-protect state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

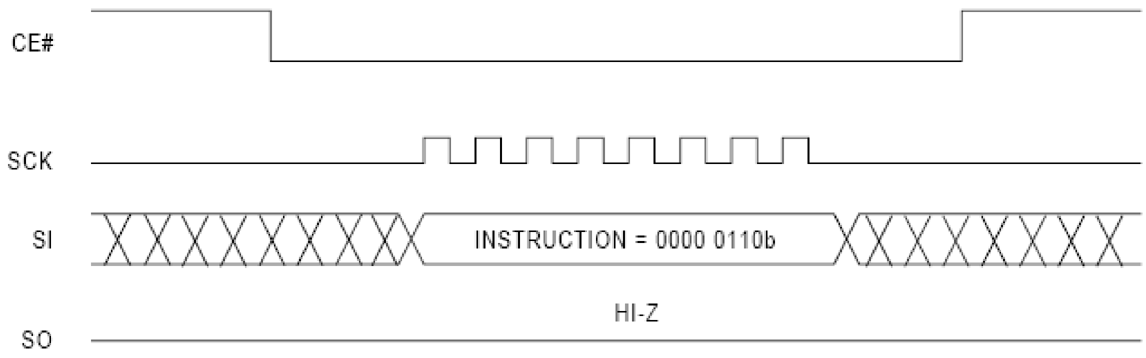


Figure 8. Write Enable Sequence

WRDI (04h): WRITE DISABLE OPERATION

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CE# low, shifting the instruction code “04h” into the SI pin and then driving CE# high. The WEL bit is automatically reset after power-up and upon completion of the Write Status Register, Page Program, Quad Page Program, Sector Erase, Block Erase and Chip Erase.

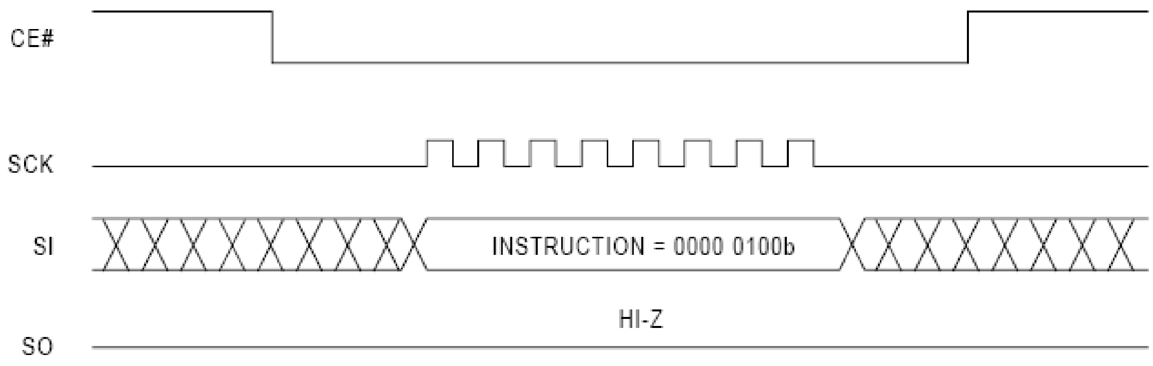


Figure 9. Write Disable Sequence

RDSR (05h): READ STATUS REGISTER OPERATION

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write status register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of the Status Register.

The instruction is entered by driving CE# low and shifting the instruction code “05h”into the SI pin on the rising edge of SCK. The status register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving CE# high.

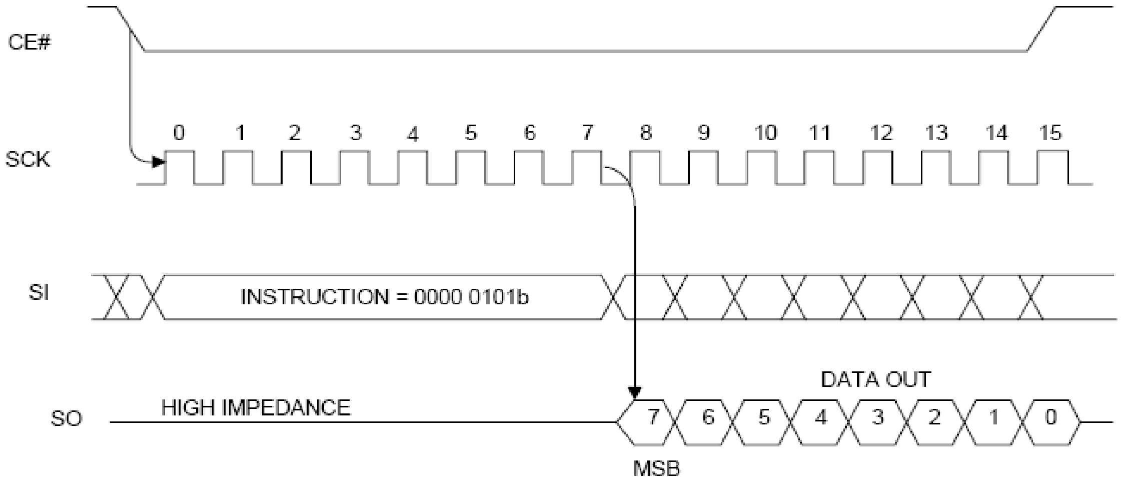


Figure 10. Read Status Register Sequence

WRSR (01h): WRITE STATUS REGISTER OPERATION

The Write Status Register (WRSR) instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CE# low, sending the instruction code “01h”, and then writing the status register data into the non-volatile BP3, BP2, BP1, BP0, QE, and SRWD bits. The user can enable or disable the block protection and status register write protection features by writing “0”s or “1”s.

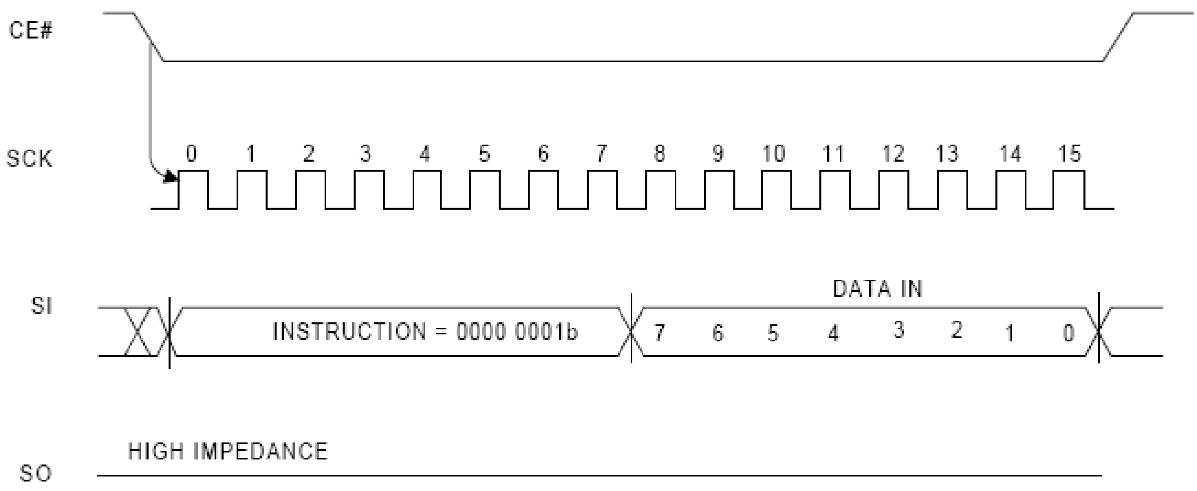


Figure 11. Write Status Register Sequence

READ (03h): READ DATA OPERATION

The READ instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MS} (most significant address) - A0 are decoded. The remaining bits (A23 – A_{MS}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI pin will be ignored. Refer to Table 9 for the related Address Key.

The first byte data (D7 - D0) addressed is then shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one READ instruction. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH). When the highest address of the devices is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

If a Read Data instruction is issued while an Erase, Program, or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

The Read Data instruction allows clock rates from D.C. to a maximum of f_C (see AC Electrical Characteristics).

Address	IS25LQ080
A_{N} $(A_{MS} – A_{0})$	A21 - A0
Don't Care Bits	A23 – A22

Table 9. Address Key

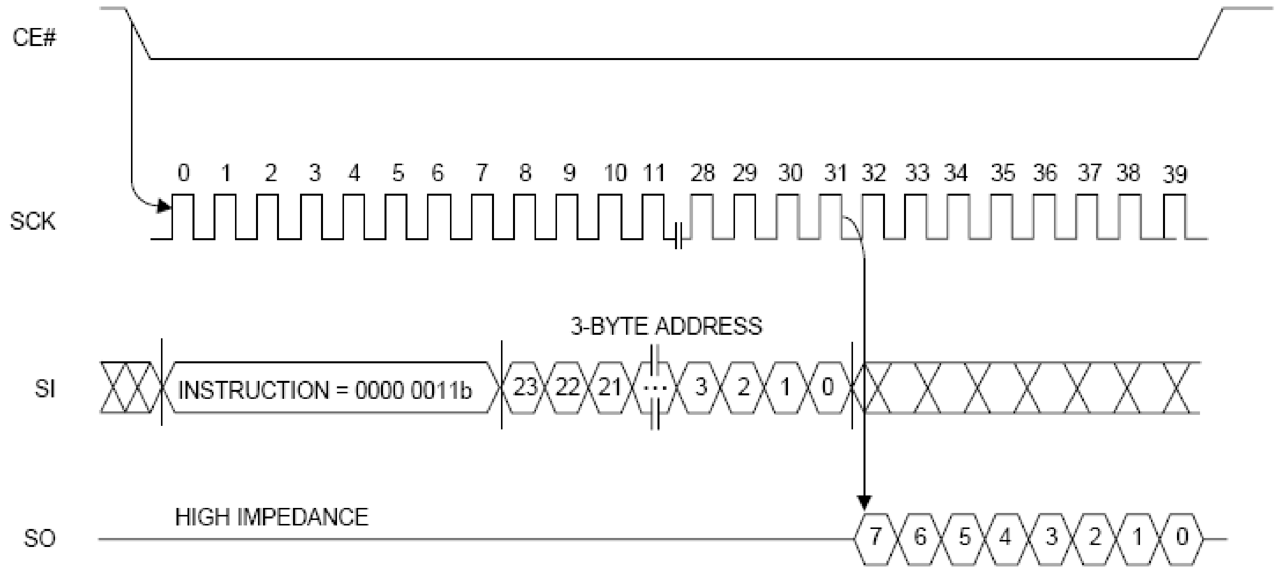


Figure 12. Read Data Sequence

FAST_READ (0Bh): FAST READ DATA OPERATION

The FAST_READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. The dummy byte allows the devices internal circuits additional time for setting up the initial address. During the dummy cycle the data value on the SI pin is a “don’t care”.

The FAST_READ instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of f_{CT} (see AC Electrical Characteristics).

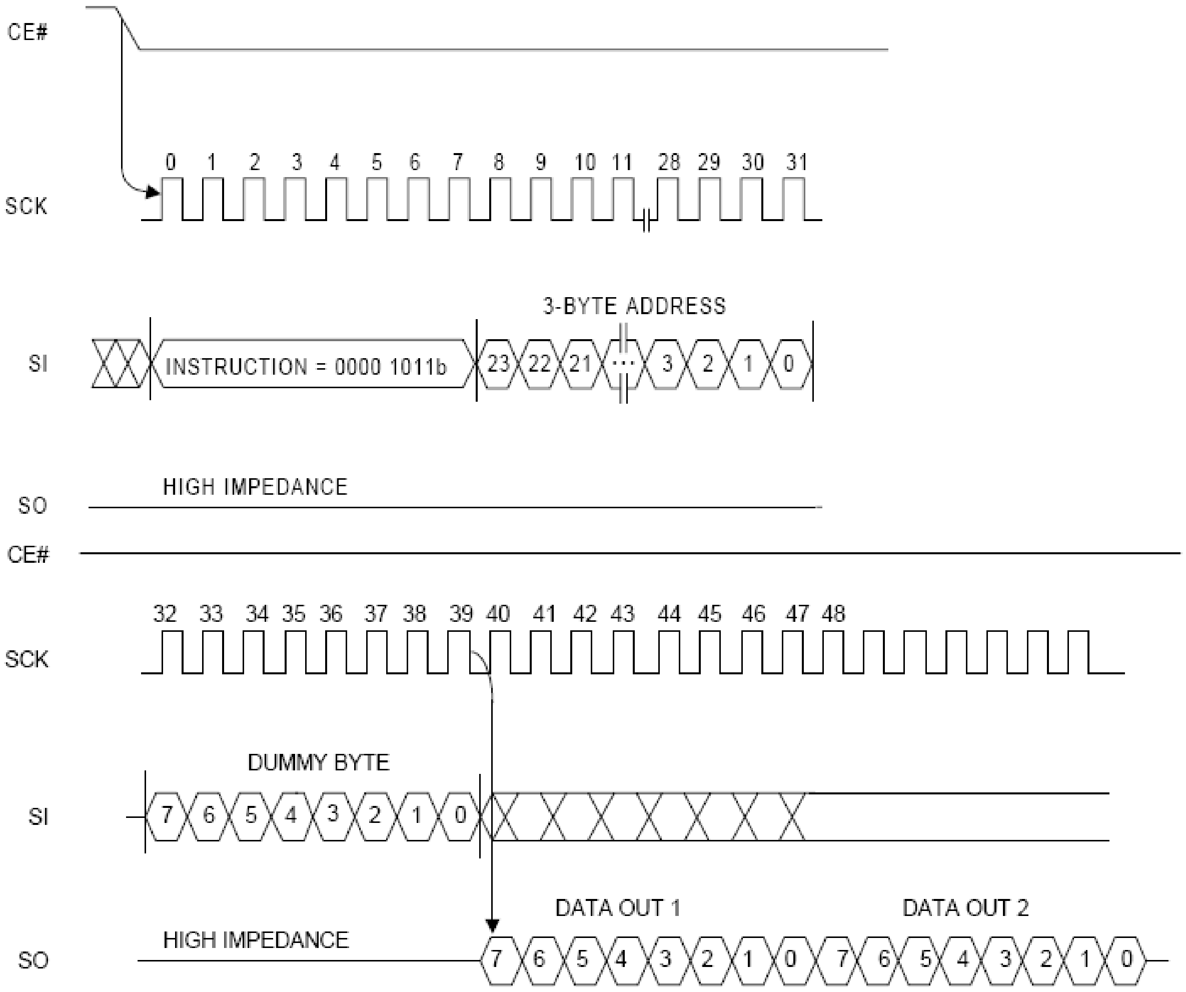


Figure 13. Fast Read Data Sequence

FRDO (3Bh): FAST READ DUAL OUTPUT OPERATION

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast_Read (0Bh) instruction except that data is output on two pins. This allows data to be transferred from the device at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code. Similar to the Fast_Read instruction, FRDO instruction can operate at the highest possible frequency of f_{CT} (see AC Electrical Characteristics).

This is accomplished by adding 1 dummy byte after the 24-bit address as. The dummy cycle allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy byte is "don't care".

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving CE# high (VIH). If a FRDO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

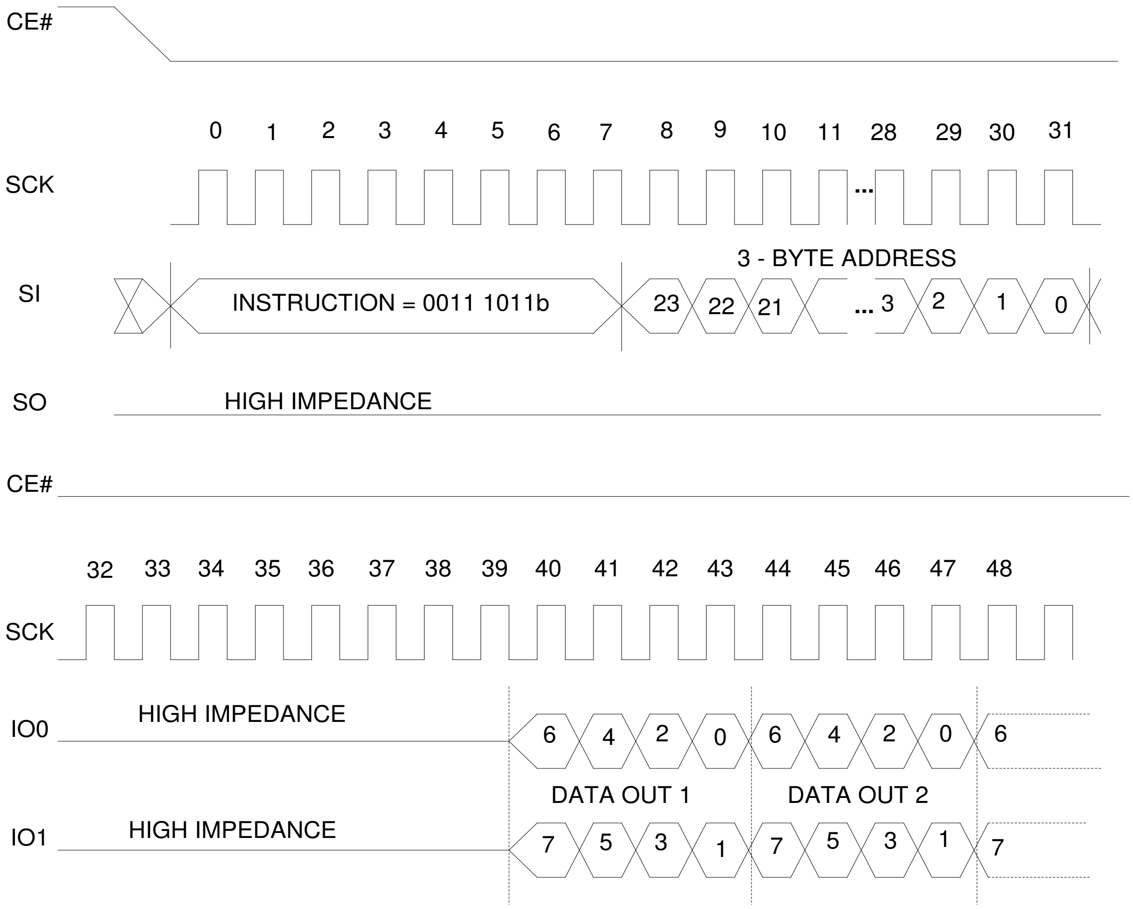


Figure 14. Fast Read Dual-Output Sequence

FRDIO (BBh): FAST READ DUAL I/O OPERATION

The FRDIO instruction is similar to the FRDO instruction, but allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications (XIP).

The FRDIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO0 and IO1 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and continues to shift in alternating on the two pins. The mode byte contains the value Ax, where x is a "don't care" value.

The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The MSB is output on IO1, while simultaneously the next bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

The device remains in this mode until it receives a Mode Reset (FFh) command. In subsequent FRDIO execution, the command code is not input, saving timing cycles. If a FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

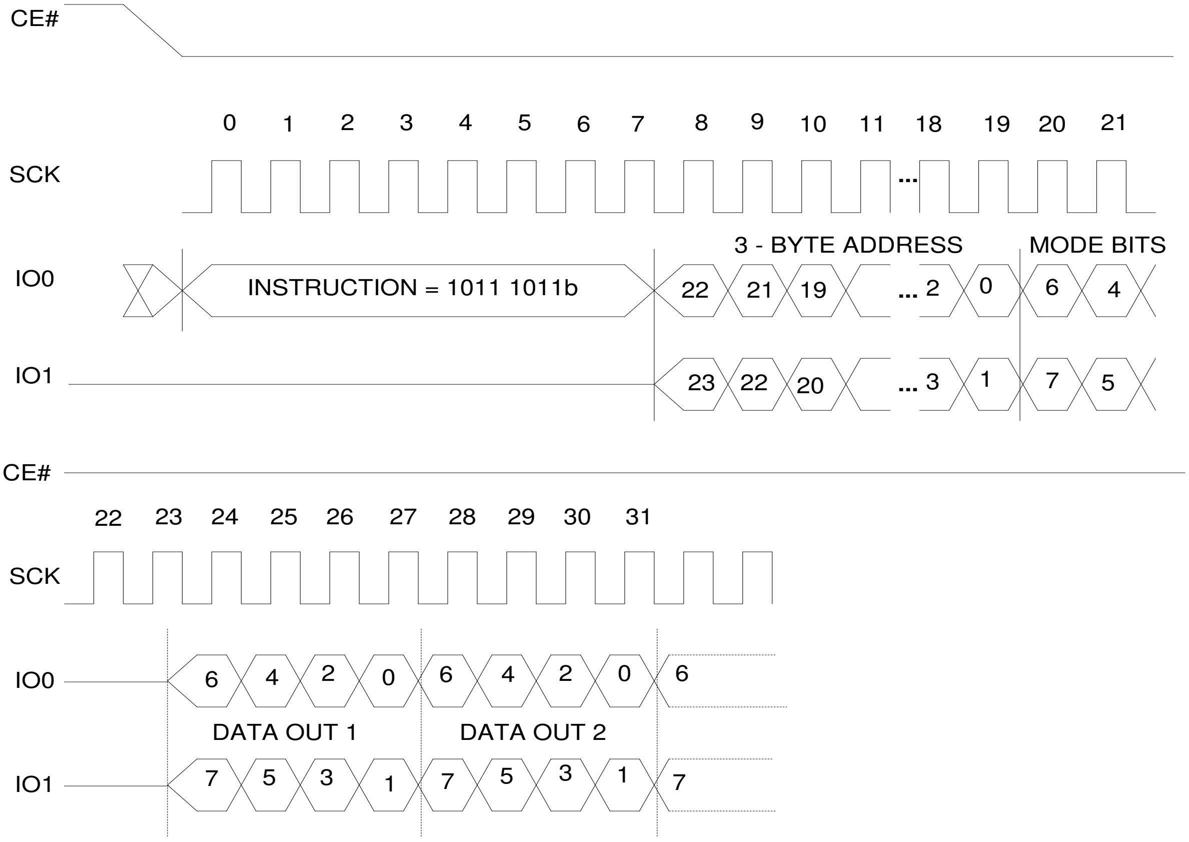


Figure 15. Fast Read Dual I/O Sequence (with command decode cycles)

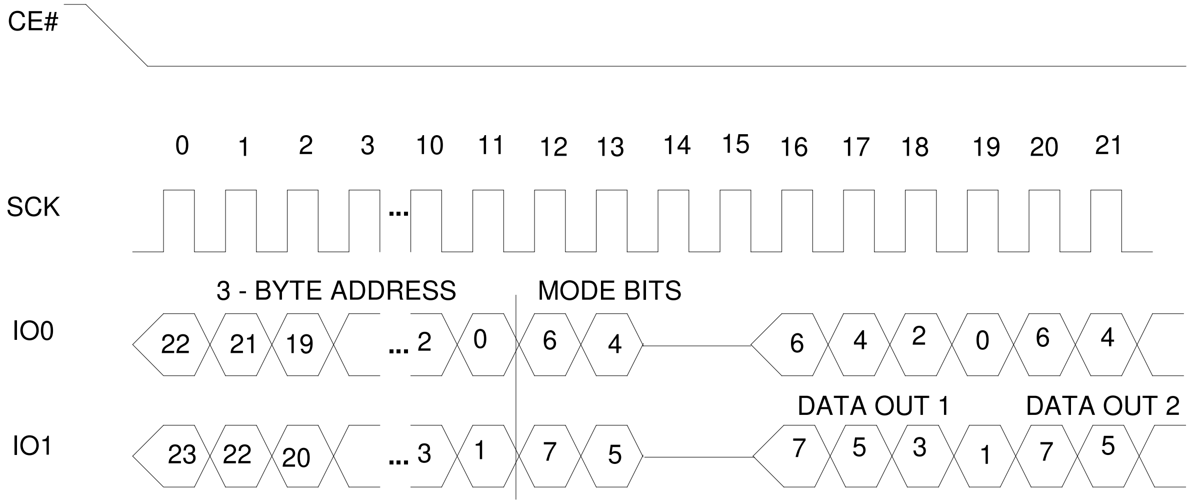


Figure 16. Fast Read Dual I/O Sequence (without command decode cycles)

FRQO (6Bh): FAST READ QUAD OUTPUT OPERATION

The FRQO instruction code is followed by three address bytes (A23 – A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. The first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each group of four bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, and the third bit is output on IO1, etc.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQO instruction. FRQO instruction is terminated by driving CE# high (VIH). If a FRQO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.