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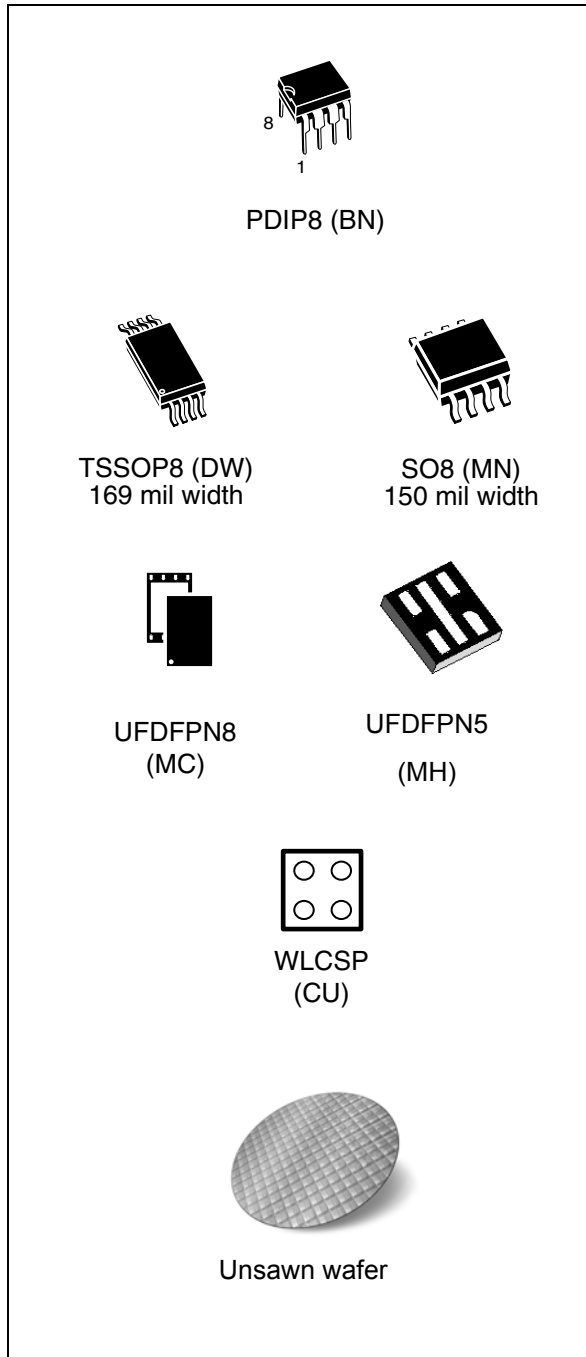
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### Features

- Compatible with all I<sup>2</sup>C bus modes:
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 32 Kbit (4 Kbyte) of EEPROM
  - Page size: 32 byte
  - Additional Write lockable page (M24C32-D order codes)
- Single supply voltage:
  - 1.7 V to 5.5 V over –40 °C / +85 °C
  - 1.6 V to 5.5 V over –20 °C / +85 °C
- Write:
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-years data retention

### Packages

- PDIP8 ECOPACK1<sup>®</sup>
- SO8 ECOPACK2<sup>®</sup>
- TSSOP8 ECOPACK2<sup>®</sup>
- UFDFPN8 ECOPACK2<sup>®</sup>
- WLCSP ECOPACK2<sup>®</sup>
- UFDFPN5 ECOPACK2<sup>®</sup>
- Unsawn wafer (each die is tested)

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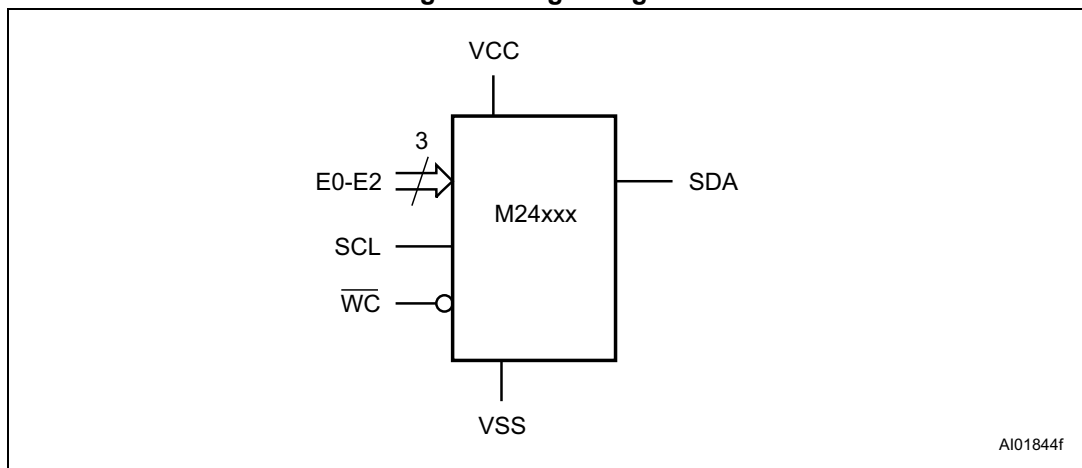
# 1 Description

The M24C32 is a 32-Kbit I<sup>2</sup>C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 4 K × 8 bits.

The M24C32-W can operate with a supply voltage from 2.5 V to 5.5 V, the M24C32-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M24C32-F and M24C32-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C; while the M24C32-X can operate with a supply voltage from 1.6 V to 5.5 V over an ambient temperature range of -20 °C / +85 °C.

The M24C32-D offers an additional page, named the Identification Page (32 byte). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

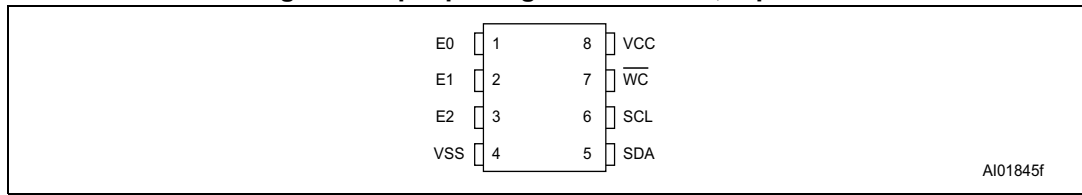
**Figure 1. Logic diagram**



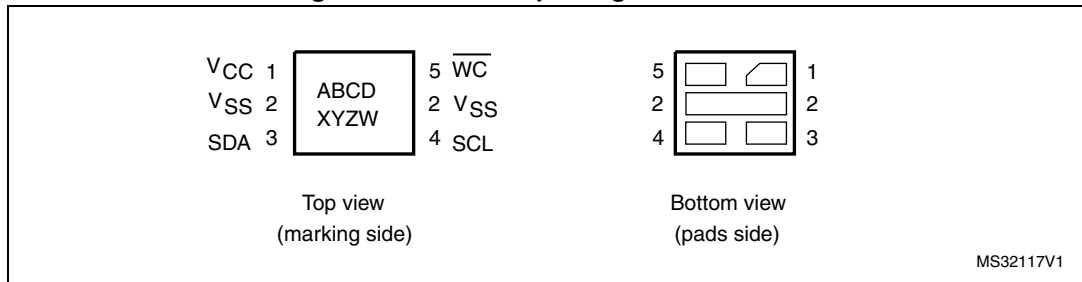
**Table 1. Signal names**

Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V <sub>CC</sub>	Supply voltage	-
V <sub>SS</sub>	Ground	-

**Figure 2. 8-pin package connections, top view**

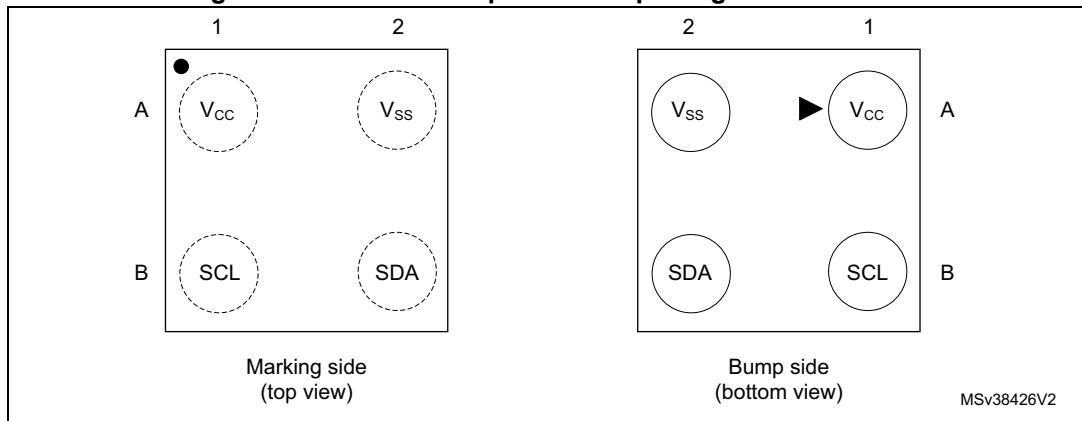


**Figure 3. UDFPN5 package connections**



1. Inputs E2, E1, E0 are not connected, therefore read as (000). Please refer to [Section 2.3](#) for further explanations.

**Figure 4. WLCSP 4 bump Ultra thin package connections**



1. Inputs E2, E1, E0 are read as (000). Please refer to [Section 2.3](#) for further explanations.

**Table 2. Signals vs. bump position**

Position	A	B
1	V <sub>CC</sub>	SCL
2	V <sub>SS</sub>	SDA



## 2 Signal description

### 2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

### 2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to  $V_{CC}$  (Figure 13 indicates how to calculate the value of the pull-up resistor).

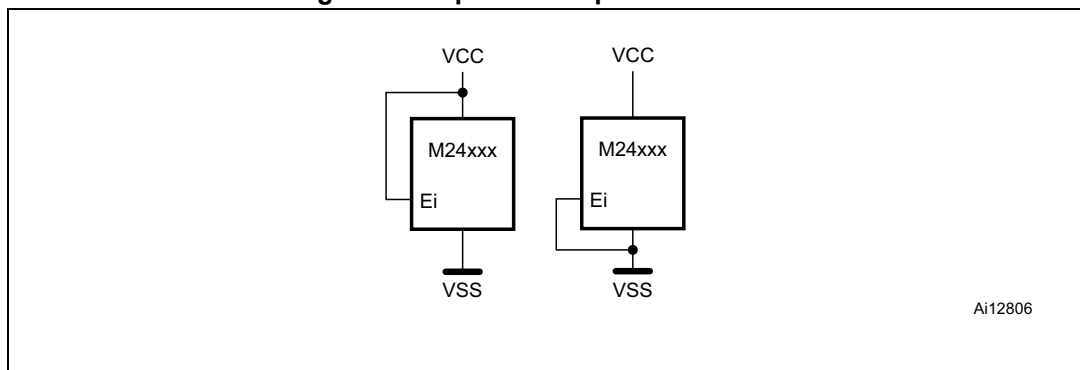
### 2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see Table 3). These inputs must be tied to  $V_{CC}$  or  $V_{SS}$ , as shown in Figure 5. When not connected (left floating), these inputs are read as low (0).

For the UDFFPN5 package, the (E2,E1,E0) inputs are not connected, therefore read as (0,0,0).

For the 4-balls WLCSP package (see Figure 4), the (E2,E1,E0) inputs are internally connected to (0, 0, 0).

Figure 5. Chip enable inputs connection



### 2.4 Write Control ( $\overline{WC}$ )

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ( $\overline{WC}$ ) is driven high. Write operations are enabled when Write Control ( $\overline{WC}$ ) is either driven low or left floating.

When Write Control ( $\overline{WC}$ ) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

## 2.5 $V_{SS}$ (ground)

$V_{SS}$  is the reference for the  $V_{CC}$  supply voltage.

## 2.6 Supply voltage ( $V_{CC}$ )

### 2.6.1 Operating supply voltage ( $V_{CC}$ )

Prior to selecting the memory and issuing instructions to it, a valid and stable  $V_{CC}$  voltage within the specified [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range must be applied (see Operating conditions in [Section 8: DC and AC parameters](#)). In order to secure a stable DC supply voltage, it is recommended to decouple the  $V_{CC}$  line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the  $V_{CC}/V_{SS}$  package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle ( $t_W$ ).

### 2.6.2 Power-up conditions

The  $V_{CC}$  voltage has to rise continuously from 0 V up to the minimum  $V_{CC}$  operating voltage (see Operating conditions in [Section 8: DC and AC parameters](#)).

### 2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until  $V_{CC}$  has reached the internal reset threshold voltage. This threshold is lower than the minimum  $V_{CC}$  operating voltage (see Operating conditions in [Section 8: DC and AC parameters](#)). When  $V_{CC}$  passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until  $V_{CC}$  reaches a valid and stable DC voltage within the specified [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range (see Operating conditions in [Section 8: DC and AC parameters](#)).

In a similar way, during power-down (continuous decrease in  $V_{CC}$ ), the device must not be accessed when  $V_{CC}$  drops below  $V_{CC}(\min)$ . When  $V_{CC}$  drops below the internal reset threshold voltage, the device stops responding to any instruction sent to it.

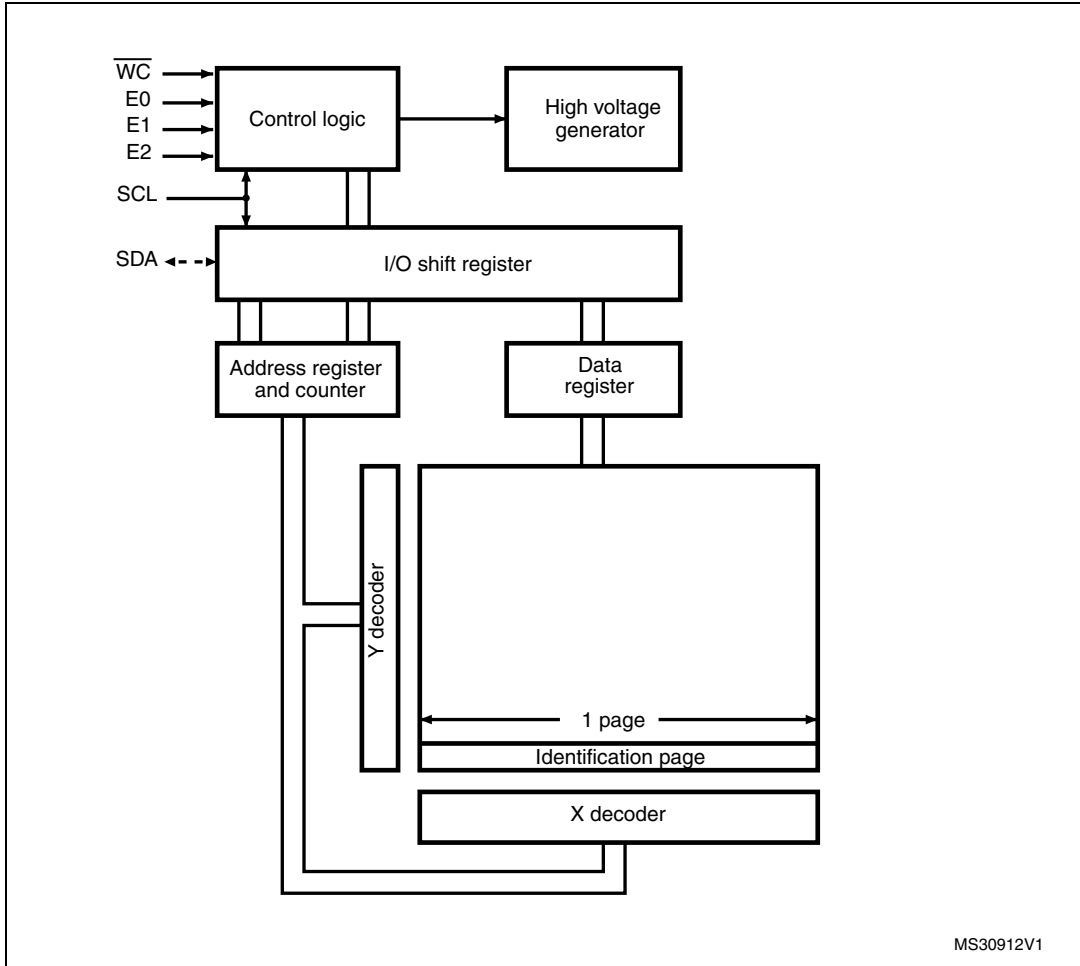
### 2.6.4 Power-down conditions

During power-down (continuous decrease in  $V_{CC}$ ), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

### 3 Memory organization

The memory is organized as shown below.

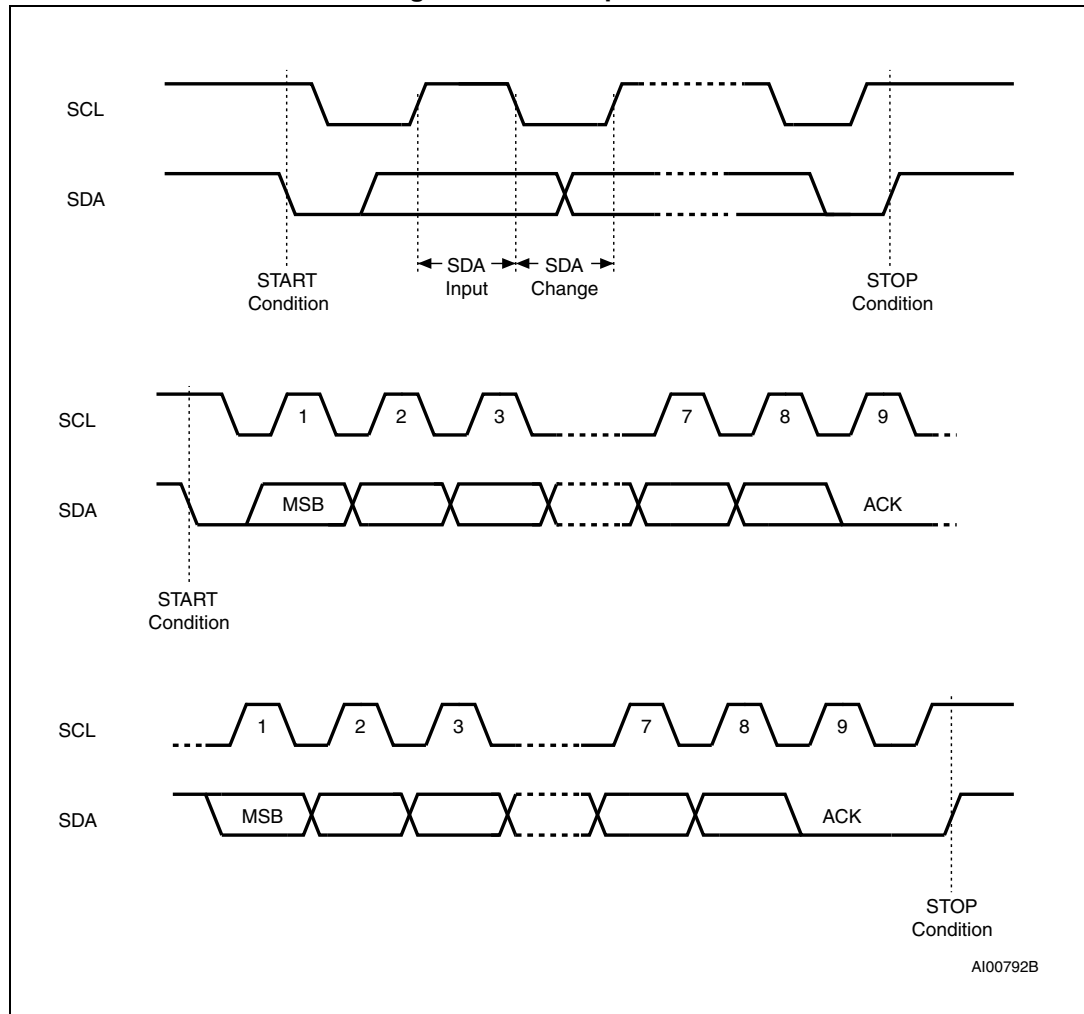
Figure 6. Block diagram



## 4 Device operation

The device supports the I<sup>2</sup>C protocol. This is summarized in [Figure 7](#). Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 7. I<sup>2</sup>C bus protocol



## 4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

## 4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

## 4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

## 4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9<sup>th</sup> clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in [Table 3](#) (most significant bit first).

**Table 3. Device select code**

	Device type identifier <sup>(1)</sup>				Chip Enable address <sup>(2)</sup>			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	$\overline{RW}$
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	$\overline{RW}$

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared with the value read on input pins E0, E1 and E2.

When the device select code is received, the device only responds if the Chip Enable address is the same as the value on its Chip Enable E2,E1,E0 inputs.

The 8<sup>th</sup> bit is the Read/Write bit ( $\overline{RW}$ ). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9<sup>th</sup> bit time. If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode.

## 5 Instructions

### 5.1 Write operations

Following a Start condition the bus master sends a device select code with the  $\overline{R/\overline{W}}$  bit ( $\overline{RW}$ ) reset to 0. The device acknowledges this, as shown in [Figure 8](#), and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

**Table 4. Most significant address byte**

A15	A14	A13	A12	A11	A10	A9	A8
-----	-----	-----	-----	-----	-----	----	----

**Table 5. Least significant address byte**

A7	A6	A5	A4	A3	A2	A1	A0
----	----	----	----	----	----	----	----

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10<sup>th</sup> bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle  $t_W$  is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle ( $t_W$ ), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

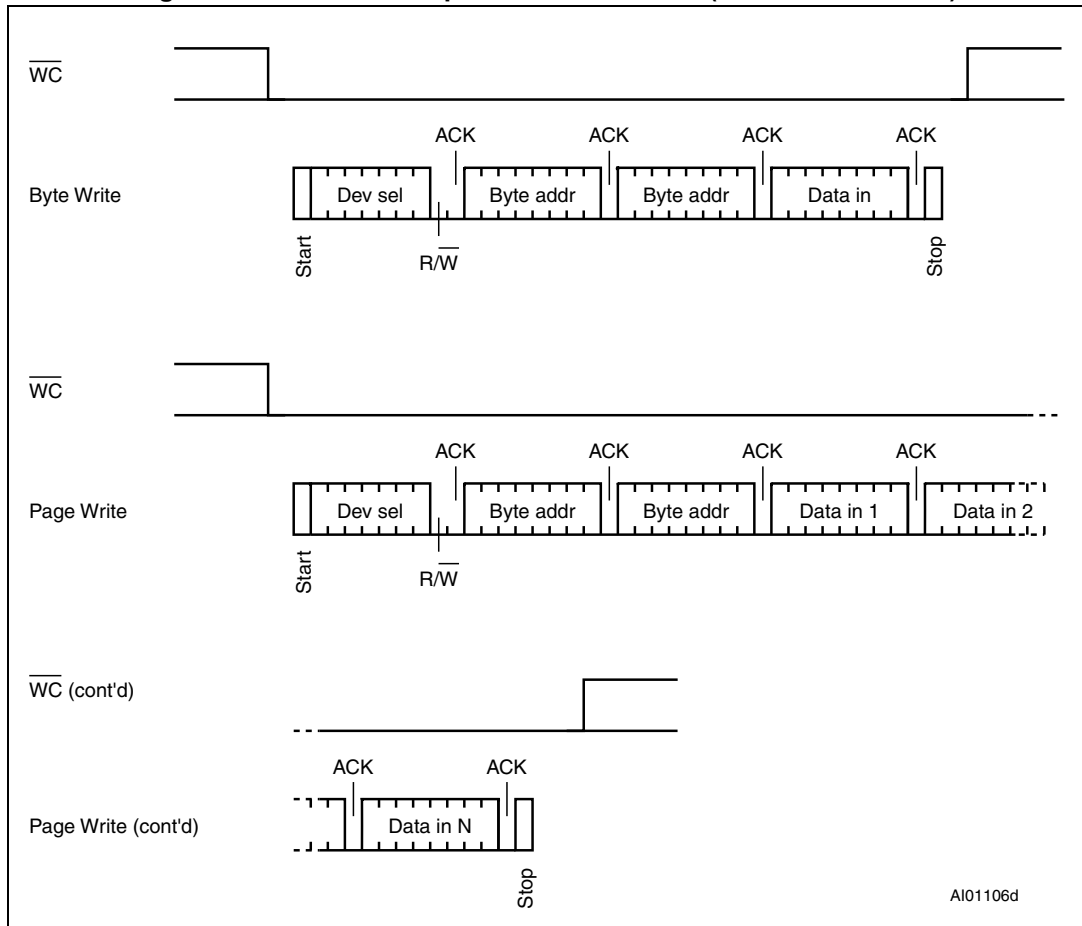
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in [Figure 9](#).

### 5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ( $\overline{WC}$ ) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 8*.

**Figure 8. Write mode sequences with  $\overline{WC} = 0$  (data write enabled)**





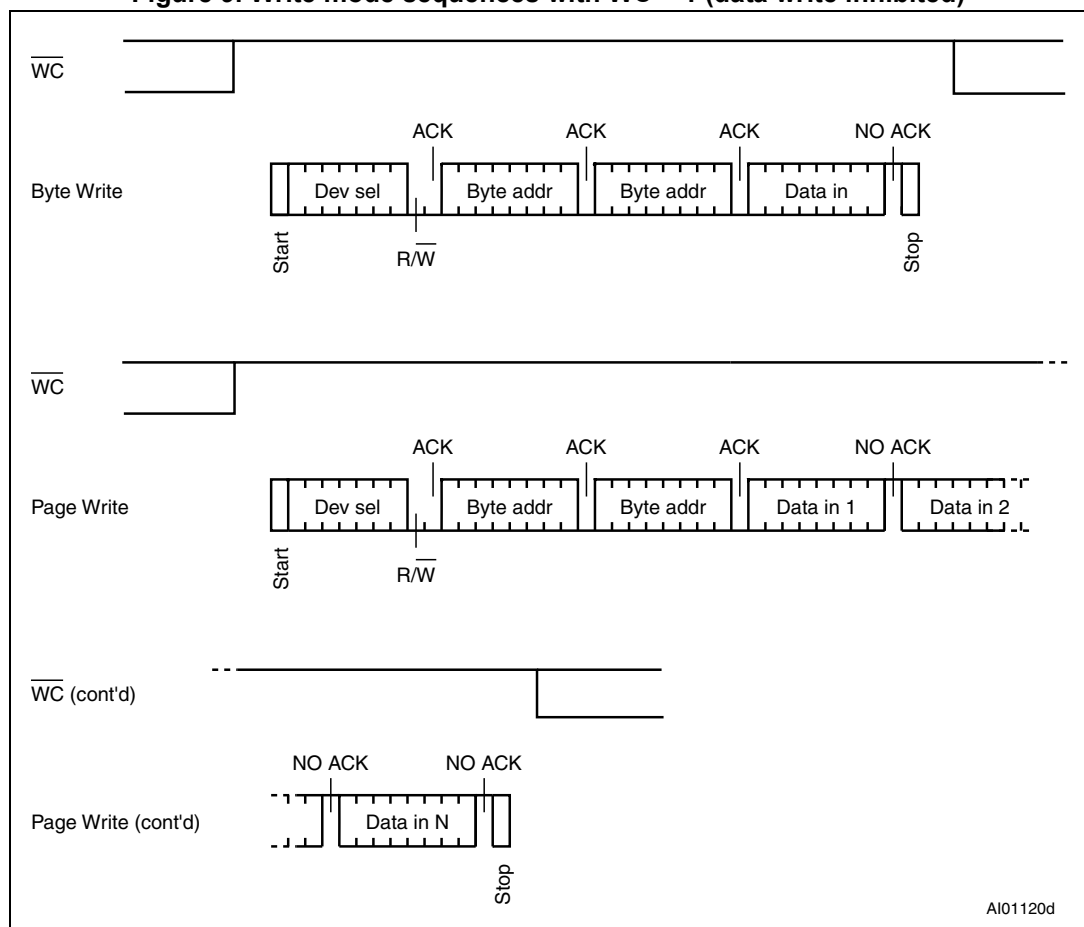
### 5.1.2 Page Write

The Page Write mode allows up to 32 byte to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, b16-b5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 byte of data, each of which is acknowledged by the device if Write Control ( $\overline{WC}$ ) is low. If Write Control ( $\overline{WC}$ ) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 9*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

**Figure 9. Write mode sequences with  $\overline{WC} = 1$  (data write inhibited)**



### 5.1.3 Write Identification Page (M24C32-D only)

The Identification Page (32 byte) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/A5 are don't care except for address bit A10 which must be '0'. LSB address bits A4/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

### 5.1.4 Lock Identification Page (M24C32-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

### 5.1.5 ECC (Error Correction Code) and Write cycling

The ECC is offered only in devices identified with process letter K, all other devices (identified with a different process letter) do not embed the ECC logic.

The Error Correction Code (ECC) is an internal logic function which is transparent for the I<sup>2</sup>C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes<sup>(1)</sup>. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group<sup>(1)</sup>. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined [Table 13: Cycling performance](#).

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1. A group of four bytes is located at addresses [4\*N, 4\*N+1, 4\*N+2, 4\*N+3], where N is an integer.

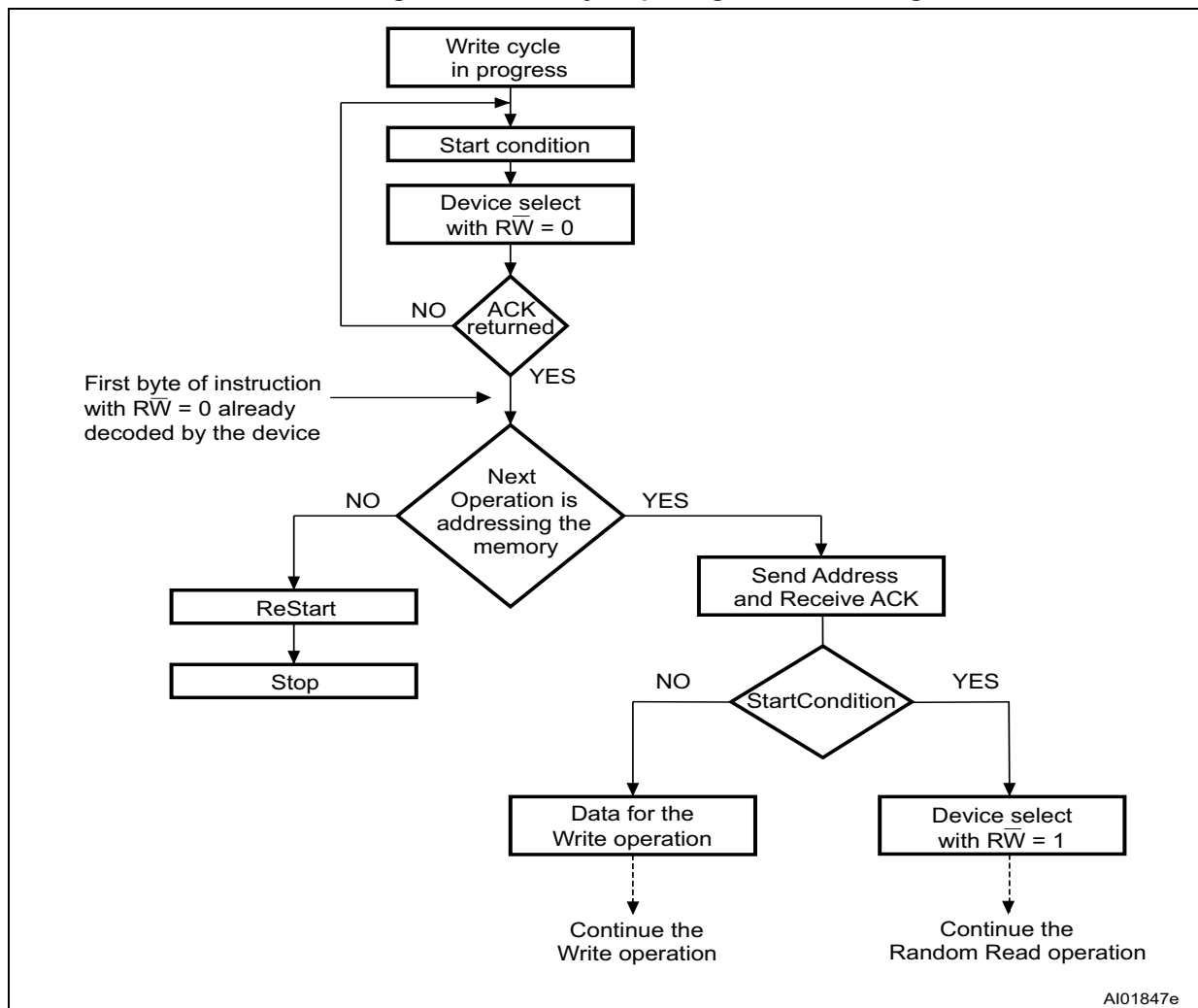
### 5.1.6 Minimizing Write delays by polling on ACK

The maximum Write time ( $t_w$ ) is shown in AC characteristics tables in [Section 8: DC and AC parameters](#), but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in [Figure 10](#), is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

**Figure 10. Write cycle polling flowchart using ACK**



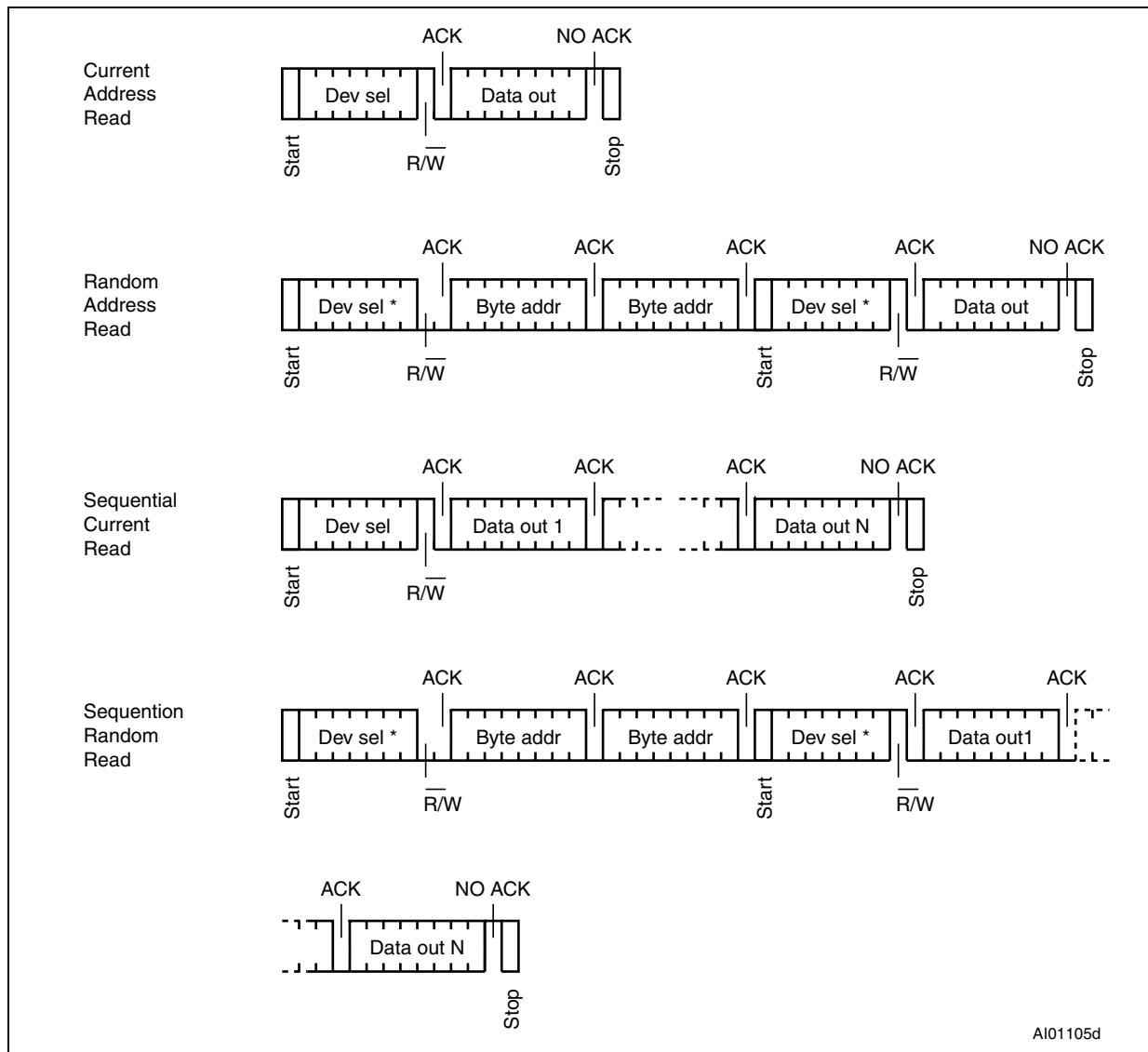
1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

## 5.2 Read operations

Read operations are performed independently of the state of the Write Control ( $\overline{WC}$ ) signal. After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 11. Read mode sequences



### 5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in [Figure 11](#)) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the  $\overline{RW}$  bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

### 5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the  $R/\overline{W}$  bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in [Figure 11](#), *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the byte location in the Identification page, therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory, see [Section 5.2.1](#)) instead of the Current Address Read instruction.

### 5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in [Figure 11](#).

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

### 5.2.4 Read Identification Page (M24C32-D only)

The Identification Page (32 byte) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 byte).

### 5.2.5 Read the lock status (M24C32-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

## 6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

When delivered in unsawn wafer, all memory bits are set to 1 (each memory byte contains FFh) except the last byte located at address FFFh which is written with the value 22h.

## 7 Maximum rating

Stressing the device outside the ratings listed in [Table 6](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6. Absolute maximum ratings**

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	-40	130	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C
T <sub>LEAD</sub>	Lead temperature during soldering	see note <sup>(1)</sup>		°C
	PDIP-specific lead temperature during soldering	-	260 <sup>(2)</sup>	°C
I <sub>OL</sub>	DC output current (SDA = 0)	-	5	mA
V <sub>IO</sub>	Input or output range	-0.50	6.5	V
V <sub>CC</sub>	Supply voltage	-0.50	6.5	V
V <sub>ESD</sub>	Electrostatic pulse (Human Body model) <sup>(3)</sup>	-	3000 <sup>(4)</sup>	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. T<sub>LEAD</sub> max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012 standard, C1=100 pF, R1=1500 Ω).
4. 4000 V for devices identified with process letter K and P.



## 8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

**Table 7. Operating conditions (voltage range W)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	2.5	5.5	V
$T_A$	Ambient operating temperature	-40	85	°C
$f_C$	Operating clock frequency	-	1 <sup>(1)</sup>	MHz

1. 400 kHz for devices identified by process letter P.

**Table 8. Operating conditions (voltage range R)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	1.8	5.5	V
$T_A$	Ambient operating temperature	-40	85	°C
$f_C$	Operating clock frequency	-	1 <sup>(1)</sup>	MHz

1. 400 kHz for devices by process letter P.

**Table 9. Operating conditions (voltage range F)**

Symbol	Parameter	Min.		Max.	Unit
$V_{CC}$	Supply voltage	1.6 <sup>(1)</sup>	1.7	5.5	V
$T_A$	Ambient operating temperature: READ	-40	-40	85	°C
	Ambient operating temperature: WRITE	0	-40	85	
$f_C$	Operating clock frequency, $V_{CC} \geq 1.6$ V <sup>(1)</sup>	-		400	kHz
	Operating clock frequency, $V_{CC} \geq 1.7$ V	-		1000	

1. Only for devices identified with process letter T

**Table 10. Operating conditions (voltage range X)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	1.6	5.5	V
$T_A$	Ambient operating temperature	-20	85	°C
$f_C$	Operating clock frequency	-	1	MHz

Table 11. Input parameters

Symbol	Parameter <sup>(1)</sup>	Test condition	Min.	Max.	Unit
C <sub>IN</sub>	Input capacitance (SDA)	-	-	8	pF
C <sub>IN</sub>	Input capacitance (other pins)	-	-	6	pF
Z <sub>L</sub>	Input impedance (E2, E1, E0, $\overline{WC}$ ) <sup>(2)</sup>	V <sub>IN</sub> < 0.3 V <sub>CC</sub>	30	-	kΩ
Z <sub>H</sub>		V <sub>IN</sub> > 0.7 V <sub>CC</sub>	500	-	kΩ

1. Characterized only, not tested in production.
2. E2, E1, E0 input impedance when the memory is selected (after a Start condition).

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C <sub>bus</sub>	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V <sub>CC</sub> to 0.8 V <sub>CC</sub>		V
-	Input and output timing reference levels	0.3 V <sub>CC</sub> to 0.7 V <sub>CC</sub>		V

Figure 12. AC measurement I/O waveform

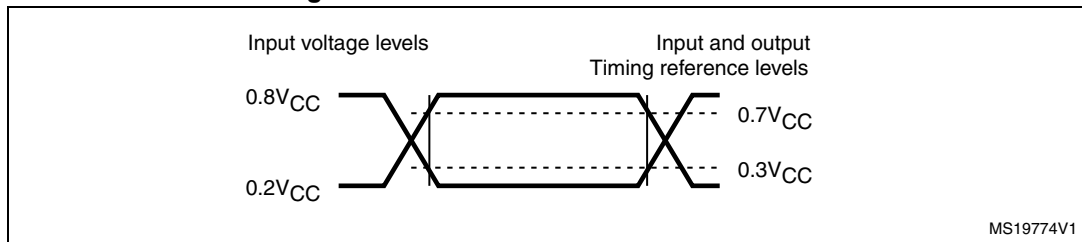


Table 13. Cycling performance

Symbol	Parameter	Test condition	Max. <sup>(1)</sup>	Unit
N <sub>cycle</sub>	Write cycle endurance <sup>(2)</sup>	T <sub>A</sub> ≤ 25 °C, V <sub>CC</sub> (min) < V <sub>CC</sub> < V <sub>CC</sub> (max)	4,000,000	Write cycle <sup>(3)</sup>
		T <sub>A</sub> = 85 °C, V <sub>CC</sub> (min) < V <sub>CC</sub> < V <sub>CC</sub> (max)	1,200,000	

1. Cycling performance for products identified by process letter K or T (previous products were specified with 1 million cycles at 25 °C & 300 K cycles at 85 °C)
2. The Write cycle endurance is defined by characterization and qualification. For devices embedding the ECC functionality (see [Chapter 5.1.5](#)), the write cycle endurance is defined for group of four bytes located at addresses [4\*N, 4\*N+1, 4\*N+2, 4\*N+3] where N is an integer.
3. A Write cycle is executed when either a Page Write, a Byte write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to [Section 5.1.5: ECC \(Error Correction Code\) and Write cycling](#)

Table 14. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention <sup>(1)</sup>	T <sub>A</sub> = 55 °C	200 <sup>(2)</sup>	Year

1. The data retention behavior is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.
2. For products identified by process letter K or T (previous products were specified with a data retention of 40 years at 55°C).