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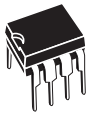
M24C64-DF
M24C64-W M24C64-R M24C64-F

64 Kbit serial I²C bus EEPROM

Features

- Compatible with all I²C bus modes:
  - 1 MHz Fast-mode Plus
  - 400 kHz Fast mode
  - 100 kHz Standard mode
- Memory array:
  - 64 Kb (8 Kbytes) of EEPROM
  - Page size: 32 bytes
  - Additional Write lockable Page (M24C64-DF)
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Single supply voltage:
  - M24C64-W: 2.5 V to 5.5 V
  - M24C64-R: 1.8 V to 5.5 V
  - M24C64-xF: 1.7 V
- Random and Sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - RoHS-compliant and halogen-free (ECOPACK2®)
  - PDIP8 package: RoHS-compliant (ECOPACK1®)



PDIP8 (BN)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)

WLCSP5 (CS)

Contents

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1 Description

The M24C64-W operates with a supply voltage range of 2.5 V/5.5 V, the M24C64-R operates with a supply voltage range of 1.8 V/5.5 V and the M24C64-F, M24C64-DF devices operate with a supply voltage range of 1.7 V/5.5 V.

The M24C64-DF offers an additional page, named the Identification Page (32 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in read only mode.

Figure 1. Logic diagram

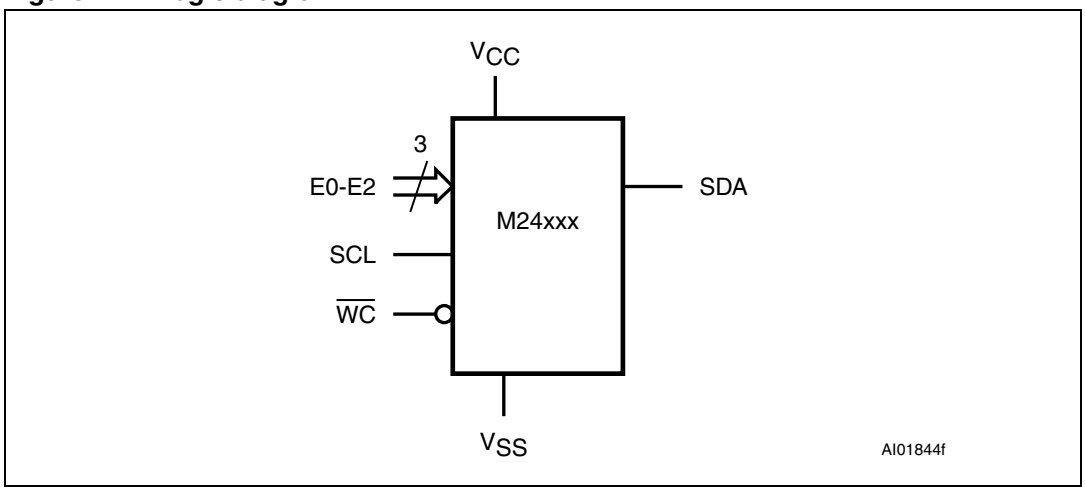
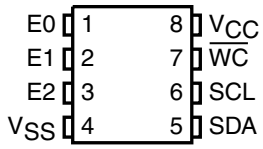


Table 1. Signal names

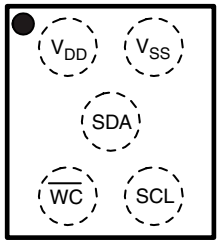
Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. WLCSP connections (top view)



Note: Inputs E2, E1, E0 are internally connected to (001). Please refer to Section 2.3 for further explanations.

Caution: As EEPROM cells loose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

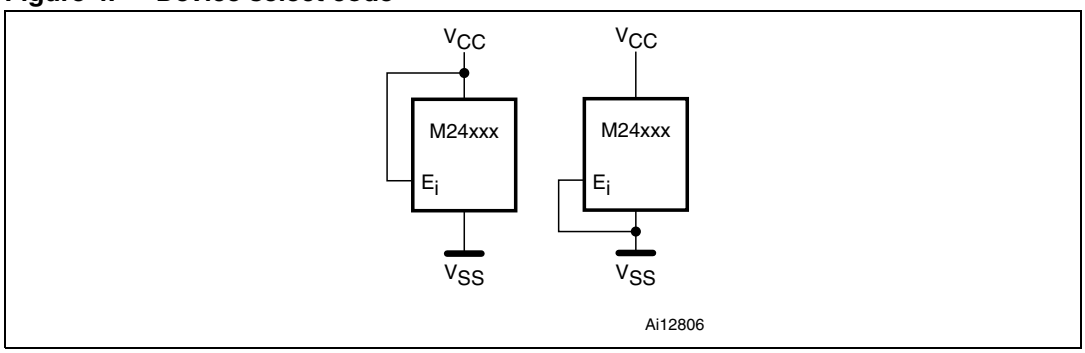
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 4*. When not connected (left floating), these inputs are read as low (0). For the WLCSP package, the (E2,E1,E0) inputs are internally connected to (0,0,1).

Figure 4. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven high, device select and Address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 7*, *Table 8* and *Table 9*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 7*, *Table 8* and *Table 9*. The rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8* and *Table 9*). Until V_{CC} passes over the POR threshold, the device is reset and in Standby Power mode.

In a similar way, during power-down (continuous decay of V_{CC}), as soon as V_{CC} drops below the POR threshold voltage, the device is reset and stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

Figure 5. I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

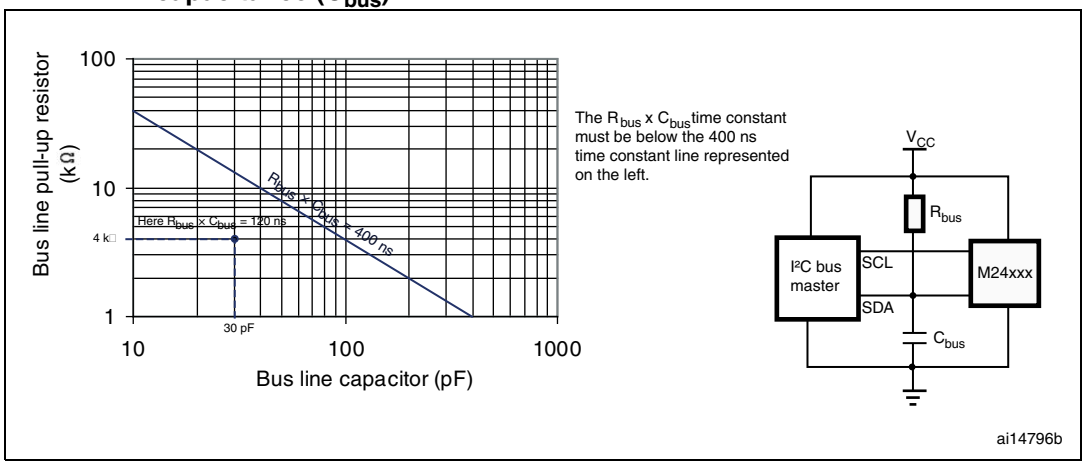


Figure 6. I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

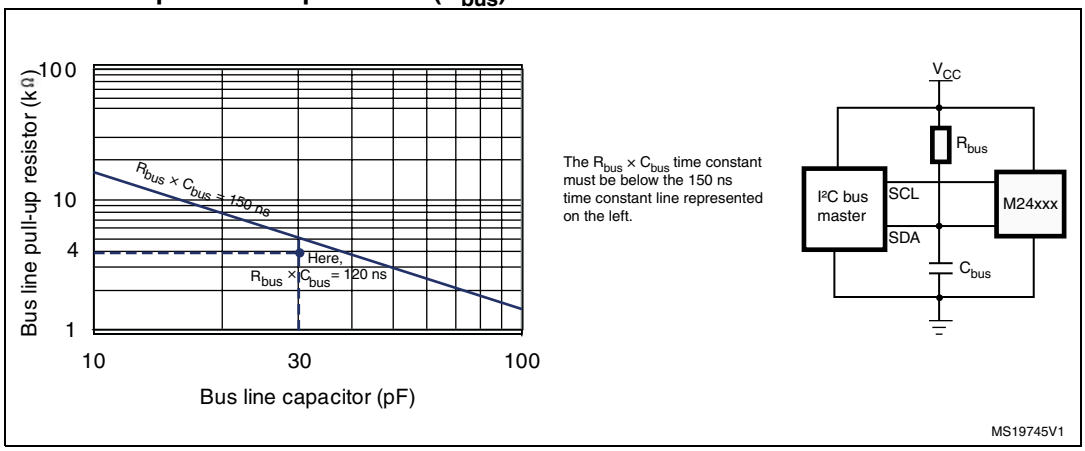


Figure 7. I^2C bus protocol

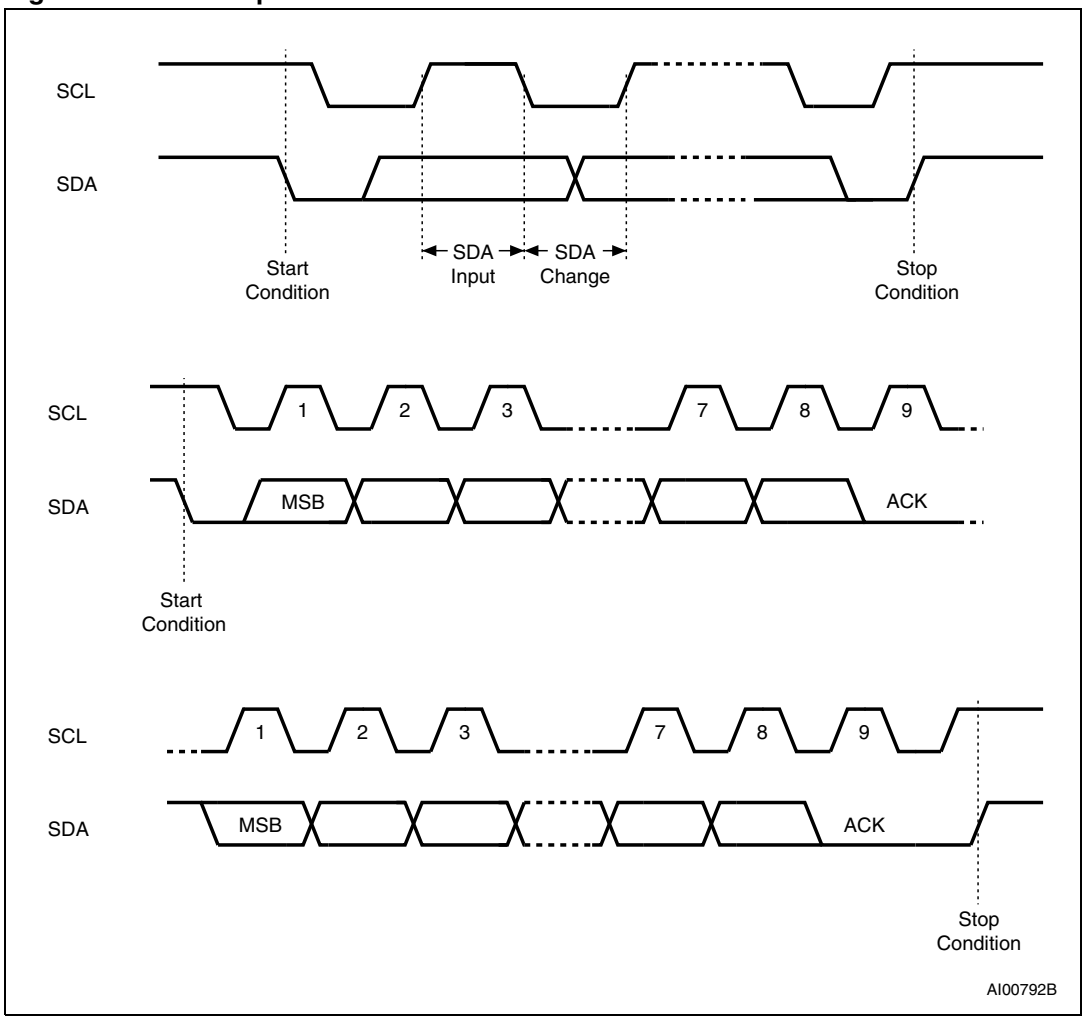


Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)(3)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E2, E1 and E0 are compared against the respective external pins on the memory device.
3. For the WLCSP package, the (E2,E1,E0) inputs are internally connected to (0,0,1).

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

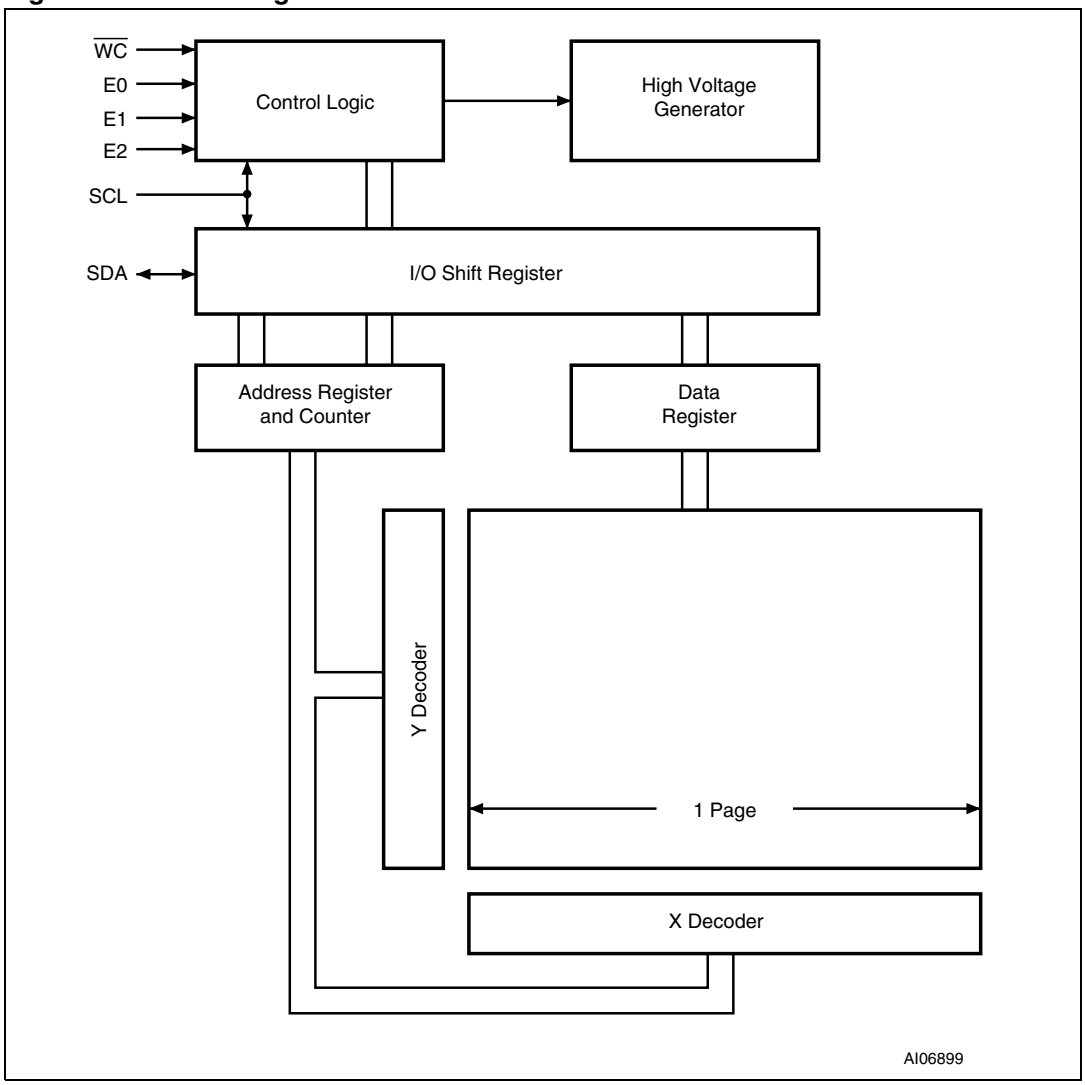
Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Memory organization

The memory is organized as shown in *Figure 8*.

Figure 8. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 7*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

4.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.4 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit device type identifier is 1010b. Up to eight memory devices can be connected on a single I^2C bus[a]. Each one is given a unique 3-bit code on the Chip Enable (E2, E1, E0) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E2, E1, E0) inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

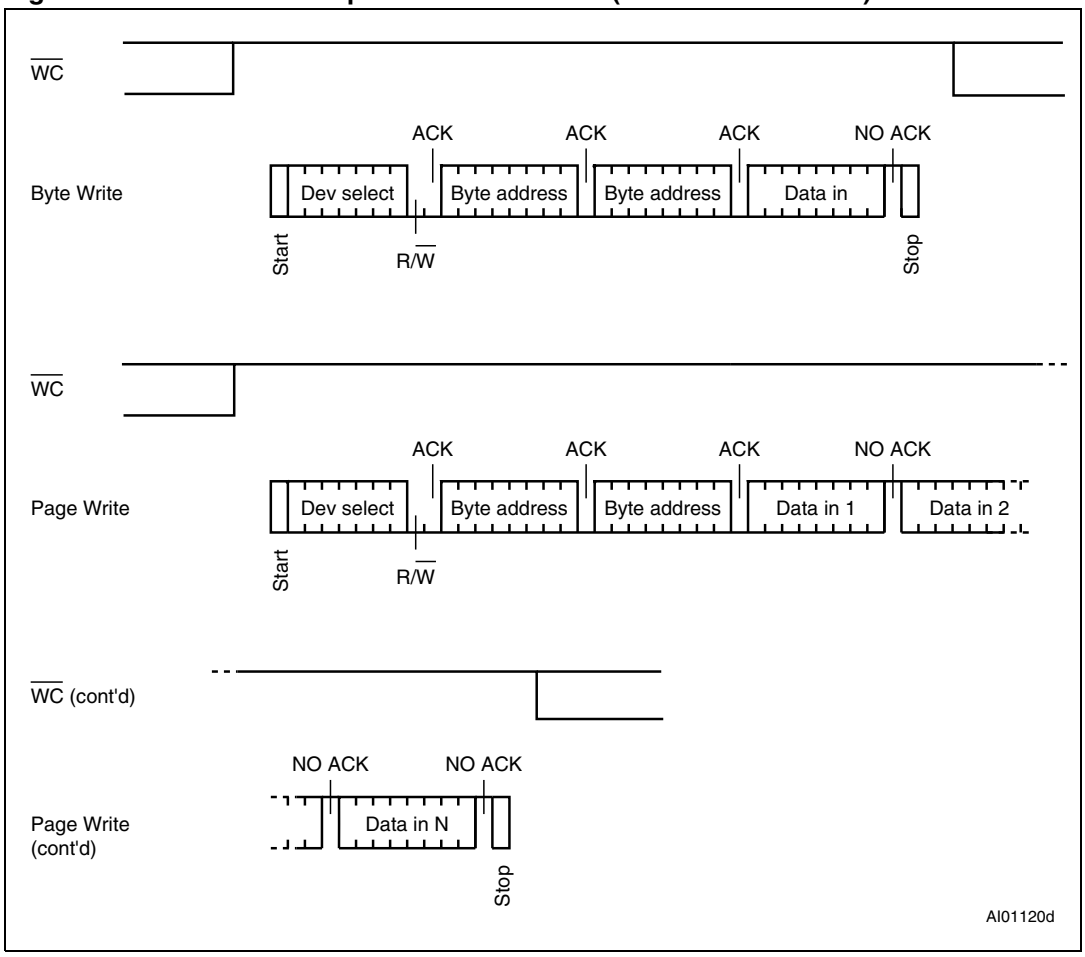
Table 5. Operating modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$[1]	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	Start, device select, $\overline{\text{RW}}$ = 0, Address
	1	X		reStart, device select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤ 32	Start, device select, $\overline{\text{RW}}$ = 0

1. X = V_{IH} or V_{IL}.

a. Only one M24C64 in WLCSP package can be connected on the I²C bus (see *Figure 4*).

Figure 9. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



4.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) reset to 0. The device acknowledges this, as shown in *Figure 10*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data Byte.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 3*) is sent first, followed by the Least Significant Byte (*Table 4*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in *Figure 9*.

4.7 Byte Write

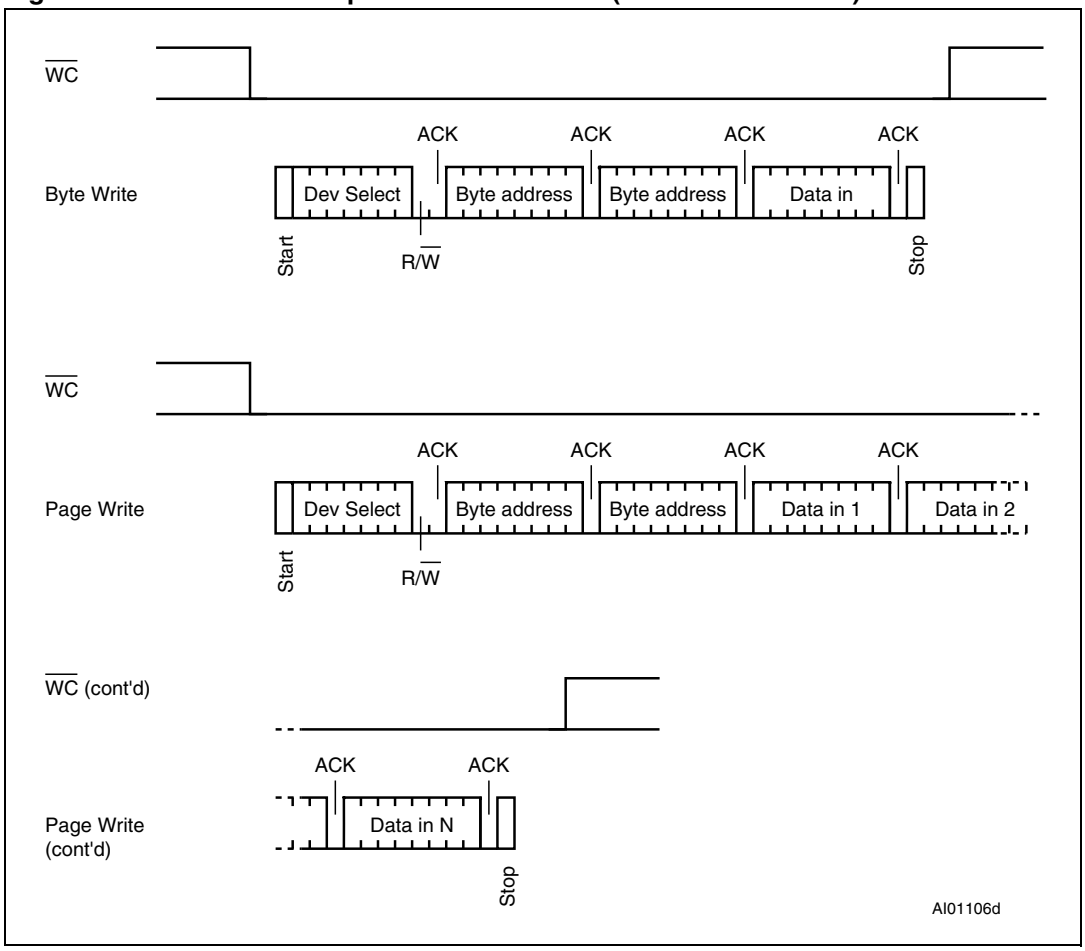
After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{\text{WC}}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 10*.

4.8 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b12-b5) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{\text{WC}}$) is low. If Write Control ($\overline{\text{WC}}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (inside the page) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 10. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



4.9 Write Identification Page (M24C64-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page is written by issuing an Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/A5 are don't care except for address bit A10 which must be ‘0’.

LSB address bits A4/A0 define the byte address inside the Identification Page.

If the Identification Page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

4.10 Lock Identification Page (M24C64-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification Page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

If the Identification Page is locked, the data bytes transferred during the Lock Identification Page instruction are not acknowledged (NoAck).

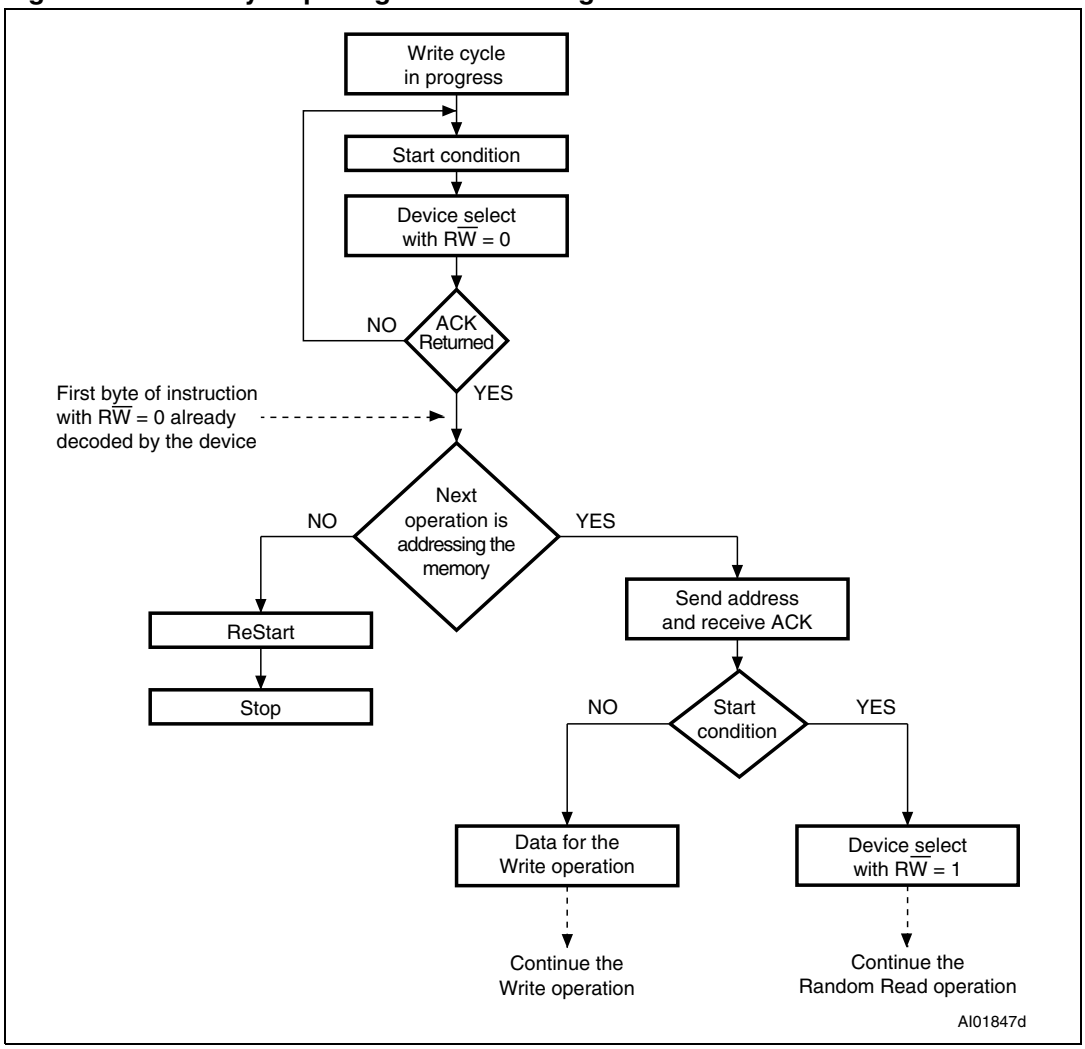
4.11 ECC (Error Correction Code) and Write cycling

The M24C64 devices identified with the process letter A or K offer an ECC (Error Correction Code) logic which compares each 4-byte word with its associated 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

The M24C64 devices are qualified as 1 million (1,000,000) Write cycles, using a cycling routine that writes to the device by multiples of 4-byte words.

Figure 11. Write cycle polling flowchart using ACK



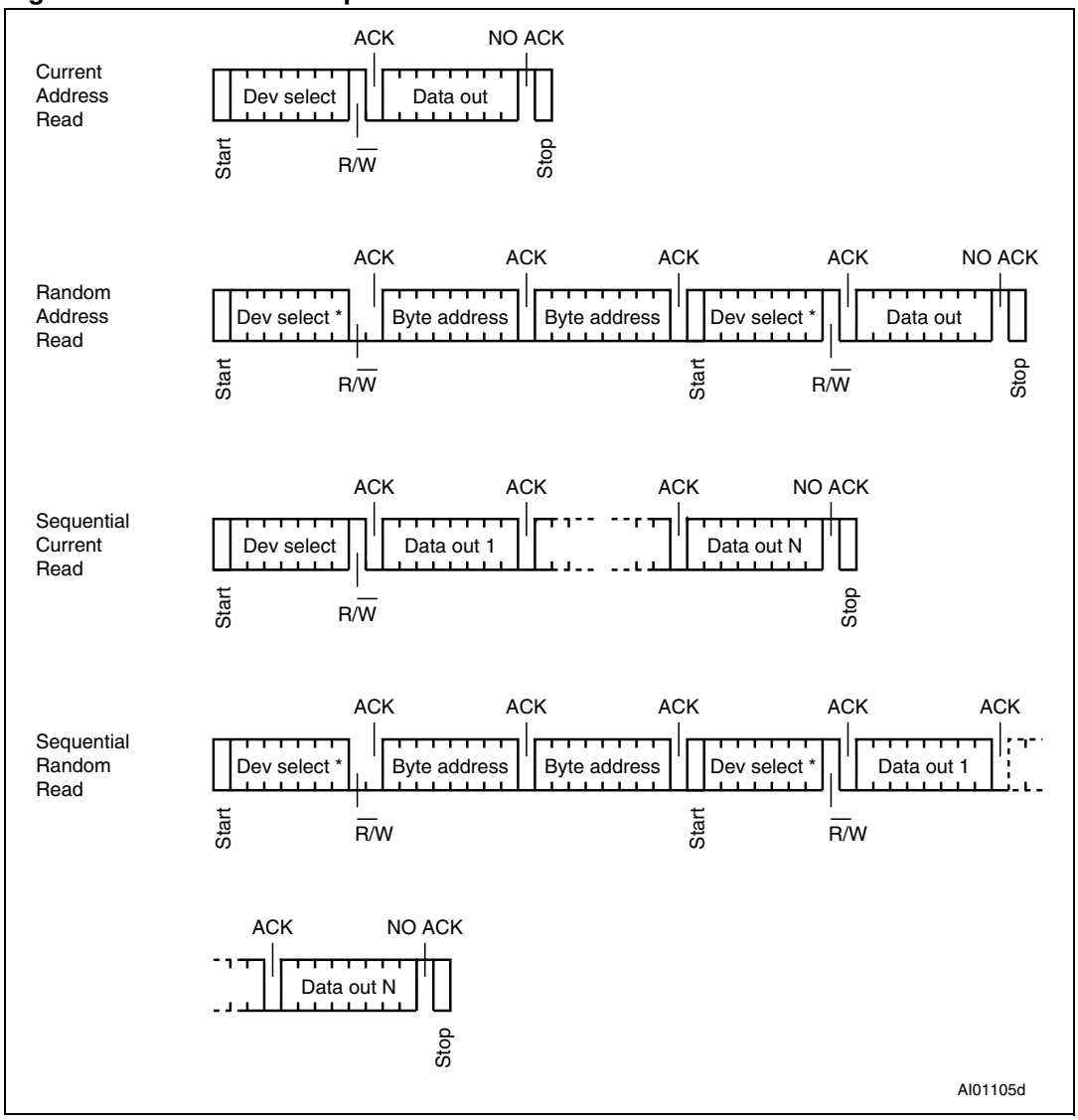
4.12 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 17*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 11*, is:

1. Initial condition: a Write cycle is in progress.
2. Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
3. Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 12. Read mode sequences



1. The seven most significant bits of the device select code of a Random Read (in the 1st and 4th bytes) must be identical.

4.13 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

4.14 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 12*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/$\overline{Write}$ bit (R$\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

4.15 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/$\overline{Write}$ bit (R$\overline{W}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 12*, *without* acknowledging the Byte.

4.16 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 12*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

4.17 Read Identification Page (M24C64-D)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary, otherwise unexpected data is read (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

4.18 Read the lock status (M24C64-D)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

4.19 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9^{th} bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

5 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

6 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
	PDIP-specific lead temperature during soldering		260(2)	°C
V_{IO}	Input or output range	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(3)	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on pin pairs, according to the AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100pF, R1=1500Ω, R2=500Ω)

7 DC and AC parameters

Table 7. Operating conditions (M24xxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C
f_C	Operating clock frequency	-	1	MHz

Table 8. Operating conditions (M24xxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 9. Operating conditions (M24xxx-F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	400(1)	kHz

1. f_{Cmax} is 1 MHz under certain conditions, see *Table 16*, note 1.

Table 10. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time		50	ns
	Input voltage levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 13. AC test measurement I/O waveform

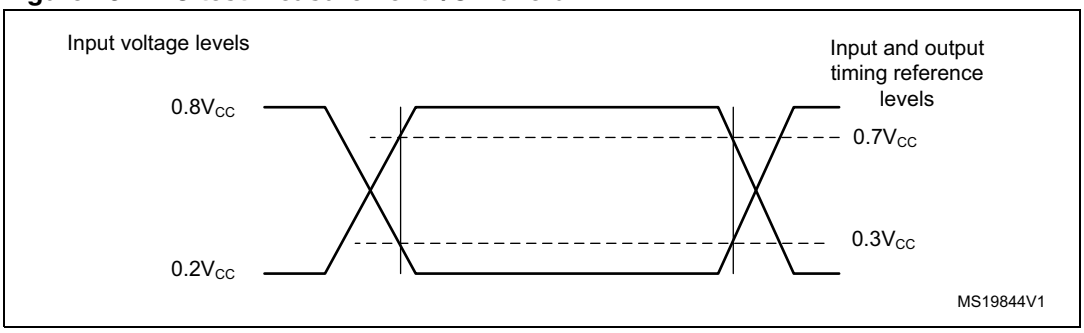


Table 11. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L(2)	Input impedance (E2, E1, E0, WC)	$V_{IN} < 0.3V_{CC}$	30		kΩ
Z_H(2)	Input impedance (E2, E1, E0, WC)	$V_{IN} > 0.7V_{CC}$	500		kΩ

1. Characterized value, not tested in production.
2. E2,E1,E0: Input impedance when the memory is selected (after a Start condition).

Table 12. Memory cell characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
N_{cycle}	Endurance	TA = 25°C, 1.8 V < V_{cc} < 5.5 V	1,000,000	-	Write cycle

Note: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please refer to AN2014.