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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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M24C64S-FCU

64-Kbit serial I²C bus EEPROM 4 balls CSP

Datasheet - production data

WLCSP (CU)

Features

- Compatible with the 400 kHz I²C protocol
- High speed 1MHz transfer rate
- Memory array:
  - 64 Kbit (8 Kbyte) of EEPROM
  - Page size: 32 byte
- Supply voltage range:
  - 1.7 V to 5.5 V
- Operating temperature range
  - V_{CC} = 1.7 V to 5.5V over -40°C / +85°C
  - V_{CC} = 1.6 V to 5.5V over 0°C / +85°C
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential Read modes
- Software Write protect
  - Upper quarter memory array
  - Upper half memory array
  - Upper 3/4 memory array
  - Whole memory array
- ESD protection
  - Human Body Model: 4 kV
- More than 4 million Write cycles
- More than 200-years data retention
- Package
  - WLCSP, RoHS and Halogen free compliant (ECOPACK2®)

Contents

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1 Description

The M24C64S-FCU is a 64-Kbit I2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 8 K × 8 bits.

The M24C64S-FCU can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C/+85 °C and with an extended supply voltage from 1.6 V to 5.5 V, over a reduced ambient temperature range.

The M24C64S-FCU is delivered in a 4-ball WLCSP package.

Figure 1. Logic diagram

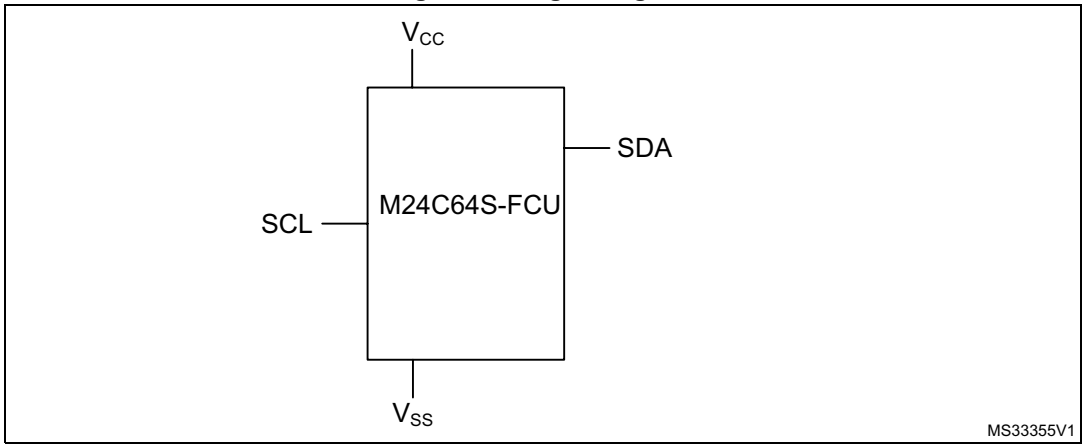
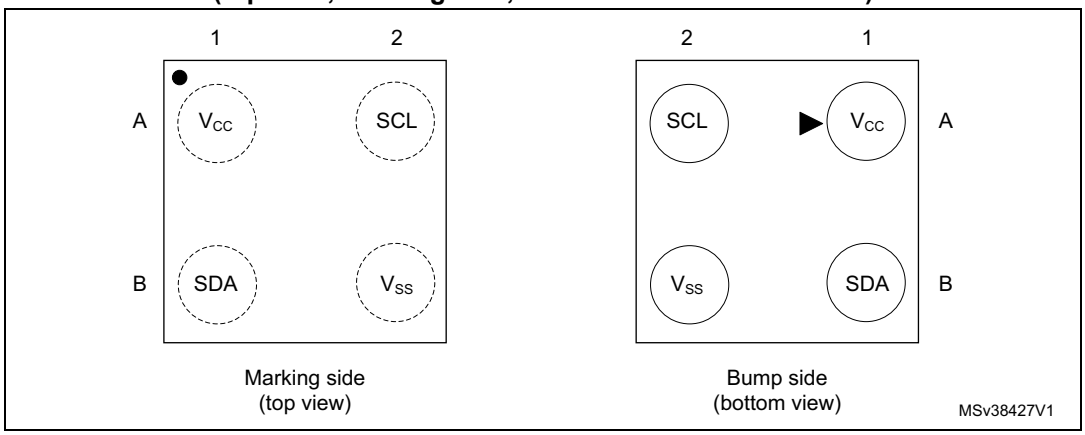


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial Data	I/O
SCL	Serial Clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 4-bump WLCSP connections
(top view, marking side, with balls on the underside)



2 Signal description

2.1 Serial Clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 9* indicates how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)*.

2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

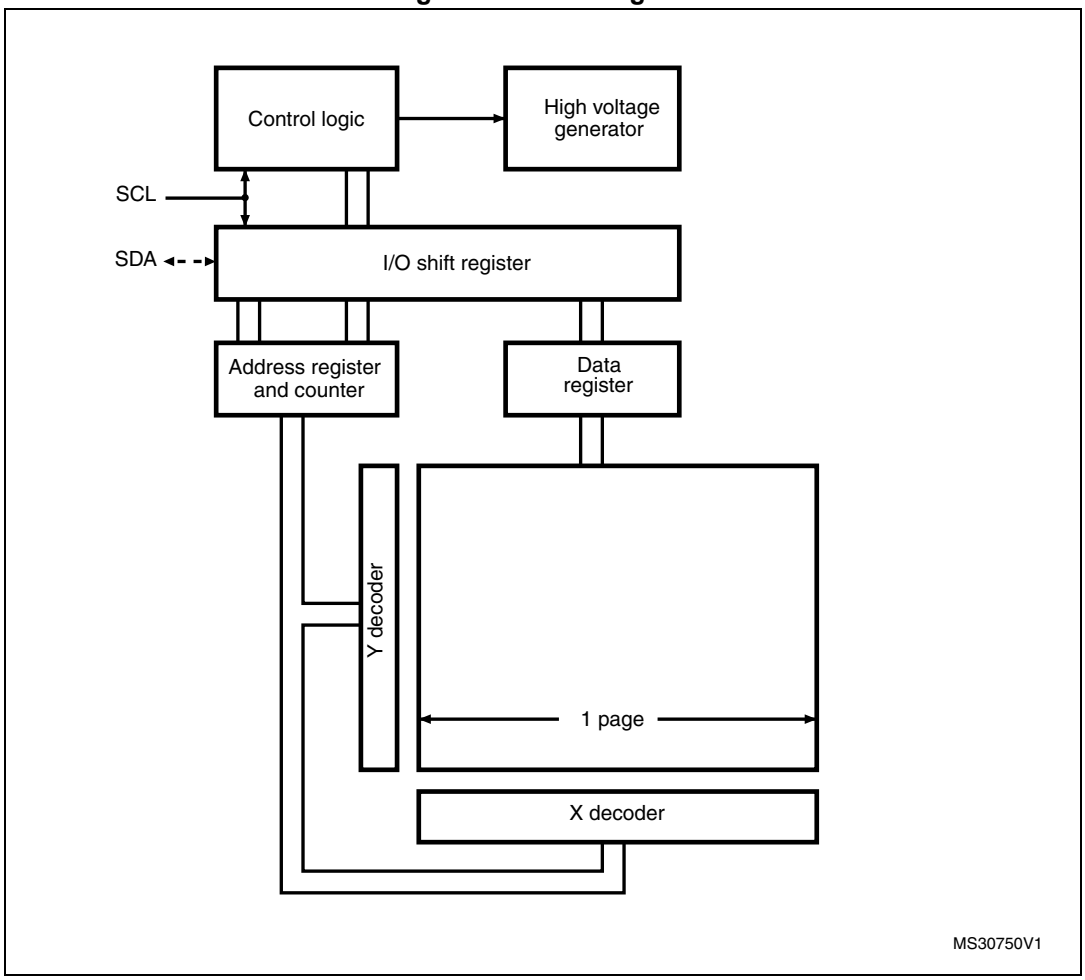
2.4.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

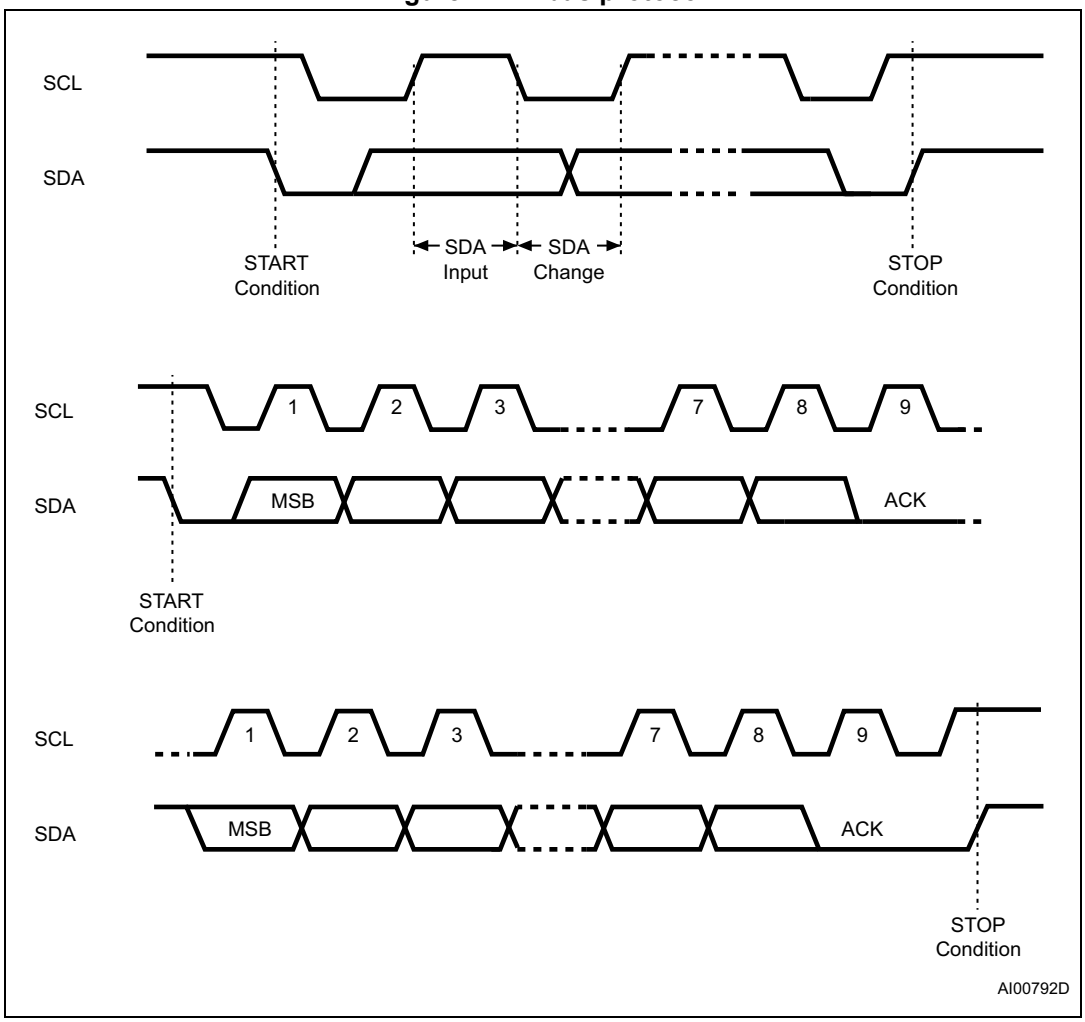
Figure 3. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 4*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 4. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

Device type identifier(1)				Chip Enable address			$\overline{RW}$
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	0	0	1	$\overline{RW}$

1. The most significant bit, b7, is sent first.

The 8th bit is the Read/$\overline{Write}$ bit ($\overline{RW}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time.

If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode (therefore will not acknowledge the device select code).

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 5*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 4. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

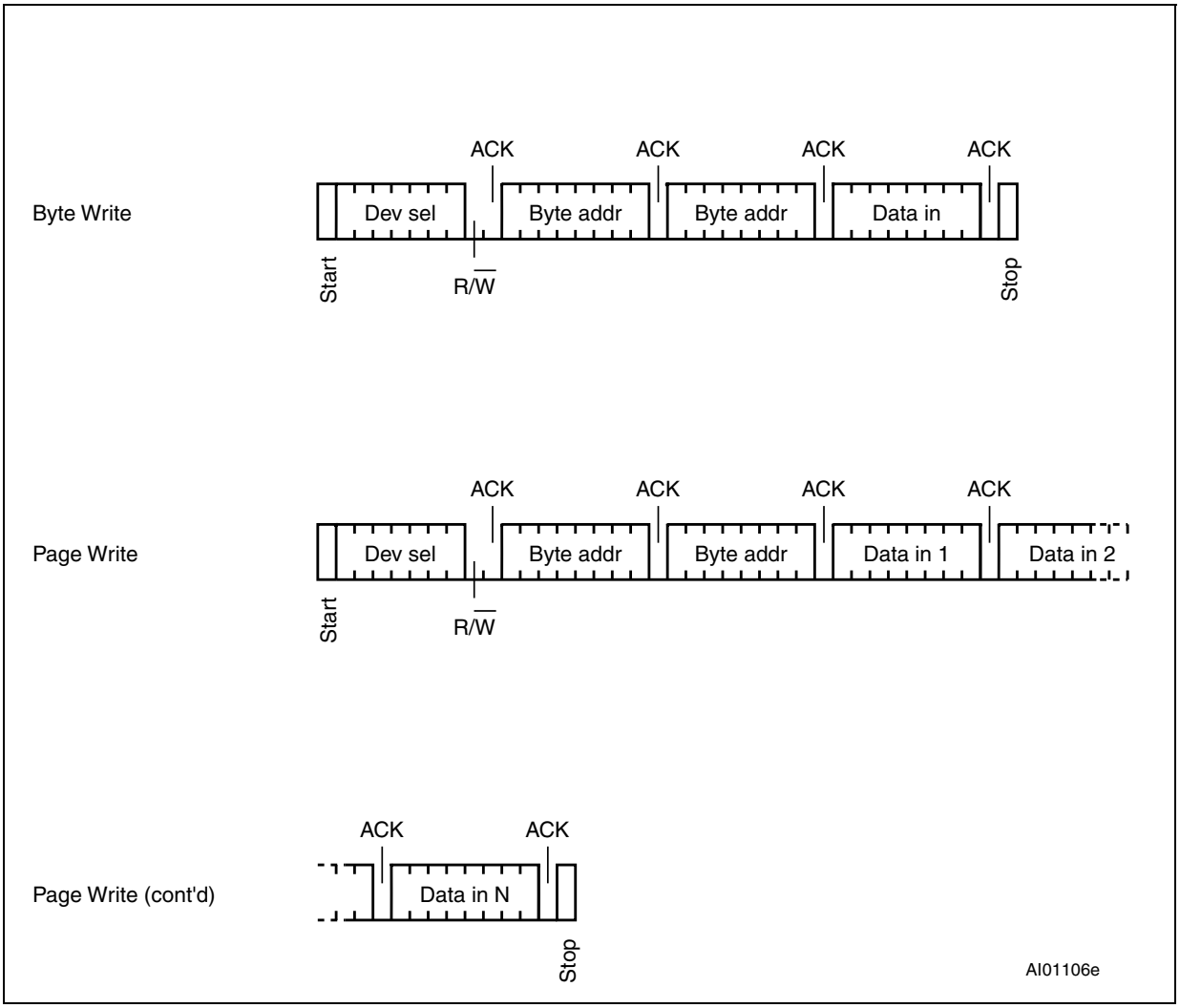
After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, the device replies with NoAck, and the location is not modified, as shown in *Figure 6*. If, instead, the addressed location is not Write-protected, the device replies with Ack, as shown in *Figure 5*. The bus master shall terminate the transfer by generating a Stop condition.

Figure 5. Write mode sequence (data write enabled)



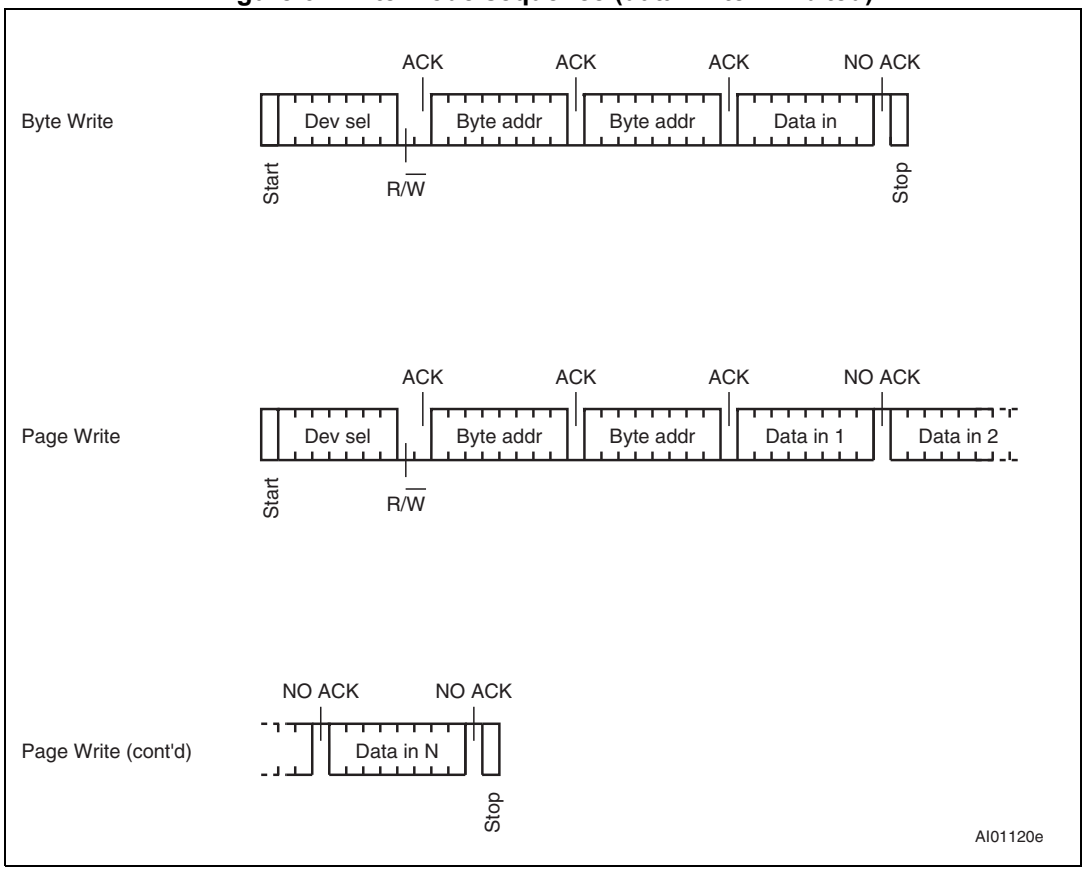
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if the page is not write-protected, as shown in *Figure 5*. If the page is write-protected, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 6*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 6. Write mode sequence (data write inhibited)



5.1.3 Write protection

By writing specific values in a register (*Table 5*) located at address 1xxx.xxxx.xxxx.xxxxb, the memory array can be write-protected by blocks, which size can be defined as:

- the upper quarter memory array
- the upper half memory array
- the upper 3/4 memory array
- the whole memory array

Table 5. Write Protect register (Address = 1xxx.xxxx.xxxx.xxxxb)

	b7	b6	b5	b4	b3	b2	b1	b0
Write	x	x	x	x	Write protect activation	Size of write protected block	Size of write protected block	Write protect lock
Read	0	0	0	0				

Note: Location 1xxx.xxxx.xxxx.xxxxb is outside of the addressing field of the EEPROM memory (16 Kbytes are addressed within the 00xx.xxxx.xxxx.xxxx range)

- Bit b3 enables or disables the Write protection
  - b3=0: the whole memory can be written (no Write protection)
  - b3=1: the concerned block is write-protected
- Bits b2 and b1 define the size of the memory block to be protected against write instructions:
  - b2,b1=0,0: the upper quarter of memory is write-protected
  - b2,b1=0,1: the upper half memory is write-protected
  - b2,b1=1,0: the upper 3/4 of memory are write-protected
  - b2,b1=1,1: the whole memory is write-protected
- bit b0 locks the write protect status
  - b0=0: bits b3,b2,b1,b0 can be modified
  - b0=1: bits b3,b2,b1,b0 cannot be modified and therefore the memory write protection is frozen.
- b7, b6, b5, b4 bits are Don't Care bits.

Writing the Write Protect register

Writing in the Write protect register is performed with a Byte Write instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7,b6,b5,b4 of the data byte are not significant (Don't Care).

Writing more than one byte will discard the write cycle (Write protect register content will not be changed).

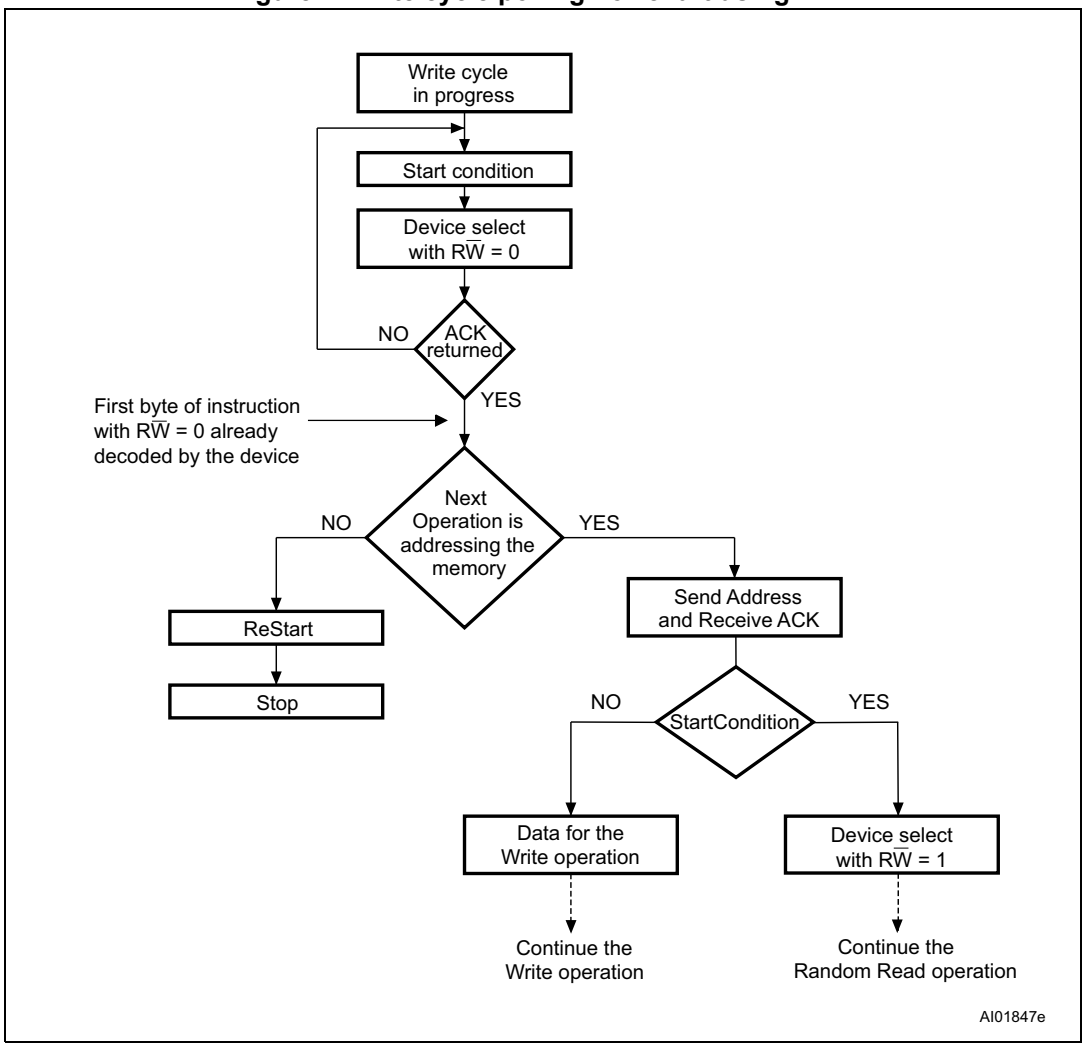
5.1.4 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 7*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 7. Write cycle polling flowchart using ACK



1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

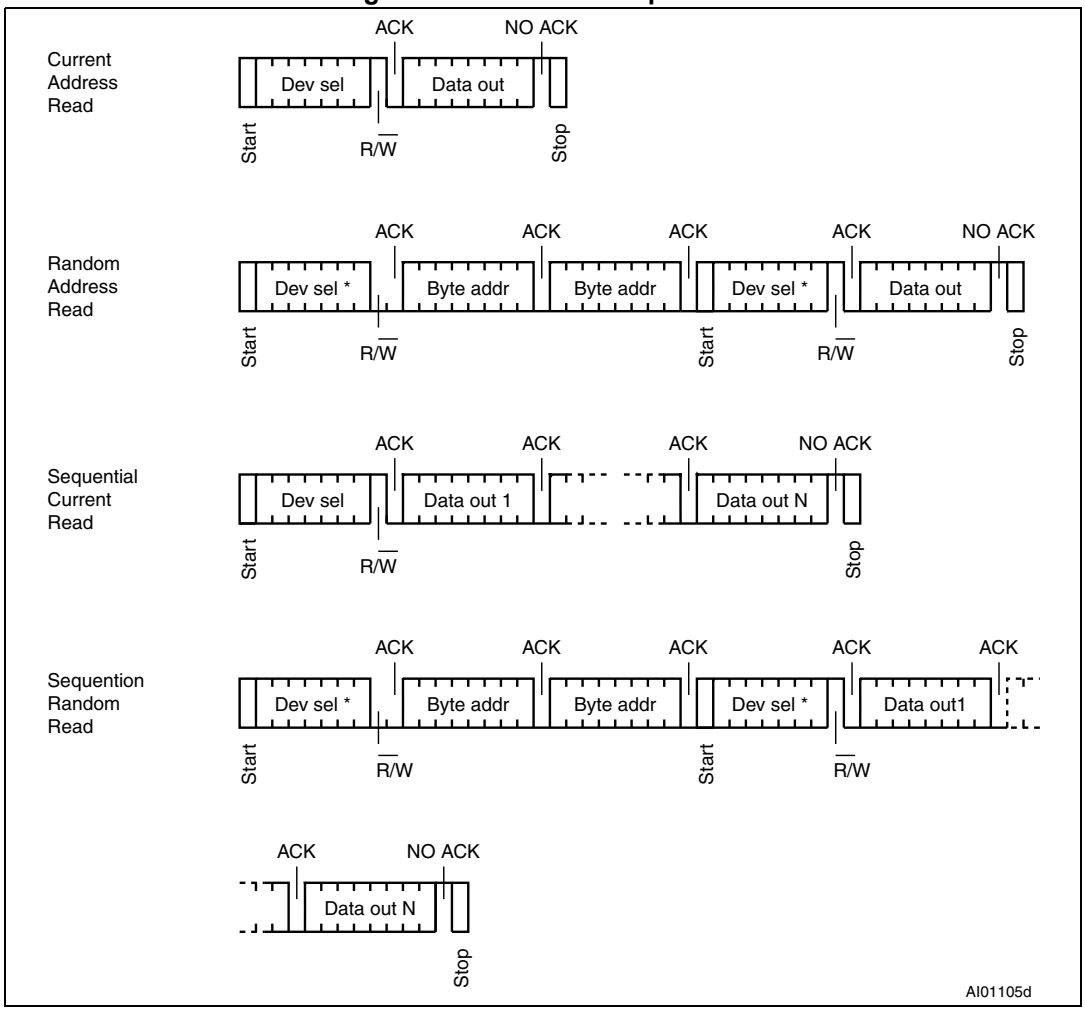
5.2 Read operations

Read operations are performed independently of the Write protection state.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 8. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 8*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 8*, *without* acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 8*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.2.4 Read the Write Protect register

Reading the Write Protect register is performed with a Random Read instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7, b6, b5, b4 of the Write Protect register content are read as 0, 0, 0, 0. The signification of the Protect Register lower bits b3, b2, b1, b0 are defined in *Section 5.1.3: Write protection*.

Reading more than one byte will loop on reading the Write Protect Register value.

The Write Protect register cannot be read while a write cycle (t_w) is ongoing.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh) and the Write Protect register set to 0 (00h).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6	V
V_{CC}	Supply voltage	–0.50	6	V
V_{ESD}	Electrostatic pulse (Human Body model)	-	4000	V

1. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Test conditions

Symbol	Parameter	Min.	Unit
Data retention(1)	TA = 55 °C	200	year
Cycling	TA = 25 °C	4 million	cycle

1. The data retention behavior is checked in production. The 200-year limit is defined from characterization and qualification results.

Table 8. Operating conditions

Symbol	Parameter	Min.		Max.	Unit
V_{CC}	Supply voltage	1.60	1.70	5.5	V
T_A	Ambient operating temperature: READ	–40	–40	85	°C
	Ambient operating temperature: WRITE	0	–40		
f_C	Operating clock frequency, V_{CC} = 1.6 V	-		400	kHz
	Operating clock frequency, V_{CC} = 1.7 V	-		1000	

Table 9. DC characteristics

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} < 1.8 V, f_C = 400 kHz	-	0.8	mA
		V_{CC} >= 1.8 V, f_C = 400 kHz	-	2	mA
		V_{CC} >= 1.8 V, f_C = 1 MHz(1)	-	2.5	mA
I_{CC0}	Supply current (Write)(2)	During t_W	-	2	mA
I_{CC1}	Standby supply current	Device not selected (3), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8 V	-	1	µA
		Device not selected (3), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected (3), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	3	µA
V_{IL}	Input low voltage (SCL, SDA)	-	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.75 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} < 1.8 V	-	0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V	-	0.4	V
		I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. Only for devices operating at f_{cMax} = 1 MHz (See *Table 8*)
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 10. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. value for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. The min value for t_{CLQX} (Data out hold time) offers a safe timing to bridge the undefined region of the falling edge SCL.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is less than 400 ns.

Table 11. 1 MHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	700(1)	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	(2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	(2)	ns
t_{QL1QL2} (3)	t_F	SDA (out) fall time	20(4)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (5)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (6)	t_{AA}	Clock low to next data valid (access time)	-	650	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (3)	-	Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. 600ns when -20°C ≤ t°≤ +85°C. Characterized only, not tested in production.
2. There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.
3. Characterized only, not tested in production.
4. With CL = 10 pF.
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 10*.