Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

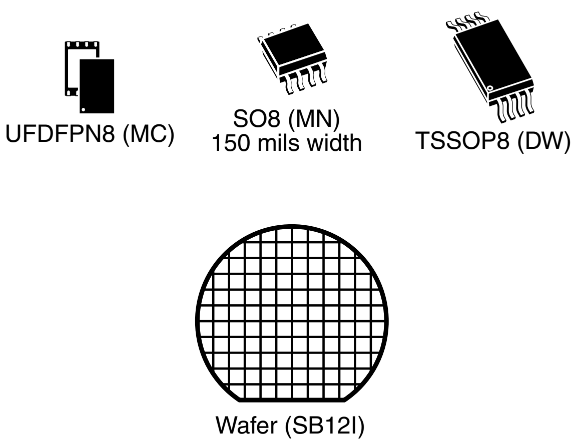
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

M24LR04E-R

Dynamic NFC/RFID tag IC with 4-Kbit EEPROM, energy harvesting, I^2C bus and ISO 15693 RF interface

Datasheet - production data



Features

- Belonging to ST25 family, which includes all NFC/RF ID tag and reader products from ST

I^2C interface

- Two-wires I^2C serial interface supports 400 kHz protocol
- Single supply voltage:
  - 1.8 V to 5.5 V
- Byte and Page Write (up to 4 bytes)
- Random and Sequential read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- I^2C timeout

Contactless interface

- ISO 15693 and ISO 18000-3 mode 1 compatible
- 13.56 MHz ± 7 kHz carrier frequency
- To tag: 10% or 100% ASK modulation using 1 out of 4 (26 Kbit/s) or 1 out of 256 (1.6 Kbit/s) pulse position coding
- From tag: load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 kbit/s) or high (26 kbit/s) data rate mode. Supports the 53 kbit/s data rate with Fast commands
- Internal tuning capacitance: 27.5pF
- 64-bit unique identifier (UID)
- Read Block & Write (32-bit blocks)

Digital output pin

- User configurable pin: RF write in progress or RF busy mode

Energy harvesting

- Analog pin for energy harvesting
- 4 sink current configurable ranges

Temperature range

- From –40 to 85 °C

Memory

- 4-Kbit EEPROM organized into:
  - 512 bytes in I^2C mode
  - 128 blocks of 32 bits in RF mode
- Write time
  - I^2C: 5 ms (max.)
  - RF: 5.75 ms including the internal Verify time
- Write cycling endurance:
  - 1 million write cycles at 25 °C
  - 150k write cycles at 85 °C
- More than 40-year data retention
- Multiple password protection in RF mode
- Single password protection in I^2C mode
- Package
  - SO8 (ECOPACK2®)
  - TSSOP8 (ECOPACK2®)
  - UFDFPN8 (ECOPACK2®)

Contents

List of tables

List of figures

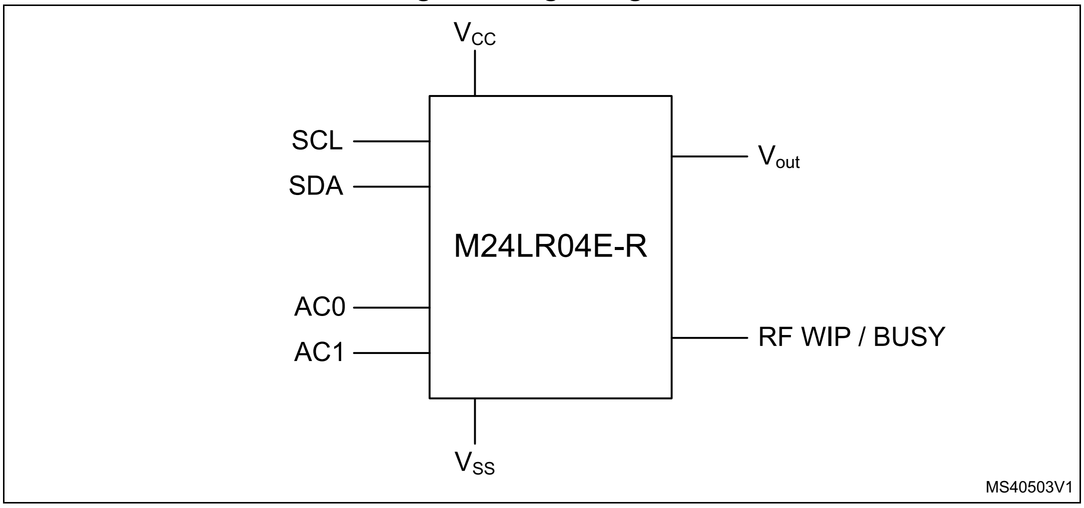
1 Description

The M24LR04E-R device is a Dynamic NFC/RFID tag IC with a dual-interface, electrically erasable programmable memory (EEPROM). The logic scheme is shown in *Figure 1*.

It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR04E-R is organized as 512 × 8 bits in the I^2C mode and as 128 × 32 bits in RF mode.

The M24LR04E-R also features an energy harvesting analog output, as well as a user-configurable digital output pin toggling during either RF write in progress or RF busy mode.

Figure 1. Logic diagram



I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) (as described in *Table 2*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR04E-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). When connected to an antenna, the operating power is derived from the RF energy and no external power supply is required. The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the M24LR04E-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR04E-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s high data rate mode. The

M24LR04E-R supports the 53 Kbit/s fast mode in high data rate mode using one subcarrier frequency at 423 kHz.

The M24LR04E-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

The M24LR04E-R provides an Energy harvesting mode on the analog output pin Vout. When the Energy harvesting mode is activated, the M24LR04E-R can output the excess energy coming from the RF field on the Vout analog pin. In case the RF field strength is insufficient or when Energy harvesting mode is disabled, the analog output pin Vout goes into high-Z state and Energy harvesting mode is automatically stopped.

The M24LR04E-R features a user configurable digital out pin RF WIP/BUSY that can be used to drive a micro controller interrupt input pin (available only when the M24LR04E-R is correctly powered on the Vcc pin).

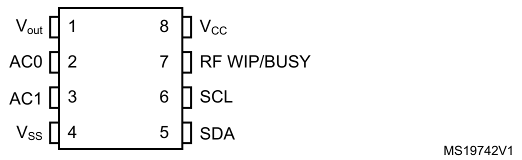
When configured in the RF write in progress mode (RF WIP mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF internal write operation. When configured in the RF busy mode (RF BUSY mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF command progress.

The RF WIP/BUSY pin is an open drain output and must be connected to a pull-up resistor.

Table 1. Signal names

Signal name	Function	Direction
Vout	Energy harvesting Output	Analog output
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O
V_{CC}	Supply voltage	-
RF WIP/BUSY	Digital signal	Digital output
V_{SS}	Ground	-

Figure 2. 8-pin package connections



1. See *Section 31* for package dimensions, and how to identify pin-1.

2 Signal descriptions

2.1 Serial clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 3* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

2.2 Serial data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 3* indicates how the value of the pull-up resistor can be calculated).

2.3 RF Write in progress / RF Busy (RF WIP/BUSY)

This configurable output signal is used either to indicate that the M24LR04E-R is executing an internal write cycle from the RF channel or that an RF command is in progress. RF WIP and signals are available only when the M24LR04E-R is powered by the Vcc pin. It is an open drain output and a pull up resistor must be connected from RF WIP/BUSY to V_{CC}.

2.4 Energy harvesting analog output (Vout)

This analog output pin is used to deliver the analog voltage Vout available when the Energy harvesting mode is enabled and the RF field strength is sufficient. When the Energy harvesting mode is disabled or the RF field strength is not sufficient, the energy harvesting analog voltage output Vout is in High-Z state.

2.5 Antenna coil (AC0, AC1)

These inputs are used to connect the device to an external coil exclusively. It is advised not to connect any other DC or AC path to AC0 or AC1.

When correctly tuned, the coil is used to power and access the device using the ISO 15693 and ISO 18000-3 mode 1 protocols.

2.5.1 Device reset in RF mode

To ensure a proper reset of the RF circuitry, the RF field must be turned off (100% modulation) for a minimum t_{RF_OFF} period of time.

2.6 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage and Vout analog output voltage.

2.7 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the M24LR04E-R, while preventing the internal power supply (rectified RF waveforms) to output a DC voltage on the V_{CC} pin.

2.7.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 118*). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal I²C write cycle (t_W).

2.7.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

2.7.3 Device reset in I²C mode

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any I²C instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 118*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby power mode. However, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

2.7.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

Figure 3. I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

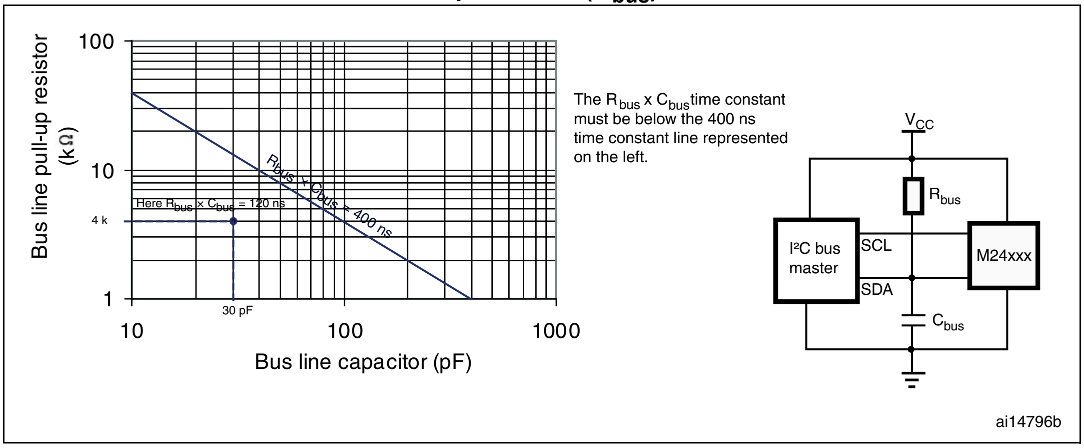


Figure 4. I^2C bus protocol

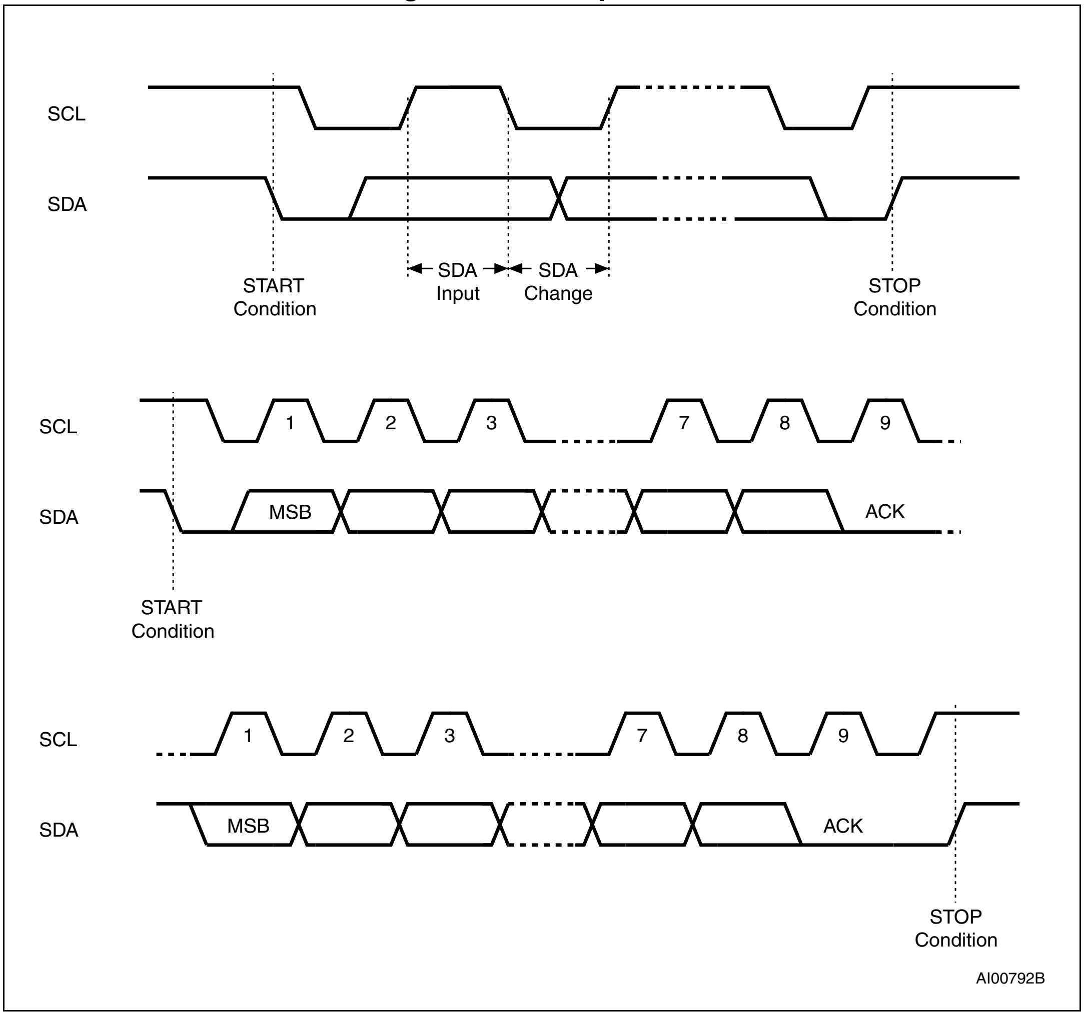


Table 2. Device select code

-	Device type identifier[1]				Chip Enable address			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2[2]	1	1	R$\overline{W}$

1. The most significant bit, b7, is sent first.
2. E2 is not connected to any external pin. It is however used to address the M24LR04E-R as described in *Section 3* and *Section 4*.

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 User memory organization

The M24LR04E-R is divided into four sectors of 32 blocks of 32 bits, as shown in *Table 5*.

Figure 6 shows the memory sector organization. Each sector can be individually read- and/or write-protected using a specific password command. Read and write operations are possible if the addressed data are not in a protected sector.

The M24LR04E-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user in RF device operation and its value is written by ST on the production line.

The M24LR04E-R includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The M24LR04E-R has four 32-bit blocks that store an I^2C password plus three RF password codes.

Figure 5. Circuit diagram

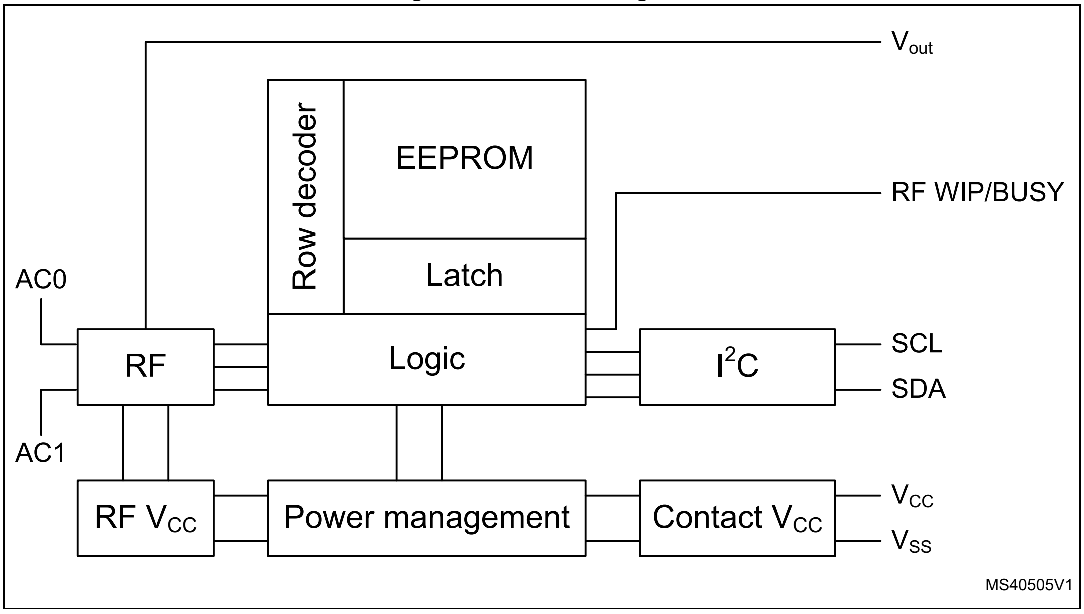


Figure 6. Memory sector organization

Sector	Area	Sector security status
0	1 Kbit EEPROM sector	5 bits
1	1 Kbit EEPROM sector	5 bits
2	1 Kbit EEPROM sector	5 bits
3	1 Kbit EEPROM sector	5 bits
	I²C password	System
	RF password 1	System
	RF password 2	System
	RF password 3	System
	8-bit DSFID	System
	8-bit AFI	System
	64-bit UID	System
	8-bit configuration	System
	16-bit I²C Write Lock_bit	System
	20-bit SSS	System

MS19766V1

Sector details

The M24LR04E-R user memory is divided into four sectors. Each sector contains 1024 bits. The protection scheme is described in *Section 4: System memory area*.

In RF mode, a sector provides 32 blocks of 32 bits. Each read and write access is done by block. Read and write block accesses are controlled by a Sector Security Status byte that defines the access rights to the 32 blocks contained in the sector. If the sector is not protected, a Write command updates the complete 32 bits of the selected block.

In I^2C mode, a sector provides 128 bytes that can be individually accessed in Read and Write modes. When protected by the corresponding I2C_Write_Lock bit, the entire sector is write-protected. To access the user memory, the device select code used for any I^2C command must have the E2 Chip Enable address at 0.

Table 5. Sector details

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	0	0	user	user	user	user
	1	4	user	user	user	user
	2	8	user	user	user	user
	3	12	user	user	user	user
	4	16	user	user	user	user
	5	20	user	user	user	user
	6	24	user	user	user	user
	7	28	user	user	user	user
	8	32	user	user	user	user
	9	36	user	user	user	user
	10	40	user	user	user	user
	11	44	user	user	user	user
	12	48	user	user	user	user
	13	52	user	user	user	user
	14	56	user	user	user	user
	15	60	user	user	user	user
	16	64	user	user	user	user
	17	68	user	user	user	user
	18	72	user	user	user	user
	19	76	user	user	user	user
	20	80	user	user	user	user
	21	84	user	user	user	user
	22	88	user	user	user	user
	23	92	user	user	user	user
	24	96	user	user	user	user
	25	100	user	user	user	user
	26	104	user	user	user	user
	27	108	user	user	user	user
	28	112	user	user	user	user
	29	116	user	user	user	user
	30	120	user	user	user	user
	31	124	user	user	user	user

Table 5. Sector details (continued)

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
1	32	128	user	user	user	user
	33	132	user	user	user	user
	34	136	user	user	user	user
	35	140	user	user	user	user
	36	144	user	user	user	user
	37	148	user	user	user	user
	38	152	user	user	user	user
	39	156	user	user	user	user
	...	...	...	...	...	...
2	...	...	...	...	...	...
3	...	...	...	...	...	...
	127	508	user	user	user	user

4 System memory area

4.1 M24LR04E-R block security in RF mode

The M24LR04E-R provides a special protection mechanism based on passwords. In RF mode, each memory sector of the M24LR04E-R can be individually protected by one out of three available passwords, and each sector can also have Read/Write access conditions set.

Each memory sector of the M24LR04E-R is assigned with a Sector security status byte including a Sector Lock bit, two Password Control bits and two Read/Write protection bits, as shown in *Table 7*.

Table 6 describes the organization of the Sector security status byte, which can be read using the Read Single Block and Read Multiple Block commands with the Option_flag set to 1.

On delivery, the default value of the SSS bytes is set to 00h.

Table 6. Sector security status byte area

I^2C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	0	SSS 3	SSS 2	SSS 1	SSS 0

Table 7. Sector security status byte organization

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	Password control bits		Read / Write protection bits		Sector Lock

When the Sector Lock bit is set to 1, for instance by issuing a Lock-sector command, the two Read/Write protection bits (b_1, b_2) are used to set the Read/Write access of the sector as described in *Table 8*.

Table 8. Read / Write protection bit setting

Sector Lock	b_2, b_1	Sector access when password presented		Sector access when password not presented	
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

The next two bits of the Sector security status byte (b_3, b_4) are the password control bits. The value of these two bits is used to link a password to the sector, as defined in *Table 9*.

Table 9. Password control bits

b_4, b_3	Password
00	The sector is not protected by a password.
01	The sector is protected by password 1.
10	The sector is protected by password 2.
11	The sector is protected by password 3.

The M24LR04E-R password protection is organized around a dedicated set of commands, plus a system area of three password blocks where the password values are stored. This system area is described in *Table 10*.

Table 10. Password system area

Add	
1	Password 1
2	Password 2
3	Password 3

The dedicated commands for protection in RF mode are:

- Write-sector password:

  The Write-sector password command is used to write a 32-bit block into the password system area. This command must be used to update password values. After the write cycle, the new password value is automatically activated. It is possible to modify a password value after issuing a valid Present-sector password command. On delivery, the three default password values are set to 0000 0000h and are activated.
- Lock-sector:

  The Lock-sector command is used to set the sector security status byte of the selected sector. Bits b_4 to b_1 of the sector security status byte are affected by the Lock-sector command. The sector lock bit, b_0, is set to 1 automatically. After issuing a Lock-sector command, the protection settings of the selected sector are activated. The protection of a locked block cannot be changed in RF mode. A Lock-sector command sent to a locked sector returns an error code.

- Present-sector password:

  The Present-sector password command is used to present one of the three passwords to the M24LR04E-R in order to modify the access rights of all the memory sectors linked to that password (*Table 8*) including the password itself. If the presented password is correct, the access rights remain activated until the tag is powered off or until a new Present-sector password command is issued. If the presented password value is not correct, all the access rights of all the memory sectors are deactivated.
- Sector security status byte area access conditions in I2C mode:

  In I^2C mode, read access to the sector security status byte area is always allowed. Write access depends on the correct presentation of the I^2C password (see *Section 5.16.1: I2C present password command description*).

  To access the Sector security status byte area, the device select code used for any I^2C command must have the E2 Chip Enable address at 1.

  An I^2C write access to a sector security status byte re-initializes the RF access condition to the given memory sector.

4.1.1 Example of the M24LR04E-R security protection in RF mode

Table 11 and *Table 12* show the sector security protections before and after a valid Present-sector password command. *Table 11* shows the sector access rights of an M24LR04E-R after power-up. After a valid Present-sector password command with password 1, the memory sector access is changed as shown in *Table 12*.

Table 11. M24LR04E-R sector security protection after power-up

Sector address	Protection			Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: password 1	Read	No Write	xxx	0	1	0	0	1
2	Protection: password 1	Read	Write	xxx	0	1	0	1	1
3	Protection: password 1	No Read	No Write	xxx	0	1	1	0	1
4	Protection: password 1	No Read	No Write	xxx	0	1	1	1	1

Table 12. M24LR04E-R sector security protection after a valid presentation of password 1

Sector address	Protection			Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: password 1	Read	Write	xxx	0	1	0	0	1
2	Protection: password 1	Read	Write	xxx	0	1	0	1	1
3	Protection: password 1	Read	Write	xxx	0	1	1	0	1
4	Protection: password 1	Read	No Write	xxx	0	1	1	1	1