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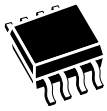
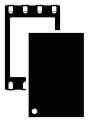
M24LR64-R

Dynamic NFC/RFID tag IC with 64-Kbit EEPROM with I²C bus and ISO 15693 RF interface

Datasheet - production data



SO8 (MN)
150 mils width



UFDFPN8 (MC)
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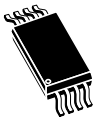
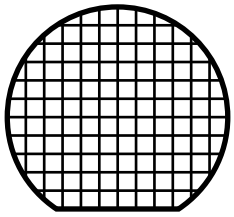


TSSOP8 (DW)



Sawn wafer on UV tape

Features

I²C interface

- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltage:
  - 1.8 V to 5.5 V
- Byte and Page Write (up to 4 bytes)
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection

Contactless interface

- ISO 15693 and ISO 18000-3 mode 1 compatible
- 13.56 MHz ± 7 kHz carrier frequency
- To tag:
  - 10% or 100% ASK modulation using 1/4 (26 kbit/s) or 1/256 (1.6 kbit/s) pulse position coding
- From tag:
  - load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 kbit/s) or high (26 kbit/s) data rate mode.
  - Supports the 53 kbit/s data rate with Fast commands
- Internal tuning capacitance:
  - 27.5 pF
- 64-bit unique identifier (UID)
- Read Block & Write (32-bit Blocks)

Memory

- 64-Kbit EEPROM organized into:
  - 8192 bytes in I²C mode
  - 2048 blocks of 32 bits in RF mode
- Write time:
  - I²C: 5 ms (Max.)
  - RF: 5.75 ms including the internal Verify time
- More than 1 Million write cycles
- Multiple password protection in RF mode
- Single password protection in I²C mode
- More than 40-year data retention
- Package:
  - ECOPACK2® (RoHS compliant and Halogen-free)

Contents

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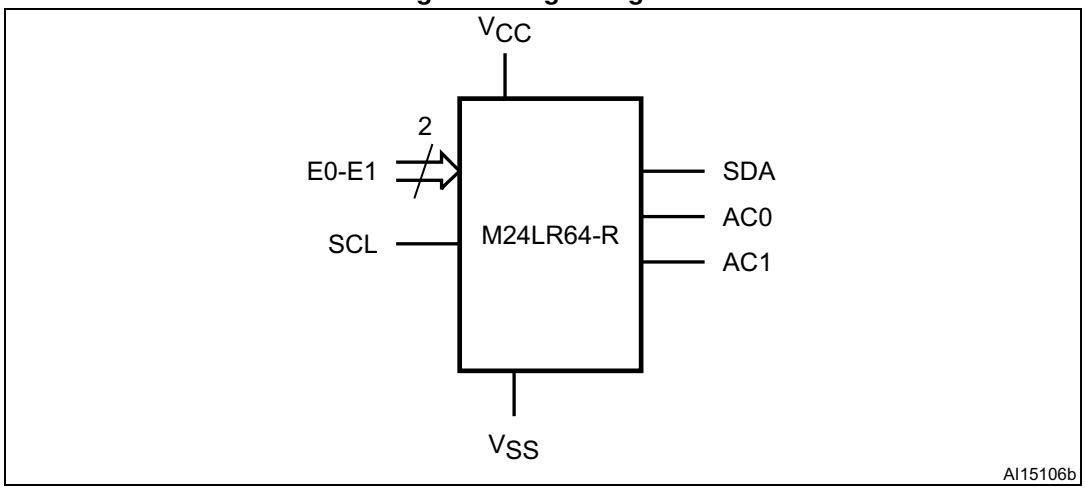
1 Description

The M24LR64-R device is a Dynamic NFC/RFID tag IC with a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR64-R is organized as 8192 × 8 bits in the I^2C mode and as 2048 × 32 bits in the ISO 15693 and ISO 18000-3 mode 1 RF mode.

Figure 1. Logic diagram



I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit ($\overline{RW}$) (as described in *Table 2*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR64-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 kbits/s using the 1/256 pulse coding mode or a data rate of 26 kbit/s using the 1/4 pulse coding mode.

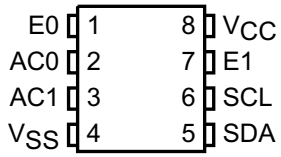
Outgoing data are generated by the M24LR64-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR64-R at 6.6 kbit/s in low data rate mode and 26 kbit/s high data rate mode. The M24LR64-R supports the 53 kbit/s in high data rate mode in one subcarrier frequency at 423 kHz.

The M24LR64-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

Table 1. Signal names

Signal name	Function	Direction
E0, E1	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections



AI15107

1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

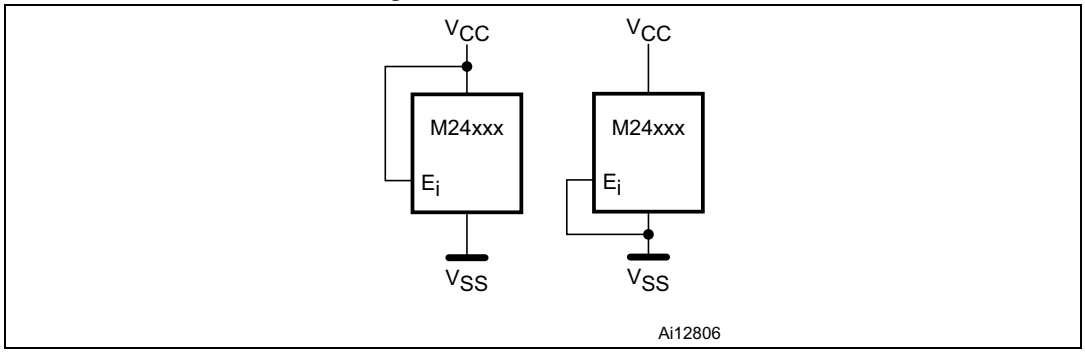
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1)

These input signals are used to set the value that is to be looked for on the two least significant bits (b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0,0).

Figure 3. Device select code



2.4 Antenna coil (AC0, AC1)

These inputs are used to connect the device to an external coil exclusively. It is advised to not connect any other DC or AC path to AC0 and AC1 pads. When correctly tuned, the coil is used to power and access the device using the ISO 15693 and ISO 18000-3 mode 1 protocols.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the M24LR64-R, while preventing the internal power supply (rectified RF waveforms) to output a DC voltage on the V_{CC} pin.

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 100*). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal I²C write cycle (t_W).

2.6.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 100*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode, however, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

Figure 4. I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

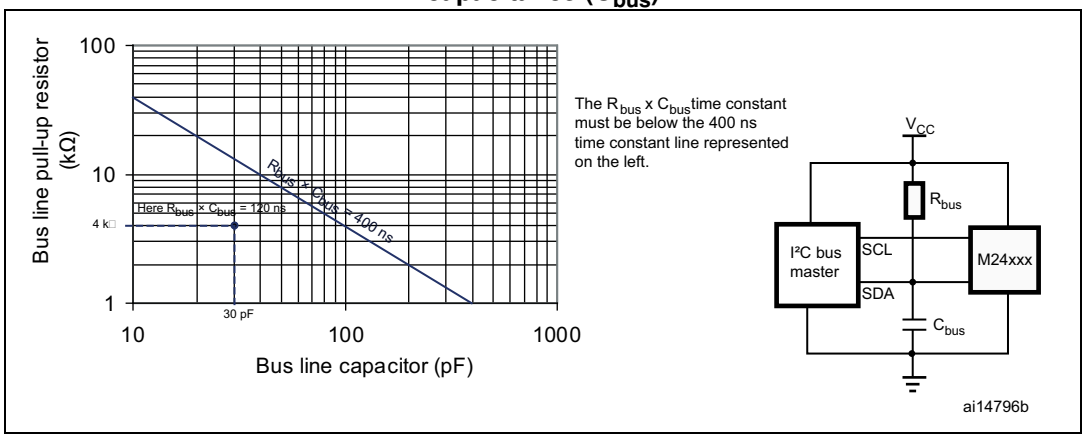


Figure 5. I^2C bus protocol

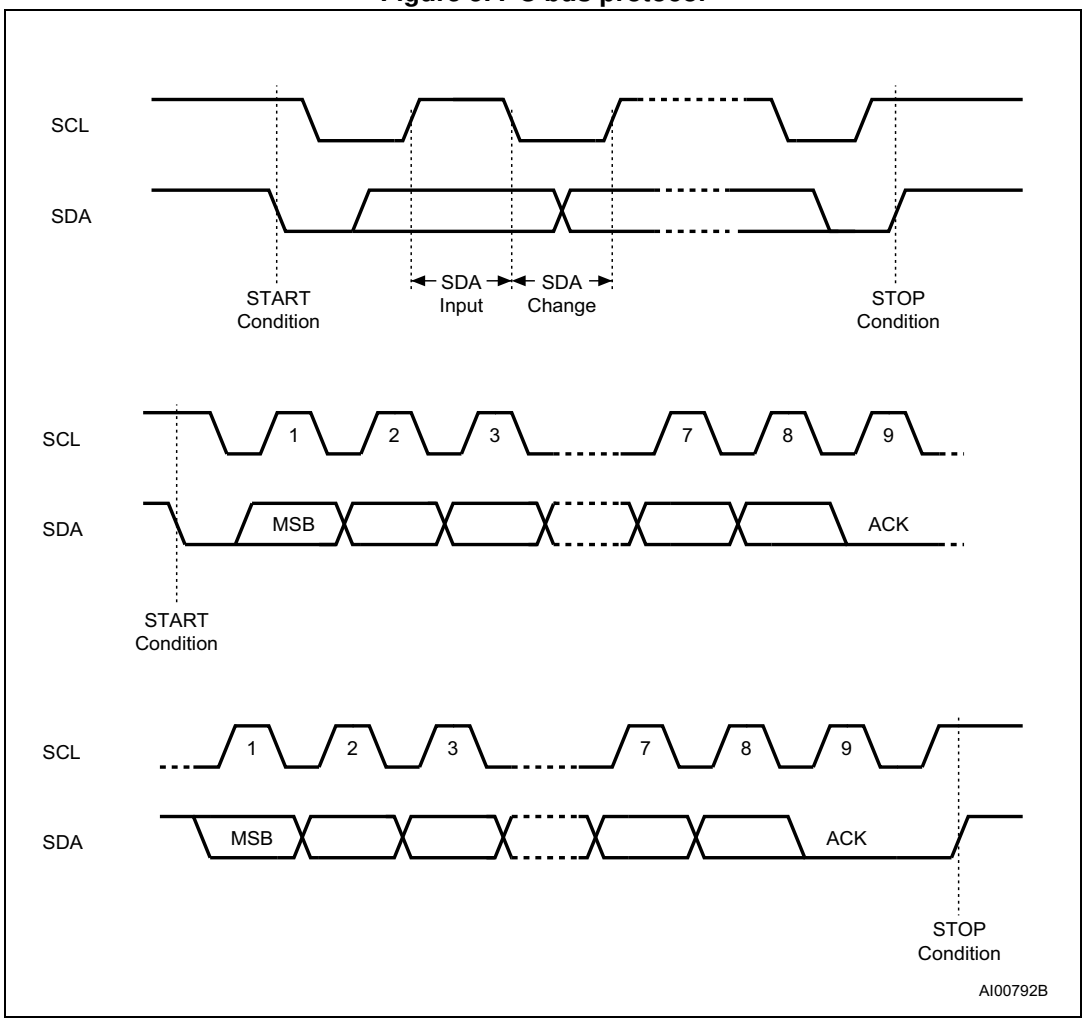


Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2(3)	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0 and E1 are compared against the respective external pins on the memory device.
3. E2 is not connected to any external pin. It is however used to address the M24LR64-R as described in *Section 3* and *Section 4*.

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 User memory organization

The M24LR64-R is divided into 64 sectors of 32 blocks of 32 bits as shown in *Table 5*. *Figure 7* shows the memory sector organization. Each sector can be individually read- and/or write-protected using a specific password command. Read and write operations are possible if the addressed data are not in a protected sector.

The M24LR64-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user and its value is written by ST on the production line.

The M24LR64-R includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The M24LR64-R has four additional 32-bit blocks that store an I^2C password plus three RF password codes.

Figure 6. Block diagram

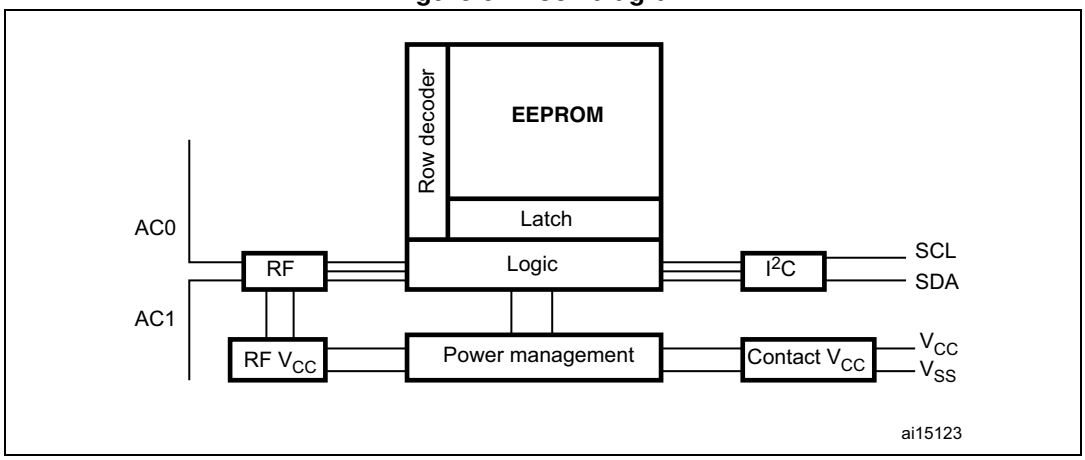
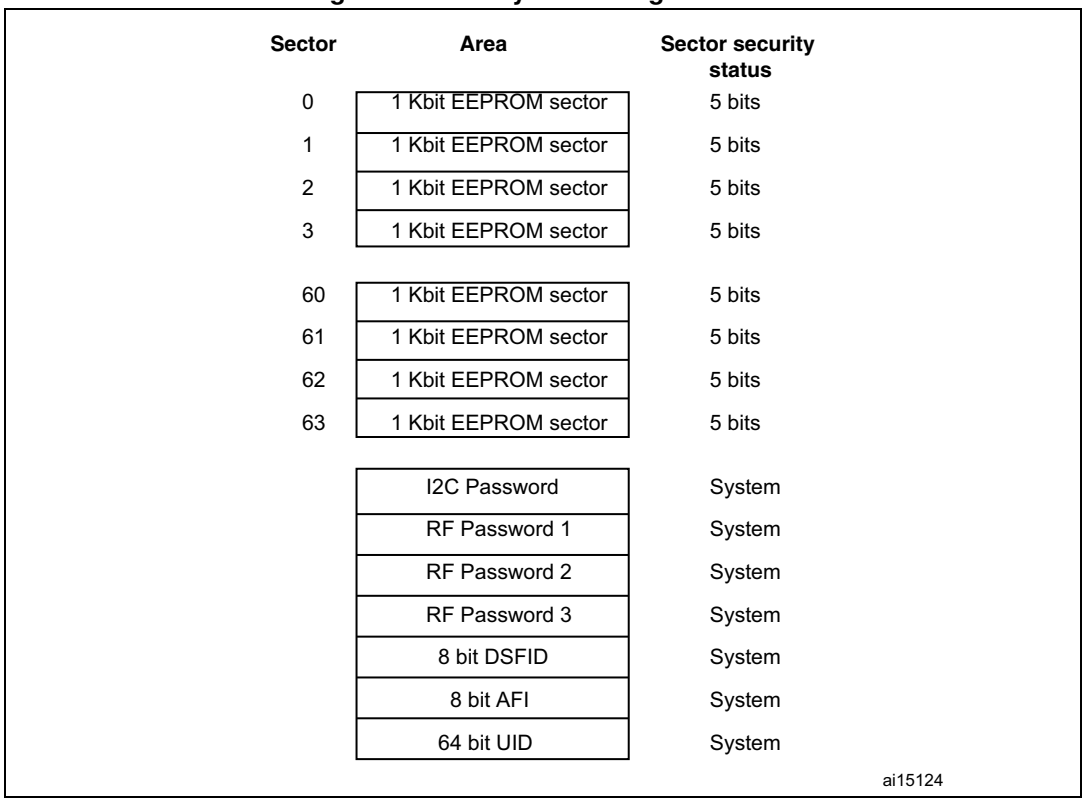


Figure 7. Memory sector organization



Sector details

The M24LR64-R user memory is divided into 64 sectors. Each sector contains 1024 bits. The protection scheme is described in *Section 4: System memory area*.

In RF mode, a sector provides 32 blocks of 32 bits. Each read and write access are done by block. Read and write block accesses are controlled by a Sector Security Status byte that defines the access rights to all the 32 blocks contained in the sector. If the sector is not protected, a Write command updates the complete 32 bits of the selected block.

In I^2C mode, a sector provides 128 bytes that can be individually accessed in read and write modes. When protected by the corresponding I2C_Write_Lock bit, the entire sector is write-protected. To access the user memory, the device select code used for any I^2C command must have the E2 Chip Enable address at 0.

Table 5. Sector details

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	0	0	user	user	user	user
	1	4	user	user	user	user
	2	8	user	user	user	user
	3	12	user	user	user	user
	4	16	user	user	user	user
	5	20	user	user	user	user
	6	24	user	user	user	user
	7	28	user	user	user	user
	8	32	user	user	user	user
	9	36	user	user	user	user
	10	40	user	user	user	user
	11	44	user	user	user	user
	12	48	user	user	user	user
	13	52	user	user	user	user
	14	56	user	user	user	user
	15	60	user	user	user	user
	16	64	user	user	user	user
	17	68	user	user	user	user
	18	72	user	user	user	user
	19	76	user	user	user	user
	20	80	user	user	user	user
	21	84	user	user	user	user
	22	88	user	user	user	user
	23	92	user	user	user	user
	24	96	user	user	user	user
	25	100	user	user	user	user
	26	104	user	user	user	user
	27	108	user	user	user	user
	28	112	user	user	user	user
	29	116	user	user	user	user
	30	120	user	user	user	user
	31	124	user	user	user	user

Table 5. Sector details (continued)

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
1	32	128	user	user	user	user
	33	132	user	user	user	user
	34	136	user	user	user	user
	35	140	user	user	user	user
	36	144	user	user	user	user
	37	148	user	user	user	user
	38	152	user	user	user	user
	39	156	user	user	user	user
	...	...	...	...	...	...
...	...	...	...	...	...	...

Table 5. Sector details (continued)

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
63	2016	8064	user	user	user	user
	2017	8068	user	user	user	user
	2018	8072	user	user	user	user
	2019	8076	user	user	user	user
	2020	8080	user	user	user	user
	2021	8084	user	user	user	user
	2022	8088	user	user	user	user
	2023	8092	user	user	user	user
	2024	8096	user	user	user	user
	2025	8100	user	user	user	user
	2026	8104	user	user	user	user
	2027	8108	user	user	user	user
	2028	8112	user	user	user	user
	2029	8116	user	user	user	user
	2030	8120	user	user	user	user
	2031	8124	user	user	user	user
	2032	8128	user	user	user	user
	2033	8132	user	user	user	user
	2034	8136	user	user	user	user
	2035	8140	user	user	user	user
	2036	8144	user	user	user	user
	2037	8148	user	user	user	user
	2038	8152	user	user	user	user
	2039	8156	user	user	user	user
	2040	8160	user	user	user	user
	2041	8164	user	user	user	user
	2042	8168	user	user	user	user
	2043	8172	user	user	user	user
	2044	8176	user	user	user	user
	2045	8180	user	user	user	user
	2046	8184	user	user	user	user
	2047	8188	user	user	user	user

4 System memory area

4.1 M24LR64-R RF block security

The M24LR64-R provides a special protection mechanism based on passwords. Each memory sector of the M24LR64-R can be individually protected by one out of three available passwords, and each sector can also have Read/Write access conditions set.

Each memory sector of the M24LR64-R is assigned with a Sector security status byte including a Sector Lock bit, two Password Control bits and two Read/Write protection bits as shown in *Table 7*. *Table 6* describes the organization of the Sector security status byte which can be read using the Read Single Block and Read Multiple Block commands with the Option_flag set to '1'.

On delivery, the default value of the SSS bytes is reset to 00h.

Table 6. Sector Security Status Byte area

I^2C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	0	SSS 3	SSS 2	SSS 1	SSS 0
E2 = 1	4	SSS 7	SSS 6	SSS 5	SSS 4
E2 = 1	8	SSS 11	SSS 10	SSS 9	SSS 8
E2 = 1	12	SSS 15	SSS 14	SSS 13	SSS 12
E2 = 1	16	SSS 19	SSS 18	SSS 17	SSS 16
E2 = 1	20	SSS 23	SSS 22	SSS 21	SSS 20
E2 = 1	24	SSS 27	SSS 26	SSS 25	SSS 24
E2 = 1	28	SSS 31	SSS 30	SSS 29	SSS 28
E2 = 1	32	SSS 35	SSS 34	SSS 33	SSS 32
E2 = 1	36	SSS 39	SSS 38	SSS 37	SSS 36
E2 = 1	40	SSS 43	SSS 42	SSS 41	SSS 40
E2 = 1	44	SSS 47	SSS 46	SSS 45	SSS 44
E2 = 1	48	SSS 51	SSS 50	SSS 49	SSS 48
E2 = 1	52	SSS 55	SSS 54	SSS 53	SSS 52
E2 = 1	56	SSS 59	SSS 58	SSS 57	SSS 56
E2 = 1	60	SSS 63	SSS 62	SSS 61	SSS 60

Table 7. Sector security status byte organization

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	Password Control bits		Read / Write protection bits		Sector Lock

When the Sector Lock bit is set to '1', for instance by issuing a Lock-sector Password command, the 2 Read/Write protection bits (b_1, b_2) are used to set the Read/Write access of the sector as described in *Table 8*.

Table 8. Read / Write protection bit setting

Sector Lock	b_2, b_1	Sector access when password presented		Sector access when password not presented	
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

The next 2 bits of the Sector security status byte (b_3, b_4) are the Password Control bits. The value these two bits is used to link a password to the sector as defined in *Table 9*.

Table 9. Password Control bits

b_4, b_3	Password
00	The sector is not protected by a Password
01	The sector is protected by the Password 1
10	The sector is protected by the Password 2
11	The sector is protected by the Password 3

The M24LR64-R password protection is organized around a dedicated set of commands plus a system area of three password blocks where the password values are stored. This system area is described in *Table 10*.

Table 10. Password system area

Block number	32-bit password number
1	Password 1
2	Password 2
3	Password 3

The dedicated password commands are:

- **Write-sector Password:**

  The Write-sector Password command is used to write a 32-bit block into the password system area. This command must be used to update password values. After the write cycle, the new password value is automatically activated. It is possible to modify a password value after issuing a valid Present-sector Password command.
  On delivery, the three default password values are set to 0000 0000h and are activated.

- **Lock-sector Password:**

  The Lock-sector Password command is used to set the Sector security status byte of the selected sector. Bits b_4 to b_1 of the Sector security status byte are affected by the Lock-sector Password command. The Sector Lock bit, b_0, is set to '1' automatically. After issuing a Lock-sector Password command, the protection settings of the selected

sector are activated. The protection of a locked block cannot be changed in RF mode. A Lock-sector Password command sent to a locked sector returns an error code.

- **Present-sector Password:**

  The Present-sector Password command is used to present one of the three passwords to the M24LR64-R in order to modify the access rights of all the memory sectors linked to that password (*Table 8*) including the password itself. If the presented password is correct, the access rights remain activated until the tag is powered off or until a new Present-sector Password command is issued. If the presented password value is not correct, all the access rights of all the memory sectors are deactivated.

- **Sector security status byte area access conditions in I^2C mode:**

  In I^2C mode, read access to the Sector security status byte area is always allowed. Write access depends on the correct presentation of the I^2C password (see *I^2C Present Password command description on page 27*).

  To access the Sector security status byte area, the device select code used for any I^2C command must have the E2 Chip Enable address at 1.

  An I^2C write access to a Sector security status byte re-initializes the RF access condition to the given memory sector.

4.2 Example of the M24LR64-R security protection

Table 11 and *Table 12* show the sector security protections before and after a valid Present-sector Password command. *Table 11* shows the sector access rights of an M24LR64-R after power-up. After a valid Present-sector Password command with password 1, the memory sector access is changed as shown in *Table 12*.

Table 11. M24LR64-R sector security protection after power-up

Sector address				Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: Standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: Pswd 1	Read	No Write	xxx	0	1	0	0	1
2	Protection: Pswd 1	Read	Write	xxx	0	1	0	1	1
3	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	0	1
4	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	1	1