



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

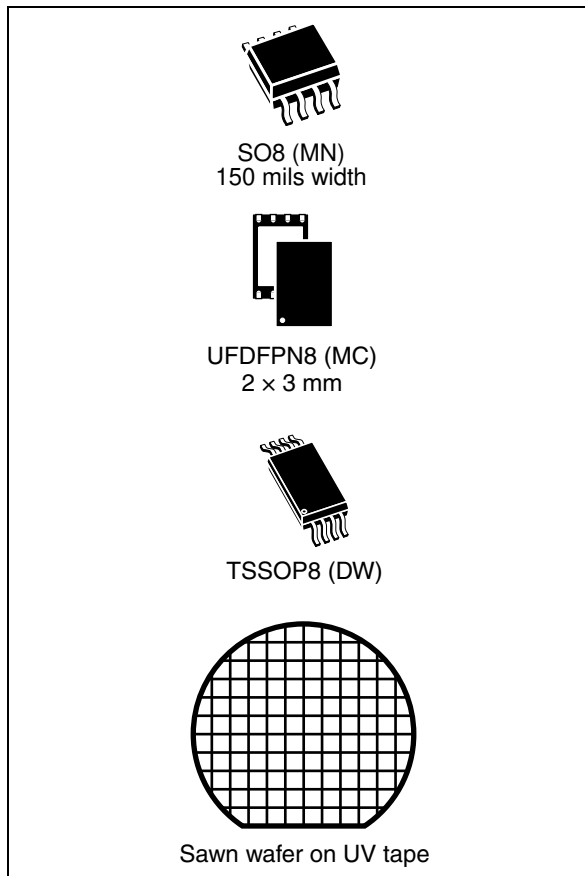
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**Dynamic NFC/RFID tag IC with 64-Kbit EEPROM
with I²C bus and ISO 15693 RF interface**

Datasheet - production data

**Features****I²C interface**

- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltage:
 - 1.8 V to 5.5 V
- Byte and Page Write (up to 4 bytes)
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection

Contactless interface

- ISO 15693 and ISO 18000-3 mode 1 compatible
- 13.56 MHz \pm 7 kHz carrier frequency
- To tag:
 - 10% or 100% ASK modulation using 1/4 (26 kbit/s) or 1/256 (1.6 kbit/s) pulse position coding
- From tag:
 - load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 kbit/s) or high (26 kbit/s) data rate mode.
 - Supports the 53 kbit/s data rate with Fast commands
- Internal tuning capacitance:
 - 27.5 pF
- 64-bit unique identifier (UID)
- Read Block & Write (32-bit Blocks)

Memory

- 64-Kbit EEPROM organized into:
 - 8192 bytes in I²C mode
 - 2048 blocks of 32 bits in RF mode
- Write time:
 - I²C: 5 ms (Max.)
 - RF: 5.75 ms including the internal Verify time
- More than 1 Million write cycles
- Multiple password protection in RF mode
- Single password protection in I²C mode
- More than 40-year data retention
- Package:
 - ECOPACK2[®] (RoHS compliant and Halogen-free)

Contents

- 1 Description 12**
- 2 Signal description 14**
 - 2.1 Serial Clock (SCL) 14
 - 2.2 Serial Data (SDA) 14
 - 2.3 Chip Enable (E0, E1) 14
 - 2.4 Antenna coil (AC0, AC1) 14
 - 2.5 V_{SS} ground 15
 - 2.6 Supply voltage (V_{CC}) 15
 - 2.6.1 Operating supply voltage V_{CC} 15
 - 2.6.2 Power-up conditions 15
 - 2.6.3 Device reset 15
 - 2.6.4 Power-down conditions 15
- 3 User memory organization 18**
- 4 System memory area 23**
 - 4.1 M24LR64-R RF block security 23
 - 4.2 Example of the M24LR64-R security protection 25
 - 4.3 I2C_Write_Lock bit area 26
 - 4.4 System parameters 26
 - 4.5 M24LR64-R I²C password security 27
 - 4.5.1 I²C Present Password command description 27
 - 4.5.2 I²C Write Password command description 28
- 5 I²C device operation 30**
 - 5.1 Start condition 30
 - 5.2 Stop condition 30
 - 5.3 Acknowledge bit (ACK) 30
 - 5.4 Data Input 30
 - 5.5 Memory addressing 30
 - 5.6 Write operations 31
 - 5.7 Byte Write 32

5.8	Page Write	32
5.9	Minimizing system delays by polling on ACK	34
5.10	Read operations	35
5.11	Random Address Read	35
5.12	Current Address Read	36
5.13	Sequential Read	36
5.14	Acknowledge in Read mode	36
6	User memory initial state	37
7	RF device operation	37
7.1	Commands	38
7.2	Initial dialog for vicinity cards	38
7.2.1	Power transfer	39
7.2.2	Frequency	39
7.2.3	Operating field	39
8	Communication signal from VCD to M24LR64-R	40
9	Data rate and data coding	42
9.1	Data coding mode: 1 out of 256	42
9.2	Data coding mode: 1 out of 4	43
9.3	VCD to M24LR64-R frames	45
9.4	Start of frame (SOF)	45
10	Communications signal from M24LR64-R to VCD	47
10.1	Load modulation	47
10.2	Subcarrier	47
10.3	Data rates	47
11	Bit representation and coding	48
11.1	Bit coding using one subcarrier	48
11.1.1	High data rate	48
11.1.2	Low data rate	49
11.2	Bit coding using two subcarriers	49
11.3	High data rate	49

11.4 Low data rate 50

12 M24LR64-R to VCD frames 51

12.1 SOF when using one subcarrier 51

12.2 High data rate 51

12.3 Low data rate 51

12.4 SOF when using two subcarriers 52

12.5 High data rate 52

12.6 Low data rate 52

12.7 EOF when using one subcarrier 53

12.8 High data rate 53

12.9 Low data rate 53

12.10 EOF when using two subcarriers 54

12.11 High data rate 54

12.12 Low data rate 54

13 Unique identifier (UID) 55

14 Application family identifier (AFI) 56

15 Data storage format identifier (DSFID) 57

15.1 CRC 57

16 M24LR64-R protocol description 58

17 M24LR64-R states 60

17.1 Power-off state 60

17.2 Ready state 60

17.3 Quiet state 60

17.4 Selected state 60

18 Modes 62

18.1 Addressed mode 62

18.2 Non-addressed mode (general request) 62

18.3 Select mode 62

19	Request format	63
	19.1 Request flags	63
20	Response format	65
	20.1 Response flags	65
	20.2 Response error code	66
21	Anticollision	67
	21.1 Request parameters	67
22	Request processing by the M24LR64-R	69
23	Explanation of the possible cases	70
24	Inventory Initiated command	72
25	Timing definition	73
	25.1 t ₁ : M24LR64-R response delay	73
	25.2 t ₂ : VCD new request delay	73
	25.3 t ₃ : VCD new request delay in the absence of a response from the M24LR64-R	73
26	Commands codes	74
	26.1 Inventory	74
	26.2 Stay Quiet	75
	26.3 Read Single Block	76
	26.4 Write Single Block	77
	26.5 Read Multiple Block	78
	26.6 Select	80
	26.7 Reset to Ready	81
	26.8 Write AFI	82
	26.9 Lock AFI	83
	26.10 Write DSFID	85
	26.11 Lock DSFID	87
	26.12 Get System Info	88
	26.13 Get Multiple Block Security Status	89

26.14	Write-sector Password	91
26.15	Lock-sector Password	92
26.16	Present-sector Password	94
26.17	Fast Read Single Block	95
26.18	Fast Inventory Initiated	97
26.19	Fast Initiate	98
26.20	Fast Read Multiple Block	99
26.21	Inventory Initiated	101
26.22	Initiate	102
27	Maximum rating	104
28	I²C DC and AC parameters	105
29	RF electrical parameters	109
30	Package mechanical data	111
31	Part numbering	114
Appendix A	Anticollision algorithm (informative)	116
A.1	Algorithm for pulsed slots	116
Appendix B	CRC (informative)	117
B.1	CRC error detection method	117
B.2	CRC calculation example	117
Appendix C	Application family identifier (AFI) (informative)	119
	Revision history	120

List of tables

Table 1.	Signal names	13
Table 2.	Device select code	17
Table 3.	Address most significant byte	17
Table 4.	Address least significant byte	17
Table 5.	Sector details	20
Table 6.	Sector Security Status Byte area	23
Table 7.	Sector security status byte organization	23
Table 8.	Read / Write protection bit setting	24
Table 9.	Password Control bits	24
Table 10.	Password system area	24
Table 11.	M24LR64-R sector security protection after power-up	25
Table 12.	M24LR64-R sector security protection after a valid presentation of password 1	26
Table 13.	I2C_Write_Lock bit	26
Table 14.	System parameter sector	27
Table 15.	Operating modes	31
Table 16.	10% modulation parameters	40
Table 17.	Response data rates	47
Table 18.	UID format	55
Table 19.	CRC transmission rules	57
Table 20.	VCD request frame format	58
Table 21.	M24LR64-R Response frame format	58
Table 22.	M24LR64-R response depending on Request_flags	61
Table 23.	General request format	63
Table 24.	Definition of request flags 1 to 4	63
Table 25.	Request flags 5 to 8 when Bit 3 = 0	64
Table 26.	Request flags 5 to 8 when Bit 3 = 1	64
Table 27.	General response format	65
Table 28.	Definitions of response flags 1 to 8	65
Table 29.	Response error code definition	66
Table 30.	Inventory request format	67
Table 31.	Example of the addition of 0 bits to an 11-bit mask value	67
Table 32.	Timing values	73
Table 33.	Command codes	74
Table 34.	Inventory request format	74
Table 35.	Inventory response format	75
Table 36.	Stay Quiet request format	75
Table 37.	Read Single Block request format	76
Table 38.	Read Single Block response format when Error_flag is NOT set	76
Table 39.	Sector security status	76
Table 40.	Read Single Block response format when Error_flag is set	77
Table 41.	Write Single Block request format	77
Table 42.	Write Single Block response format when Error_flag is NOT set	78
Table 43.	Write Single Block response format when Error_flag is set	78
Table 44.	Read Multiple Block request format	79
Table 45.	Read Multiple Block response format when Error_flag is NOT set	79
Table 46.	Sector security status	79
Table 47.	Read Multiple Block response format when Error_flag is set	79
Table 48.	Select request format	80

Table 49.	Select Block response format when Error_flag is NOT set.	80
Table 50.	Select response format when Error_flag is set.	80
Table 51.	Reset to Ready request format.	81
Table 52.	Reset to Ready response format when Error_flag is NOT set.	81
Table 53.	Reset to ready response format when Error_flag is set.	81
Table 54.	Write AFI request format.	82
Table 55.	Write AFI response format when Error_flag is NOT set.	82
Table 56.	Write AFI response format when Error_flag is set.	83
Table 57.	Lock AFI request format.	83
Table 58.	Lock AFI response format when Error_flag is NOT set.	84
Table 59.	Lock AFI response format when Error_flag is set.	84
Table 60.	Write DSFID request format.	85
Table 61.	Write DSFID response format when Error_flag is NOT set.	85
Table 62.	Write DSFID response format when Error_flag is set.	85
Table 63.	Lock DSFID request format.	87
Table 64.	Lock DSFID response format when Error_flag is NOT set.	87
Table 65.	Lock DSFID response format when Error_flag is set.	87
Table 66.	Get System Info request format.	88
Table 67.	Get System Info response format when Error_flag is NOT set.	88
Table 68.	Get System Info response format when Error_flag is set.	89
Table 69.	Get Multiple Block Security Status request format.	89
Table 70.	Get Multiple Block Security Status response format when Error_flag is NOT set.	90
Table 71.	Sector security status.	90
Table 72.	Get Multiple Block Security Status response format when Error_flag is set.	90
Table 73.	Write-sector Password request format.	91
Table 74.	Write-sector Password response format when Error_flag is NOT set.	91
Table 75.	Write-sector Password response format when Error_flag is set.	91
Table 76.	Lock-sector Password request format.	92
Table 77.	Sector security status.	93
Table 78.	Lock-sector Password response format when Error_flag is NOT set.	93
Table 79.	Lock-sector Password response format when Error_flag is set.	93
Table 80.	Present-sector Password request format.	94
Table 81.	Present-sector Password response format when Error_flag is NOT set.	94
Table 82.	Present-sector Password response format when Error_flag is set.	94
Table 83.	Fast Read Single Block request format.	95
Table 84.	Fast Read Single Block response format when Error_flag is NOT set.	95
Table 85.	Sector security status.	96
Table 86.	Fast Read Single Block response format when Error_flag is set.	96
Table 87.	Fast Inventory Initiated request format.	97
Table 88.	Fast Inventory Initiated response format.	97
Table 89.	Fast Initiate request format.	98
Table 90.	Fast Initiate response format.	98
Table 91.	Fast Read Multiple Block request format.	99
Table 92.	Fast Read Multiple Block response format when Error_flag is NOT set.	99
Table 93.	Sector security status if Option_flag is set.	99
Table 94.	Fast Read Multiple Block response format when Error_flag is set.	100
Table 95.	Inventory Initiated request format.	101
Table 96.	Inventory Initiated response format.	101
Table 97.	Initiate request format.	102
Table 98.	Initiate Initiated response format.	102
Table 99.	Absolute maximum ratings.	104
Table 100.	I ² C operating conditions.	105

Table 101.	AC test measurement conditions	105
Table 102.	Input parameters.	105
Table 103.	I ² C DC characteristics	106
Table 104.	I ² C AC characteristics.	107
Table 105.	RF characteristics	109
Table 106.	Operating conditions.	110
Table 107.	SO8N – 8-lead plastic small outline, 150 mils body width, package data.	111
Table 108.	UFDFPN8 (MLP8) – Ultra thin fine pitch dual flat package no lead 2 x 3 mm, package mechanical data.	112
Table 109.	TSSOP8 – 8-lead thin shrink small outline, package mechanical data.	113
Table 110.	Ordering information scheme for packaged devices	114
Table 111.	Ordering information scheme for bare die devices	115
Table 112.	CRC definition.	117
Table 113.	AFI coding.	119
Table 114.	Document revision history	120

List of figures

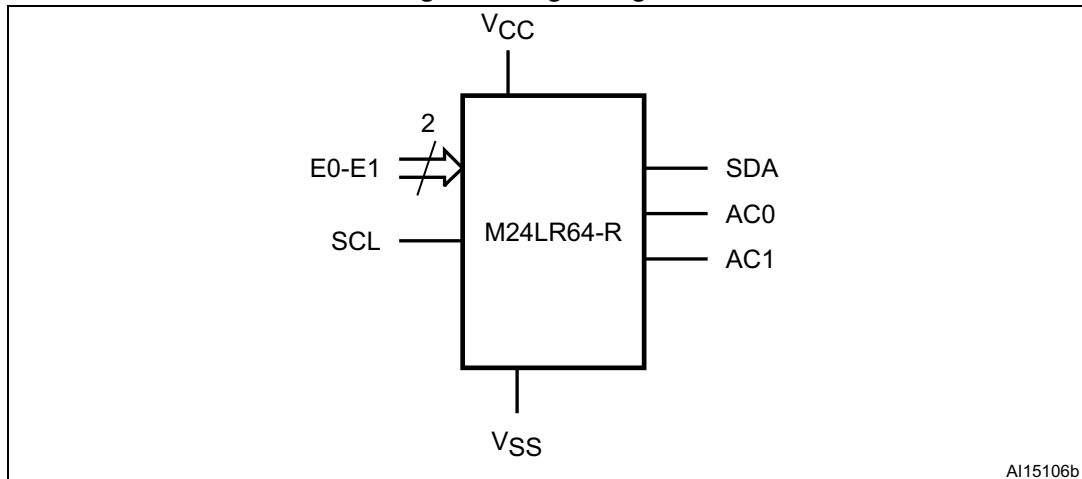
Figure 1.	Logic diagram	12
Figure 2.	8-pin package connections	13
Figure 3.	Device select code	14
Figure 4.	I ² C Fast mode ($f_C = 400$ kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})	16
Figure 5.	I ² C bus protocol	16
Figure 6.	Block diagram	18
Figure 7.	Memory sector organization	19
Figure 8.	I ² C Present Password command	28
Figure 9.	I ² C Write Password command	29
Figure 10.	Write mode sequences with I2C_Write_Lock bit = 1 (data write inhibited)	31
Figure 11.	Write mode sequences with I2C_Write_Lock bit = 0 (data write enabled)	33
Figure 12.	Write cycle polling flowchart using ACK	33
Figure 13.	Read mode sequences	35
Figure 14.	100% modulation waveform	40
Figure 15.	10% modulation waveform	41
Figure 16.	1 out of 256 coding mode	42
Figure 17.	Detail of a time period	43
Figure 18.	1 out of 4 coding mode	44
Figure 19.	1 out of 4 coding example	44
Figure 20.	SOF to select 1 out of 256 data coding mode	45
Figure 21.	SOF to select 1 out of 4 data coding mode	45
Figure 22.	EOF for either data coding mode	46
Figure 23.	Logic 0, high data rate	48
Figure 24.	Logic 0, high data rate x2	48
Figure 25.	Logic 1, high data rate	48
Figure 26.	Logic 1, high data rate x2	48
Figure 27.	Logic 0, low data rate	49
Figure 28.	Logic 0, low data rate x2	49
Figure 29.	Logic 1, low data rate	49
Figure 30.	Logic 1, low data rate x2	49
Figure 31.	Logic 0, high data rate	50
Figure 32.	Logic 1, high data rate	50
Figure 33.	Logic 0, low data rate	50
Figure 34.	Logic 1, low data rate	50
Figure 35.	Start of frame, high data rate, one subcarrier	51
Figure 36.	Start of frame, high data rate, one subcarrier x2	51
Figure 37.	Start of frame, low data rate, one subcarrier	51
Figure 38.	Start of frame, low data rate, one subcarrier x2	52
Figure 39.	Start of frame, high data rate, two subcarriers	52
Figure 40.	Start of frame, low data rate, two subcarriers	52
Figure 41.	End of frame, high data rate, one subcarriers	53
Figure 42.	End of frame, high data rate, one subcarriers x2	53
Figure 43.	End of frame, low data rate, one subcarriers	53
Figure 44.	End of frame, low data rate, one subcarriers x2	53
Figure 45.	End of frame, high data rate, two subcarriers	54
Figure 46.	End of frame, low data rate, two subcarriers	54
Figure 47.	M24LR64-R decision tree for AFI	56

Figure 48.	M24LR64-R protocol timing	59
Figure 49.	M24LR64-R state transition diagram	61
Figure 50.	Principle of comparison between the mask, the slot number and the UID	68
Figure 51.	Description of a possible anticollision sequence	71
Figure 52.	Stay Quiet frame exchange between VCD and M24LR64-R	76
Figure 53.	Read Single Block frame exchange between VCD and M24LR64-R	77
Figure 54.	Write Single Block frame exchange between VCD and M24LR64-R	78
Figure 55.	Read Multiple Block frame exchange between VCD and M24LR64-R	80
Figure 56.	Select frame exchange between VCD and M24LR64-R	81
Figure 57.	Reset to Ready frame exchange between VCD and M24LR64-R	82
Figure 58.	Write AFI frame exchange between VCD and M24LR64-R	83
Figure 59.	Lock AFI frame exchange between VCD and M24LR64-R	84
Figure 60.	Write DSFID frame exchange between VCD and M24LR64-R	86
Figure 61.	Lock DSFID frame exchange between VCD and M24LR64-R	88
Figure 62.	Get System Info frame exchange between VCD and M24LR64-R	89
Figure 63.	Get Multiple Block Security Status frame exchange between VCD and M24LR64-R	90
Figure 64.	Write-sector Password frame exchange between VCD and M24LR64-R	92
Figure 65.	Lock-sector Password frame exchange between VCD and M24LR64-R	93
Figure 66.	Present-sector Password frame exchange between VCD and M24LR64-R	95
Figure 67.	Fast Read Single Block frame exchange between VCD and M24LR64-R	96
Figure 68.	Fast Initiate frame exchange between VCD and M24LR64-R	98
Figure 69.	Fast Read Multiple Block frame exchange between VCD and M24LR64-R	100
Figure 70.	Initiate frame exchange between VCD and M24LR64-R	103
Figure 71.	AC test measurement I/O waveform	105
Figure 72.	I ² C AC waveforms	108
Figure 73.	M24LR64-R synchronous timing, transmit and receive	110
Figure 74.	SO8N – 8-lead plastic small outline, 150 mils body width, package outline	111
Figure 75.	UFDFPN8 (MLP8) – Ultra thin fine pitch dual flat package no lead 2 x 3 mm, package outline	112
Figure 76.	TSSOP8 – 8-lead thin shrink small outline, package outline	113

1 Description

The M24LR64-R device is a Dynamic NFC/RFID tag IC with a dual-interface, electrically erasable programmable memory (EEPROM). It features an I²C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR64-R is organized as 8192 × 8 bits in the I²C mode and as 2048 × 32 bits in the ISO 15693 and ISO 18000-3 mode 1 RF mode.

Figure 1. Logic diagram



I²C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I²C bus definition.

The device behaves as a slave in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW) (as described in [Table 2](#)), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR64-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 kbit/s using the 1/256 pulse coding mode or a data rate of 26 kbit/s using the 1/4 pulse coding mode.

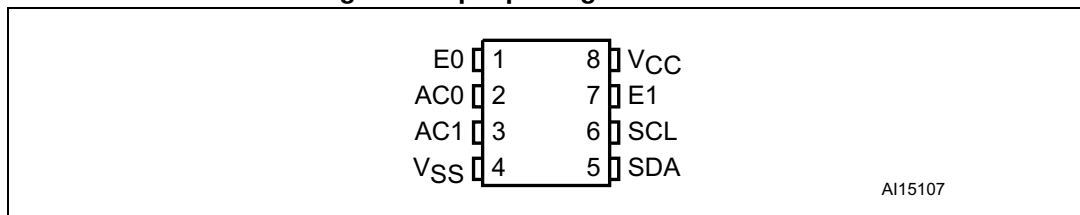
Outgoing data are generated by the M24LR64-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR64-R at 6.6 kbit/s in low data rate mode and 26 kbit/s high data rate mode. The M24LR64-R supports the 53 kbit/s in high data rate mode in one subcarrier frequency at 423 kHz.

The M24LR64-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

Table 1. Signal names

Signal name	Function	Direction
E0, E1	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O
V _{CC}	Supply voltage	-
V _{SS}	Ground	-

Figure 2. 8-pin package connections



1. See [Package mechanical data](#) section for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC} . (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

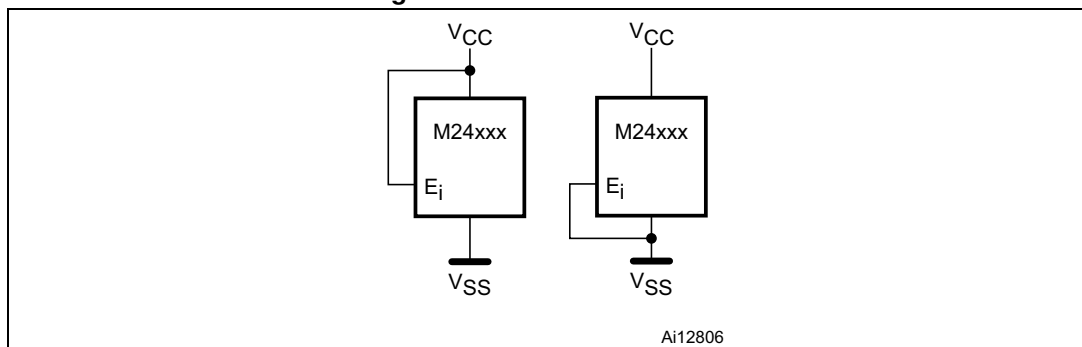
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC} . (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1)

These input signals are used to set the value that is to be looked for on the two least significant bits (b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS} , to establish the device select code as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0,0).

Figure 3. Device select code



2.4 Antenna coil (AC0, AC1)

These inputs are used to connect the device to an external coil exclusively. It is advised to not connect any other DC or AC path to AC0 and AC1 pads. When correctly tuned, the coil is used to power and access the device using the ISO 15693 and ISO 18000-3 mode 1 protocols.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the M24LR64-R, while preventing the internal power supply (rectified RF waveforms) to output a DC voltage on the V_{CC} pin.

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range must be applied (see [Table 100](#)). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal I²C write cycle (t_W).

2.6.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC} . The V_{CC} rise time must not vary faster than 1V/ μ s.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in [Table 100](#)). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode, however, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

Figure 4. I²C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

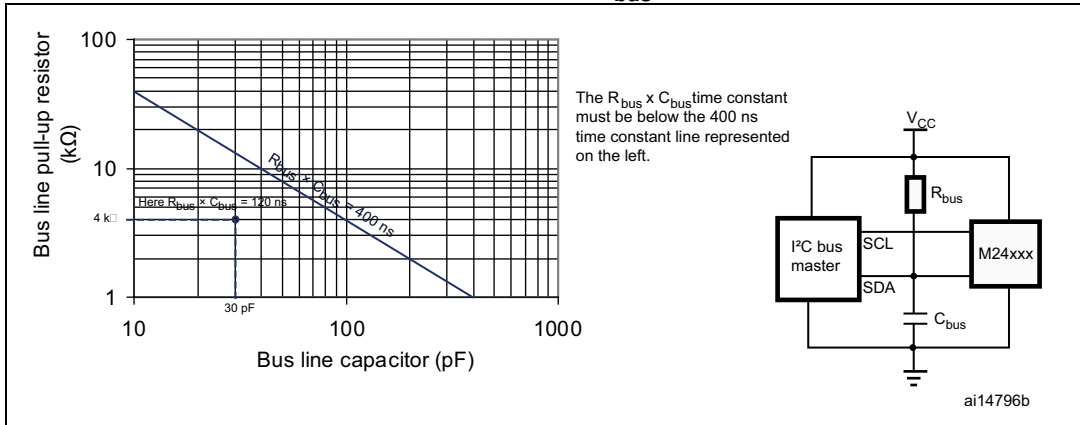


Figure 5. I²C bus protocol

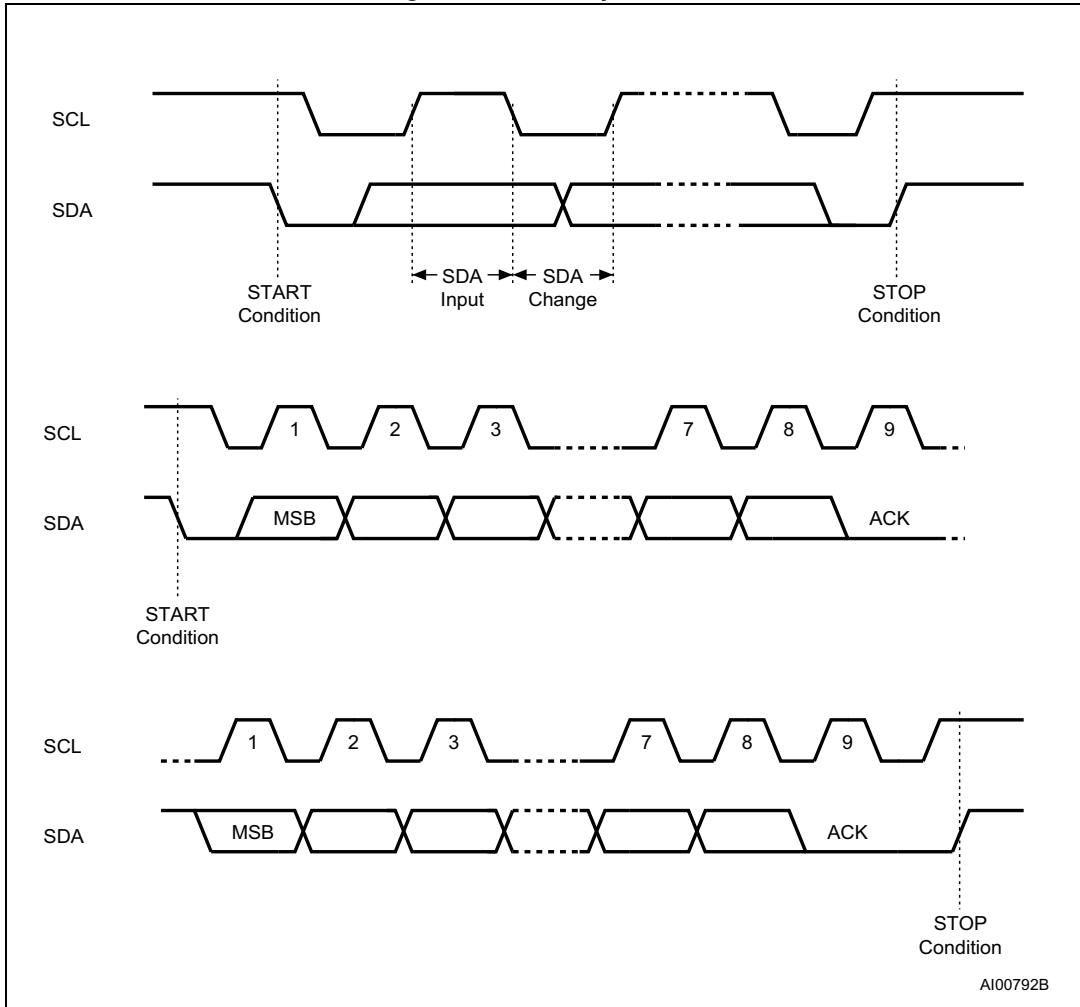


Table 2. Device select code

	Device type identifier ⁽¹⁾				Chip Enable address ⁽²⁾			\overline{RW}
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2 ⁽³⁾	E1	E0	\overline{RW}

1. The most significant bit, b7, is sent first.
2. E0 and E1 are compared against the respective external pins on the memory device.
3. E2 is not connected to any external pin. It is however used to address the M24LR64-R as described in [Section 3](#) and [Section 4](#).

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8
-----	-----	-----	-----	-----	-----	----	----

Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

3 User memory organization

The M24LR64-R is divided into 64 sectors of 32 blocks of 32 bits as shown in [Table 5](#). [Figure 7](#) shows the memory sector organization. Each sector can be individually read-and/or write-protected using a specific password command. Read and write operations are possible if the addressed data are not in a protected sector.

The M24LR64-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user and its value is written by ST on the production line.

The M24LR64-R includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The M24LR64-R has four additional 32-bit blocks that store an I²C password plus three RF password codes.

Figure 6. Block diagram

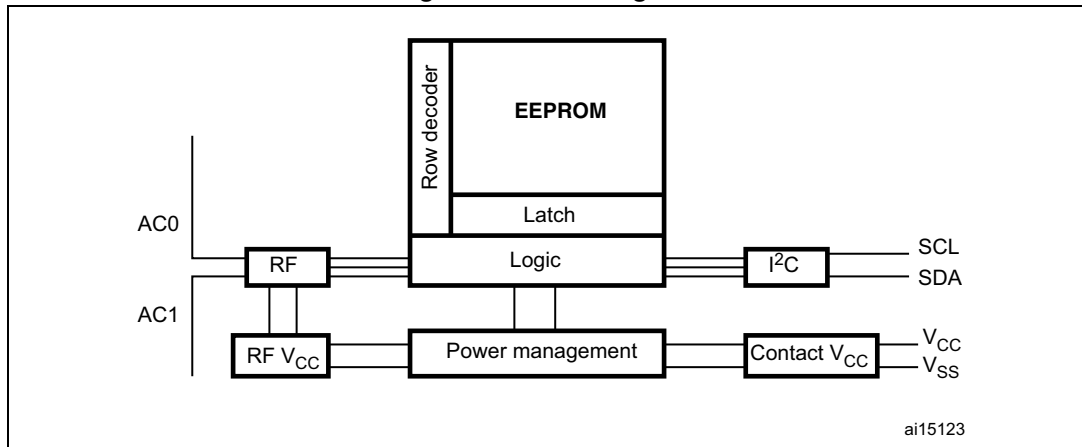


Figure 7. Memory sector organization

Sector	Area	Sector security status
0	1 Kbit EEPROM sector	5 bits
1	1 Kbit EEPROM sector	5 bits
2	1 Kbit EEPROM sector	5 bits
3	1 Kbit EEPROM sector	5 bits
60	1 Kbit EEPROM sector	5 bits
61	1 Kbit EEPROM sector	5 bits
62	1 Kbit EEPROM sector	5 bits
63	1 Kbit EEPROM sector	5 bits
	I2C Password	System
	RF Password 1	System
	RF Password 2	System
	RF Password 3	System
	8 bit DSFID	System
	8 bit AFI	System
	64 bit UID	System

ai15124

Sector details

The M24LR64-R user memory is divided into 64 sectors. Each sector contains 1024 bits. The protection scheme is described in [Section 4: System memory area](#).

In RF mode, a sector provides 32 blocks of 32 bits. Each read and write access are done by block. Read and write block accesses are controlled by a Sector Security Status byte that defines the access rights to all the 32 blocks contained in the sector. If the sector is not protected, a Write command updates the complete 32 bits of the selected block.

In I²C mode, a sector provides 128 bytes that can be individually accessed in read and write modes. When protected by the corresponding I2C_Write_Lock bit, the entire sector is write-protected. To access the user memory, the device select code used for any I²C command must have the E2 Chip Enable address at 0.

Table 5. Sector details

Sector number	RF block address	I ² C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	0	0	user	user	user	user
	1	4	user	user	user	user
	2	8	user	user	user	user
	3	12	user	user	user	user
	4	16	user	user	user	user
	5	20	user	user	user	user
	6	24	user	user	user	user
	7	28	user	user	user	user
	8	32	user	user	user	user
	9	36	user	user	user	user
	10	40	user	user	user	user
	11	44	user	user	user	user
	12	48	user	user	user	user
	13	52	user	user	user	user
	14	56	user	user	user	user
	15	60	user	user	user	user
	16	64	user	user	user	user
	17	68	user	user	user	user
	18	72	user	user	user	user
	19	76	user	user	user	user
	20	80	user	user	user	user
	21	84	user	user	user	user
	22	88	user	user	user	user
	23	92	user	user	user	user
	24	96	user	user	user	user
	25	100	user	user	user	user
	26	104	user	user	user	user
	27	108	user	user	user	user
	28	112	user	user	user	user
	29	116	user	user	user	user
	30	120	user	user	user	user
	31	124	user	user	user	user

Table 5. Sector details (continued)

Sector number	RF block address	I ² C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
1	32	128	user	user	user	user
	33	132	user	user	user	user
	34	136	user	user	user	user
	35	140	user	user	user	user
	36	144	user	user	user	user
	37	148	user	user	user	user
	38	152	user	user	user	user
	39	156	user	user	user	user
...
...

Table 5. Sector details (continued)

Sector number	RF block address	I ² C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
63	2016	8064	user	user	user	user
	2017	8068	user	user	user	user
	2018	8072	user	user	user	user
	2019	8076	user	user	user	user
	2020	8080	user	user	user	user
	2021	8084	user	user	user	user
	2022	8088	user	user	user	user
	2023	8092	user	user	user	user
	2024	8096	user	user	user	user
	2025	8100	user	user	user	user
	2026	8104	user	user	user	user
	2027	8108	user	user	user	user
	2028	8112	user	user	user	user
	2029	8116	user	user	user	user
	2030	8120	user	user	user	user
	2031	8124	user	user	user	user
	2032	8128	user	user	user	user
	2033	8132	user	user	user	user
	2034	8136	user	user	user	user
	2035	8140	user	user	user	user
	2036	8144	user	user	user	user
	2037	8148	user	user	user	user
	2038	8152	user	user	user	user
	2039	8156	user	user	user	user
	2040	8160	user	user	user	user
	2041	8164	user	user	user	user
	2042	8168	user	user	user	user
	2043	8172	user	user	user	user
	2044	8176	user	user	user	user
	2045	8180	user	user	user	user
2046	8184	user	user	user	user	
2047	8188	user	user	user	user	

4 System memory area

4.1 M24LR64-R RF block security

The M24LR64-R provides a special protection mechanism based on passwords. Each memory sector of the M24LR64-R can be individually protected by one out of three available passwords, and each sector can also have Read/Write access conditions set.

Each memory sector of the M24LR64-R is assigned with a Sector security status byte including a Sector Lock bit, two Password Control bits and two Read/Write protection bits as shown in [Table 7](#). [Table 6](#) describes the organization of the Sector security status byte which can be read using the Read Single Block and Read Multiple Block commands with the Option_flag set to '1'.

On delivery, the default value of the SSS bytes is reset to 00h.

Table 6. Sector Security Status Byte area

I ² C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	0	SSS 3	SSS 2	SSS 1	SSS 0
E2 = 1	4	SSS 7	SSS 6	SSS 5	SSS 4
E2 = 1	8	SSS 11	SSS 10	SSS 9	SSS 8
E2 = 1	12	SSS 15	SSS 14	SSS 13	SSS 12
E2 = 1	16	SSS 19	SSS 18	SSS 17	SSS 16
E2 = 1	20	SSS 23	SSS 22	SSS 21	SSS 20
E2 = 1	24	SSS 27	SSS 26	SSS 25	SSS 24
E2 = 1	28	SSS 31	SSS 30	SSS 29	SSS 28
E2 = 1	32	SSS 35	SSS 34	SSS 33	SSS 32
E2 = 1	36	SSS 39	SSS 38	SSS 37	SSS 36
E2 = 1	40	SSS 43	SSS 42	SSS 41	SSS 40
E2 = 1	44	SSS 47	SSS 46	SSS 45	SSS 44
E2 = 1	48	SSS 51	SSS 50	SSS 49	SSS 48
E2 = 1	52	SSS 55	SSS 54	SSS 53	SSS 52
E2 = 1	56	SSS 59	SSS 58	SSS 57	SSS 56
E2 = 1	60	SSS 63	SSS 62	SSS 61	SSS 60

Table 7. Sector security status byte organization

b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀
0	0	0	Password Control bits		Read / Write protection bits		Sector Lock

When the Sector Lock bit is set to '1', for instance by issuing a Lock-sector Password command, the 2 Read/Write protection bits (b₁, b₂) are used to set the Read/Write access of the sector as described in [Table 8](#).

Table 8. Read / Write protection bit setting

Sector Lock	b ₂ , b ₁	Sector access when password presented		Sector access when password not presented	
		Read	Write	Read	Write
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

The next 2 bits of the Sector security status byte (b₃, b₄) are the Password Control bits. The value these two bits is used to link a password to the sector as defined in [Table 9](#).

Table 9. Password Control bits

b ₄ , b ₃	Password
00	The sector is not protected by a Password
01	The sector is protected by the Password 1
10	The sector is protected by the Password 2
11	The sector is protected by the Password 3

The M24LR64-R password protection is organized around a dedicated set of commands plus a system area of three password blocks where the password values are stored. This system area is described in [Table 10](#).

Table 10. Password system area

Block number	32-bit password number
1	Password 1
2	Password 2
3	Password 3

The dedicated password commands are:

- Write-sector Password:**

The Write-sector Password command is used to write a 32-bit block into the password system area. This command must be used to update password values. After the write cycle, the new password value is automatically activated. It is possible to modify a password value after issuing a valid Present-sector Password command. On delivery, the three default password values are set to 0000 0000h and are activated.
- Lock-sector Password:**

The Lock-sector Password command is used to set the Sector security status byte of the selected sector. Bits b₄ to b₁ of the Sector security status byte are affected by the Lock-sector Password command. The Sector Lock bit, b₀, is set to '1' automatically. After issuing a Lock-sector Password command, the protection settings of the selected

sector are activated. The protection of a locked block cannot be changed in RF mode. A Lock-sector Password command sent to a locked sector returns an error code.

- **Present-sector Password:**

The Present-sector Password command is used to present one of the three passwords to the M24LR64-R in order to modify the access rights of all the memory sectors linked to that password ([Table 8](#)) including the password itself. If the presented password is correct, the access rights remain activated until the tag is powered off or until a new Present-sector Password command is issued. If the presented password value is not correct, all the access rights of all the memory sectors are deactivated.

- **Sector security status byte area access conditions in I²C mode:**

In I²C mode, read access to the Sector security status byte area is always allowed. Write access depends on the correct presentation of the I²C password (see [I²C Present Password command description on page 27](#)).

To access the Sector security status byte area, the device select code used for any I²C command must have the E2 Chip Enable address at 1.

An I²C write access to a Sector security status byte re-initializes the RF access condition to the given memory sector.

4.2 Example of the M24LR64-R security protection

[Table 11](#) and [Table 12](#) show the sector security protections before and after a valid Present-sector Password command. [Table 11](#) shows the sector access rights of an M24LR64-R after power-up. After a valid Present-sector Password command with password 1, the memory sector access is changed as shown in [Table 12](#).

Table 11. M24LR64-R sector security protection after power-up

Sector address				Sector security status byte					
				b ₇ b ₆ b ₅	b ₄	b ₃	b ₂	b ₁	b ₀
0	Protection: Standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: Pswd 1	Read	No Write	xxx	0	1	0	0	1
2	Protection: Pswd 1	Read	Write	xxx	0	1	0	1	1
3	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	0	1
4	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	1	1