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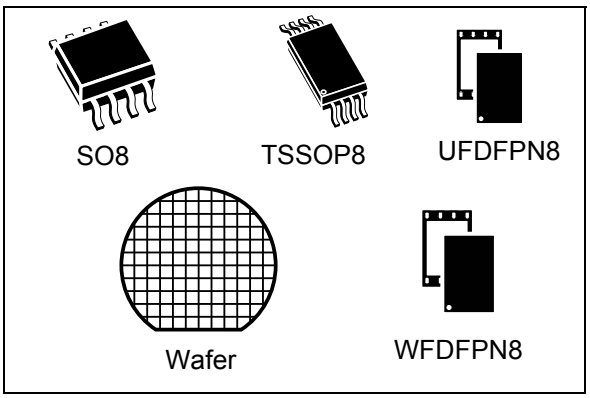
M24SR64-Y

Dynamic NFC/RFID tag IC with 64-Kbit EEPROM, NFC Forum Type 4 Tag and I²C interface

Datasheet - production data



Features

I²C interface

- Two-wire I²C serial interface supports 1 MHz protocol
- Single supply voltage: 2.7 V to 5.5 V

Contactless interface

- NFC Forum Type 4 Tag
- ISO/IEC 14443 Type A
- 106 Kbps data rate
- Internal tuning capacitance: 25 pF

Memory

- 8-Kbyte (64-kbit) EEPROM
- Support of NDEF data structure
- Data retention: 200 years
- Write cycle endurance:
  - 1 million Write cycles at 25 °C
  - 600k Write cycles at 85 °C
  - 500k Write cycles at 105 °C
- Read up to 246 bytes in a single command
- Write up to 246 bytes in a single command
- 7 bytes unique identifier (UID)
- 128 bits passwords protection

Package

- 8-lead small-outline package (SO8) ECOPACK2®
- TSSOP8 ECOPACK2®
- UFDFPN8 ECOPACK2®
- WFDFDN8 ECOPACK2®(1)(2)

Digital pad

- GPO: configurable General Purpose Output
- RF disable: activation/deactivation of RF commands

Temperature range

- From - 40 °C up to 105 °C for I²C operation
- From - 40 °C up to 85 °C for RF operation

Description

M24SR64-Y belongs to the ST25 family which includes all STMicroelectronics NFC/RFID tag and reader products.

The M24SR64-Y device is a dynamic NFC/RFID tag IC with a dual interface. It embeds an EEPROM memory. It can be operated from an I²C interface or by a 13.56 MHz RFID reader or an NFC phone.

The I²C interface uses a two-wire serial interface, consisting of a bidirectional data line and a clock line. It behaves as a slave in the I²C protocol.

The RF protocol is compatible with ISO/IEC 14443 Type A and NFC Forum Type 4 Tag.

1. Preliminary data for automotive grade (under qualification).
2. Package for automotive grade.

Contents

List of tables

List of figures

1 Functional description

The M24SR64-Y device is a dynamic NFC/RFID tag that can be accessed either from the I^2C or the RF interface. The RF and I^2C host can read or write to the same memory, that is why only one host can communicate at a time with the M24SR64-Y. The management of the interface selection is controlled by the M24SR64-Y device itself.

The RF interface is based on the ISO/IEC 14443 Type A standard. The M24SR64-Y is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

The I^2C interface uses a two-wire serial interface consisting of a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code in accordance with the I²C bus definition.

The device behaves as a slave in the I^2C protocol.

Figure 1 displays the block diagram of the M24SR64-Y device.

Figure 1. M24SR64-Y block diagram

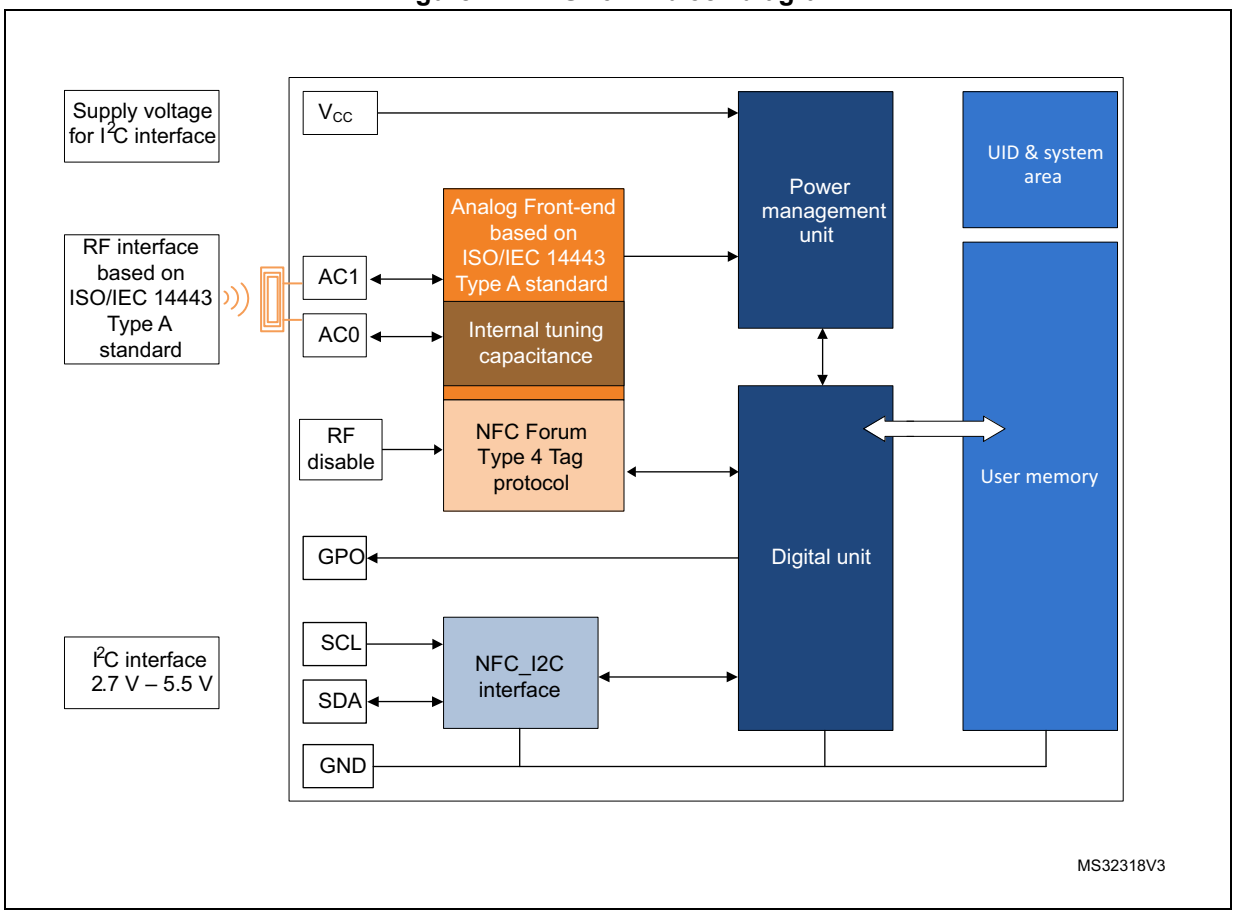
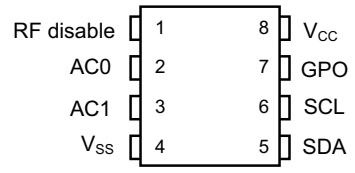


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
AC0, AC1	Antenna coils	-
V_{CC}	Supply voltage	-
VSS	Ground	-
GPO	Interrupt output (1)	Open drain output
RF disable	Disable the RF communication (2)	Input

1. An external pull-up > 4.7 kΩ is required.
2. An external pull-down is required when the voltage on V_{cc} is above its POR level.

Figure 2. 8-pin package connections



MS30744V2

1. See Package mechanical data section for package dimensions, and how to identify pin 1.

1.1 Functional modes

The M24SR64-Y has two functional modes available. The difference between the modes lies in the power supply source (see *Table 2*).

Table 2. Functional modes

Modes	Supply source	Comments
I^2C mode	V_{cc}	The I^2C interface is available
Tag mode	RF field only	The I^2C interface is disconnected
Dual interface mode	RF field or V_{cc}	Both I^2C and RF interfaces are available

1.1.1 I^2C mode

M24SR64-Y is powered by V_{CC}. The I^2C interface is connected to the M24SR64-Y. The I^2C host can communicate with the M24SR64-Y device.

1.1.2 Tag mode

The M24SR64-Y is supplied by the RF field and can communicate with an RF host (RFID reader or an NFC phone). The User memory can only be accessed by the RF commands.

1.1.3 Dual interface mode

Both interfaces, RF and I^2C, are connected to the M24SR64-Y and both RF or I^2C host can communicate with the M24SR64-Y device. The power supply and the access management are carried out by the M24SR64-Y itself. For further details, please refer to the token mechanism chapter.

2 Signal descriptions

2.1 Serial clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial clock (SCL) to V_{CC}. (*Figure 17* indicates how the value of the pull-up resistor can be calculated).

In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

2.2 Serial data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial data (SDA) to V_{CC}. (*Figure 17* indicates how the value of the pull-up resistor can be calculated).

2.3 Antenna coil (AC0, AC1)

These inputs are used to connect the device to an external coil exclusively. It is advised not to connect any other DC or AC path to AC0 or AC1.

When correctly tuned, the coil is used to access the device using NFC Forum Type 4 commands.

2.4 Ground (V_{SS})

V_{SS}, when connected, is the reference for the V_{CC} supply voltage for all pads, even AC0 and AC1.

2.5 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the M24SR64-Y.

2.5.1 Operating supply voltage V_{CC}

Prior to selecting the M24SR64-Y and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied. To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with suitable capacitors (usually of the order of 10 nF and 100 pF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a writing instruction (UpdateBinary, ChangeReferenceData,

EnableVerificationRequirement, DisableVerificationRequirement, EnablePermanentState, DisablePermanentState, until the completion of the internal I²C write cycle (t_W).

2.5.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

2.5.3 Device reset in I²C mode

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the M24SR64-Y does not respond to any I²C instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby power mode. However, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the M24SR64-Y stops responding to any instruction sent to it.

2.5.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the M24SR64-Y must be in Standby power mode (mode reached after decoding a Stop condition, assuming that there is no internal operation in progress).

2.6 RF disable

This input signal is used to disable the RF communication. When the voltage on the V_{CC} pin is below the POR level or not connected, an internal pull-down resistor is connected on this pad. Thus, the RF disable pad is maintained to the low level and the RF analog front end is activated. When the voltage on the V_{CC} pin is higher than the POR level, the I²C host shall set this pin to enable or disable the RF communication. In Dual interface mode, RF disable must not be left floating.

2.7 General purpose output (GPO)

The GPO pad is an open drain pad and a external pull-up resistor shall be connected to it. This pad is a configurable output signal. On delivery, GPO is configured as Session opened. Its behavior is consistent with the I^2C or RF session activated and with the mode chosen by the user. The GPO pad is enable when an RF or an I^2C session is open. When neither an RF nor an I^2C session is open, the GPO is high impedance.

The user can select one of these configurations(1):

- SessionOpen: an RF or I²C session is ongoing.
- MIP (NDEF Message updating In Progress): the RF host is writing an NDEF length different from 0x0000. This mode can be used to detect when the RF host changes the NDEF message as defined by the NFC Forum.
- WIP (Writing In Progress): the M24SR64-Y is executing a writing operation.
- INT (interrupt): the I²C or RF host can force the M24SR64-Y to send a negative pulse on the GPO pin.
- I²C ready response: an I²C response is ready to be read by the I²C host.
- State mode: the I²C or RF host can control the state of the GPO pad during the RF session.
- RF busy: an RF host is communicating with the M24SR64-Y.

2.7.1 Session Open configuration (GPO field = 0xX1 or 0x1X)

When the GPO is configured as "Session Open", it goes to the Low state when an RF or I²C session is ongoing (see *Figure 3*).

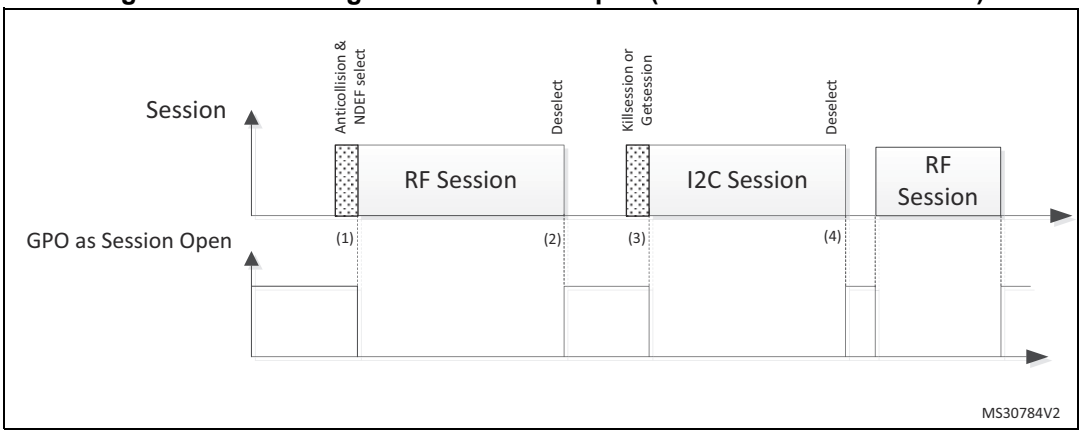
An RF session is taken when M24SR64-Y receives a valid Select Application. The session is released after M24SR64-Y has received a valid Deselect command, if M24SR64-Y has received a Kill RF session command in I²C or when the RF field became OFF.

An I²C session is taken when M24SR64-Y receives a valid Get session command or a valid Kill RF session command. The session is released after M24SR64-Y has received I²C token release sequence or after a Power Off.

GPO is driven low after a delay (1) or (3) when the session is open.

GPO is released after a delay (2) or (4) when the session is released.

Figure 3. GPO configured as Session Open (GPO field = 0xX1 or 0x1X)



1. CmdEOFtoGPlow (RF command End of frame to GPORF Session pad low)
2. CmdEOFtoGPHZ (RF command End of frame to GPORF Session pad HZ)
3. CmdSTPtoGPlow (I2C command stop to GPO low)
4. AnswerlbLBtoGPHZ (I2C answer last bit of last byte to GPO HZ)

1. See *Table 81* for more details.

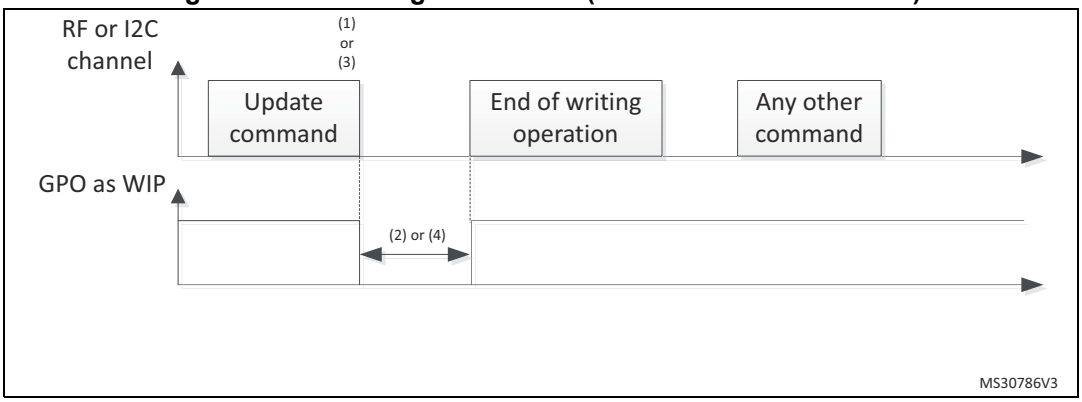
2.7.2 WIP Writing in Progress configuration (GPO field = 0xX2 or 0x2X)

When the GPO is configured as "WIP", it goes to the Low state during an I^2C or RF writing operation.

During an RF or I^2C session, when M24SR64-Y updates a file, GPO is driven low after a delay (1) or (3) following the beginning of the correspondent UpdateBinary command execution.

GPO will remain low during the writing time (2) or (4), before being released.

Figure 4. GPO configured as WIP (GPO field = 0xX2 or 0x2X)



1. CmdSTPtoGPlow (I2C Command Stop to GPO low)
2. Writing time duration
3. CmdEOFtoGPlow (RF Command End of frame to GPO low)
4. Writing time duration

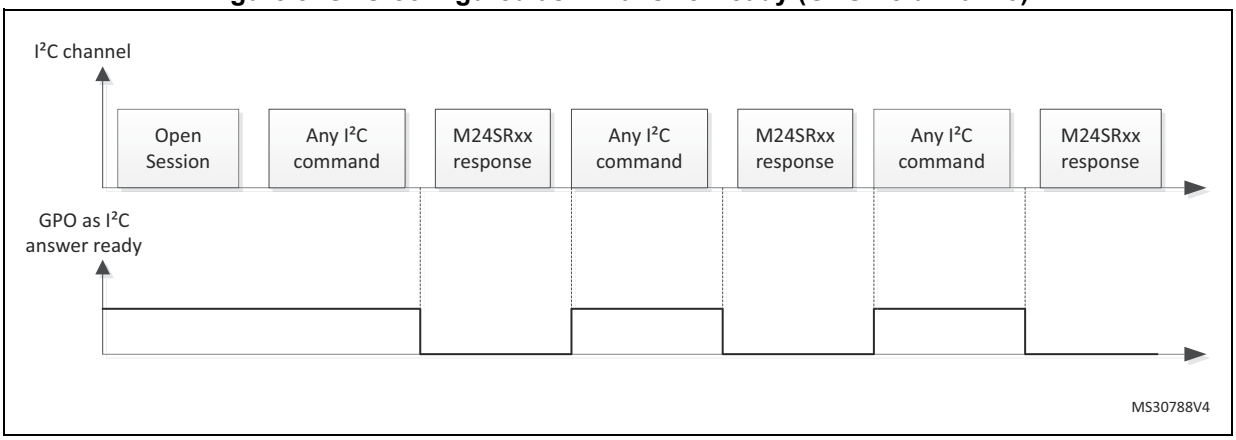
2.7.3 I²C answer ready configuration (GPO field = 0xX3)

When the GPO is configured as I²C answer ready, it goes to the Low state when the M24SR64-Y has finished to treat the I²C command and is ready to send the I²C response.

During an I²C session, after receiving a valid I²C command, GPO pin is driven low after a delay when M24SR64-Y is ready to deliver a response on the I²C bus.

GPO is released when M24SR64-Y receives a new command.

Figure 5. GPO configured as I²C answer ready (GPO field = 0xX3)



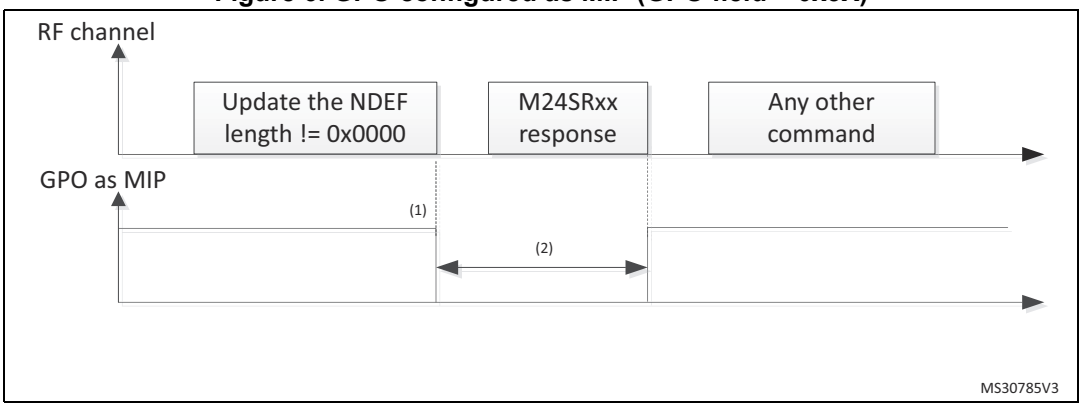
2.7.4 MIP NDEF Message writing in Progress configuration (GPO field = 0x3X)

When the GPO is configured as MIP, its state goes to the low state when the RF host writes the NDEF length to another value than 0x0000.

During an RF session, when M24SR64-Y changes an NDEF file and updates the NDEF length with a value different from 0x0000, GPO is driven low after a delay (1) following the beginning of the correspondent UpdateBinary command execution.

GPO will remain low during the writing time (2), before being released.

Figure 6. GPO configured as MIP (GPO field = 0x3X)



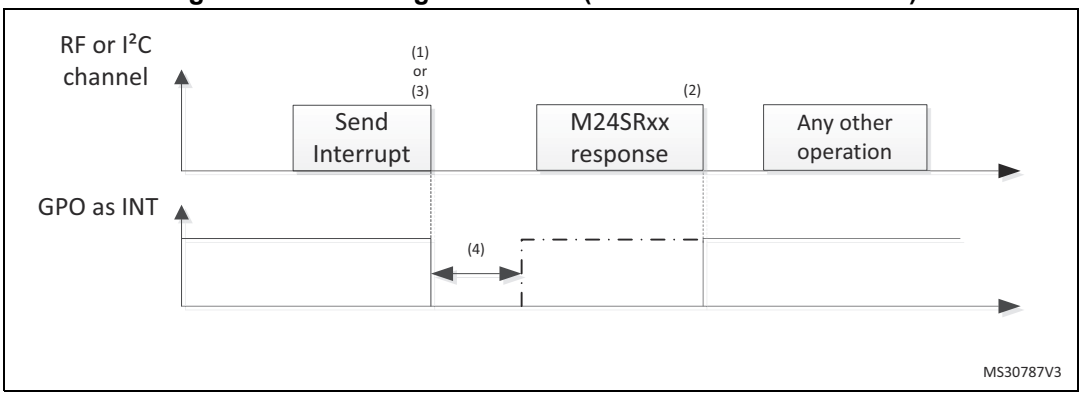
1. CmdEOFtoGPlow (RF command End of frame to GPO low)
2. Writing time duration

2.7.5 INT Interrupt configuration (GPO field = 0xX4 or 0x4X)

The I^2C or RF host can send a negative pulse on the GPO pad. The GPO pad goes to the low state at the end of the command and goes to the high state at the end of the M24SR64-Y response.

During an RF or I^2C session, when M24SR64-Y receives a valid Interrupt command, M24SR64-Y GPO pin is driven low after (1) or (3) for a duration of (4) in RF, or after responding in I2C (2). Then GPO pin is released.

Figure 7. GPO configured as INT (GPO field = 0xX4 or 0x4X)



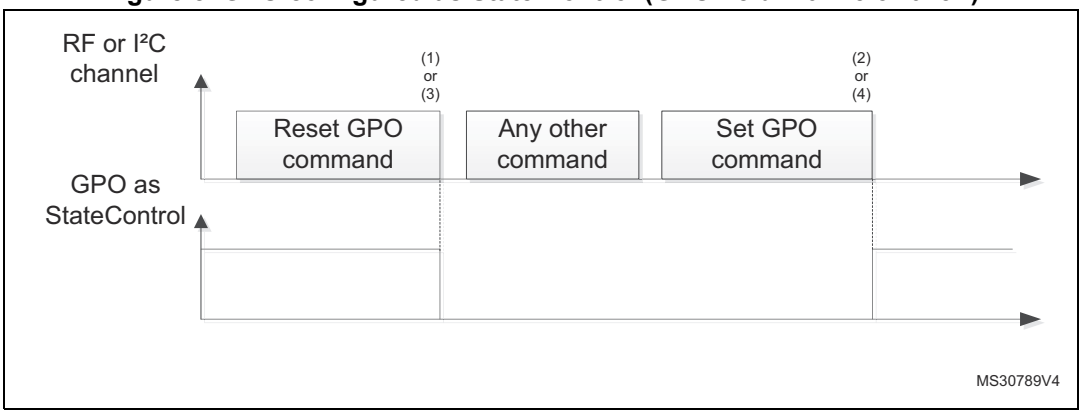
1. CmdSTPtoGPlow (I2C command Stop to GPO low)
2. After NewCmdlbFB (new I2C command last bit of first byte)
   or
   after AnswerlbFB (I2C answer last bit of first byte)
3. CmdEOFtoGPlow (RF command End of frame to GPO low)
4. GPO pulse duration

2.7.6 State Control configuration (GPO field = 0xX5 or 0x5X)

When the GPO is configured as State Control, the I^2C or RF host can control the state of the GPO by sending a dedicated command.

During an RF or I^2C session, the M24SR64-Y can control the GPO pin. After receiving a valid Set GPO command, GPO pin is driven low after a delay (1) or (3). GPO will be released after a valid Reset command or after a Power off or upon closing the RF session.

Figure 8. GPO configured as State Control (GPO field = 0xX5 or 0x5X)



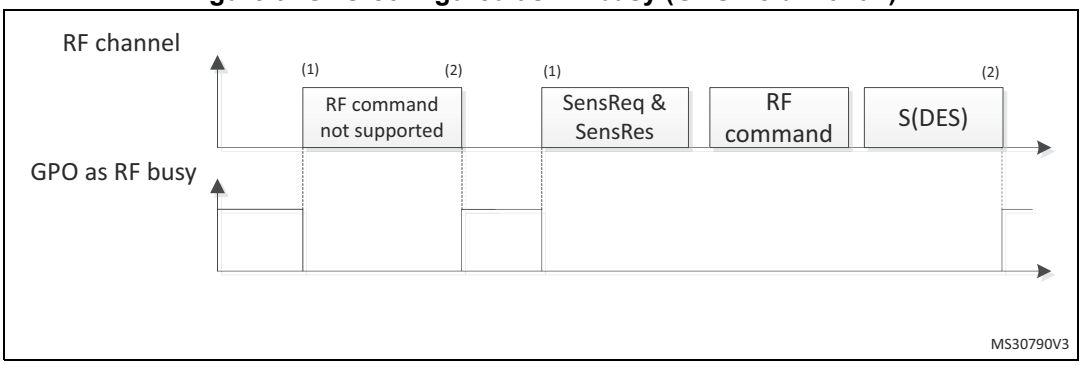
1. CmdSTPtoGPlow (I2C Set GPO command Stop to GPO low)
2. CmdSTPtoGPHZ (I2C Reset GPO command Stop to GPO HZ)
3. CmdEOFtoGPlow (RF Set GPO command End of frame to GPO low)
4. CmdEOFtoGPHZ (RF Reset GPO command End of frame to GPO HZ)

2.7.7 RF busy configuration (GPO field = 0x6X)

When the GPO is configured as RF busy, the GPO goes to the low state when the M24SR64-Y is processing an RF command or when an RFsession is ongoing.

When an RF field is present, GPO is driven low after a delay (1) when M24SR64-Y detects the first command. If the RF session is ongoing and M24SR64-Y receives a not-supported command, GPO remains low. It will be released only at the end of the RF session, after (2).

Figure 9. GPO configured as RF busy (GPO field = 0x6X)



1. CmdSOFtoGPlow (RF command Start of frame to GPO low)
2. CmdEOFtoGPHZ (RF command End of frame to GPO HZ)

3 M24SR64-Y memory management

3.1 Memory structure

The M24SR64-Y supports the NDEF Tag Application as defined in the NFC Forum Type 4 Tag. The M24SR64-Y is composed of three files:

- One Capability Container file
- One NDEF file
- One System file: this is an ST-proprietary file

The System file contains some information on the configuration of the M24SR64-Y device. The CC file gives some information about the M24SR64-Y itself and the NDEF file. The NDEF file contains the User data.

3.1.1 File identifier

The file identifier is the value used in the Select command to select a file.

Table 3. File identifier

File identifier	Meaning
0xE101	System file
0xE103	CC file
0x0001	NDEF file

3.1.2 CC file layout

The CC file gives some information about the M24SR64-Y and the NDEF file. This file is a read-only file for the RF or I²C host and cannot be modified by issuing a write command.

The T field, Read Access and Write Access fields can be changed by the RF or I²C host by issuing a specific process (refer to *Section 8: Functional procedures*).

Table 4. CC file layout for 1 NDEF file

File offset	Meaning	Value	Comments
0x0000	Number of bytes of CC file	0x000F	15 bytes
0x0002	Mapping version(1)	0x20 or 0x10	V 2.0 or V 1.0
0x0003	Maximum number of bytes that can be read	0x00F6	246 bytes
0x0005	Maximum number of bytes that can be written	0x00F6	246 bytes
0x0007	NDEF file control TLV	0x04 (2)	T field
0x0008		0x06	L field
0x0009		0x0001	FileID
0x000B		0x2000	Maximum NDEF file size
0x000D		0x00 (2)	Read access
0x000E		0x00 (2)	Write access

1. According to the reader.
2. Delivery state.

3.1.3 NDEF file layout

The NDEF file contains the NDEF message which contains the User data. The RF host or the I²C host can read and write data inside the file. The first two bytes named NDEF Message Length define the size of the NDEF message. The NDEF Message Length shall be managed by the application and the M24SR64-Y device does not check if its value is relevant vs the data written by the RF or I²C host. The M24SR64-Y device uses the NDEF Message Length, e. g. the standard read can be processed only inside the NDEF message; otherwise, the M24SR64-Y device returns an error code. For more details about the read command, refer to *Section 5.6.7: ReadBinary command*.

Table 5. NDEF file layout

File offset	Byte 0	Byte 1	Byte 2	Byte 3
0x0000	NDEF message length		User data	User data
0x0004	User data	User data	User data	User data
...	...	...	...	...
...	...	...	...	...
...	...	...	...	...
0x1FFC	...	...	...	User data

3.1.4 System file layout

The system file specifies the configuration of the M24SR64-Y. *Table 6* lists the different fields.

Table 6. Field list

File offset	Field name	Number of bytes	Read access	Write access	Delivery state (1)
0x0000	Length system file	2	I²C or RF	-	0x0012
0x0002	I²C protect	1	I²C or RF	I²C (2)	0x01
0x0003	I²C watchdog	1	I²C or RF	I²C (2)	0x00
0x0004	GPO	1	I²C or RF	I²C (2)	0x11
0x0005	ST reserved	1	I²C or RF	I²C (2)	0x00
0x0006	RF enable	1	I²C or RF	I²C (2)	0x xxxx xxx1(3)
0x0007	NDEF File number (RFU)	1	I²C or RF	none	0x00
0x0008	UID	7	I²C or RF	none	0x0284 xx xx xx xx xx or 0x028C xx xx xx xx xx(4) (5)
0x000F	Memory Size	2	I²C or RF	none	0x1FFF
0x0011	Product Code	1	I²C or RF	none	0x84 or 0x8C(5)

1. The delivery state for all passwords = 0x00000000000000000000000000000000.
2. The access is granted when the field I²C protect is set to the state Unprotected or when the right I²C password was correctly received (see *Section 3.5: I2C password*).
3. Refer *Table 11*.
4. x values are defined by ST to insure UID unicity.
5. Automotive grade

Table 7. Details about I2C watchdog

File offset	b7- b0
0x0003	The "I^2C Watchdog" ensures the I2C host will not keep the session open, while there is no more activity on the I^2C bus (between the stop bit of the previous transaction and the start bit of the next one) – 0x00 (default value): the Watchdog is off – Other values: If programmed to a non null value N, the Watchdog is enabled and counts N*30 ms (30 ms is approximate) before releasing the I^2C session.

Table 8. Details about the GPO field

File offset	b7	b6-b4	b3	b2-b0
0x0004				
RFU				
When an RF session is open: 0b000: High impedance 0b001: Session opened 0b010: WIP 0b011: MIP 0b100: Interrupt 0b101: State Control 0b110: RF Busy 0b111: RFU				
RFU				
When an I²C session is open: 0b000: High impedance 0b001: Session opened 0b010: WIP 0b011: I²C Answer Ready 0b100: Interrupt 0b101: State Control 0b110: RFU 0b111: RFU				

Table 9. Details about the RF Session field

File offset	b7	b6-b4	b3-b0
0x0004			
RFU			
When an RF session is open: 0b001: Session opened			
RFU			

Table 10 gives some details about the ST reserved field.

Table 10. Details about the ST reserved field

File offset	b7-b0
0x0005	
0x00	

Table 11 gives some details about the RF enable field.

Table 11. Details about the RF enable field

File offset	b7	b6-b4	b3	b2-b1	b0
0x0006					
0: the RF field is off (1) 1: the RF field is on (1)					
RFU					
0: the RF disable pad is at low state (1) 1: the RF disable pad is at high state (1)					
RFU					
0: the M24SR64-Y does not decode the command received from the RF interface 1: the M24SR64-Y decodes the command received from the RF interface					

1. this field is written by the M24SR64-Y.

3.2 Read and write access rights to the memory

An NDEF file can be locked for read or write accesses. It is also protected by a 128-bit password that the host shall present before accessing the NDEF file. There are two 128-bit passwords, one for the read access and the other one for the write access.

An NDEF file can be permanently locked for read or write accesses. Thus, the host cannot access the NDEF file.

The read password shall be sent to the M24SR64-Y device before reading a read-locked NDEF file.

The write password shall be present on the M24SR64-Y device before writing a write-locked NDEF file. The write password shall be sent to change the read or write access. The read or write access right is defined for the NDEF file.

3.2.1 State of the Read and Write access rights

Two bytes in the CC file are used to define the Read and Write access rights to the NDEF file. For more details, refer to *Section 3.1.2: CC file layout*.