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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# M25P10A 1Mb 3V Serial Flash Embedded Memory

## Features

- SPI bus-compatible serial interface
- 1Mb Flash memory
- 50 MHz clock frequency (maximum)
- 2.3V to 3.6V single supply voltage
- Page program (up to 256 bytes) in 1.4ms (TYP)
- Erase capability
  - Sector erase: 256Kb in 0.65s (TYP)
  - Bulk erase: 1Mb in 1.7s (TYP)
- Deep power-down: 1μA (TYP)
- Electronic signature
  - JEDEC-standard 2-byte signature (2011h)
  - RES command, 1-byte signature (10h) for backward compatibility
- More than 20 years data retention
- Automotive-certified parts available
- Packages (RoHS-compliant)
  - SO8N (MN) 150 mils
  - VFQFPN8 (MP) MLP8 6mm x 5mm
  - UDFDN8 (MB) 2mm x 3mm

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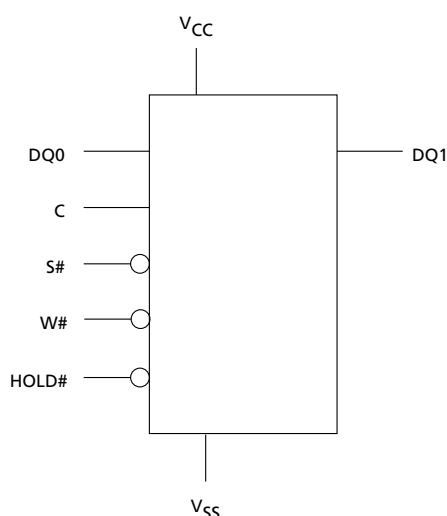
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## Functional Description

The M25P10A is a 1Mb (125Kb x 8) serial Flash memory device with advanced write protection mechanisms accessed by a high-speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time using the PAGE PROGRAM command. It is organized as 4 sectors, each containing 128 pages. Each page is 256 bytes wide. Memory can be viewed either as 512 pages or as 131,072 bytes. The entire memory can be erased using the BULK ERASE command, or it can be erased one sector at a time using the SECTOR ERASE command.

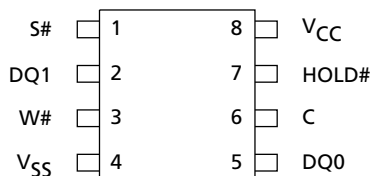
**Figure 1: Logic Diagram**



**Table 1: Signal Names**

| Signal Name     | Function           | Direction |
|-----------------|--------------------|-----------|
| C               | Serial clock       | Input     |
| DQ0             | Serial data input  | Input     |
| DQ1             | Serial data output | Output    |
| S#              | Chip select        | Input     |
| W#              | Write protect      | Input     |
| HOLD#           | Hold               | Input     |
| V <sub>CC</sub> | Supply voltage     | —         |
| V <sub>SS</sub> | Ground             | —         |

**Figure 2: Pin Connections: SO8, VFQFPN, and UFDFPN8**



Note: 1. There is an exposed central pad on the underside of the MLP8 package that is pulled internally to V<sub>SS</sub>, and must not be connected to any other voltage or signal line on the PCB. The Package Mechanical section provides information on package dimensions and how to identify pin 1.

## Signal Descriptions

**Table 2: Signal Descriptions**

| Signal          | Type   | Description   |
|-----------------|--------|---|
| DQ1             | Output | <b>Serial data:</b> The DQ1 output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock (C).   |
| DQ0             | Input  | <b>Serial data:</b> The DQ0 input signal is used to transfer data serially into the device. It receives commands, addresses, and the data to be programmed. Values are latched on the rising edge of the serial clock (C).  |
| C               | Input  | <b>Clock:</b> The C input signal provides the timing of the serial interface. Commands, addresses, or data present at serial data input (DQ0) is latched on the rising edge of the serial clock (C). Data on DQ1 changes after the falling edge of C.   |
| S#              | Input  | <b>Chip select:</b> When the S# input signal is HIGH, the device is deselected and DQ1 is at HIGH impedance. Unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress, the device will be in the standby power mode (not the DEEP POWER-DOWN mode). Driving S# LOW enables the device, placing it in the active power mode. After power-up, a falling edge on S# is required prior to the start of any command. |
| HOLD#           | Input  | <b>Hold:</b> The HOLD# signal is used to pause any serial communications with the device without deselecting the device. During the hold condition, DQ1 is High-Z. DQ0 and C are "Don't Care." To start the hold condition, the device must be selected, with S# driven LOW.  |
| W#              | Input  | <b>Write protect:</b> The W# input signal is used to freeze the size of the area of memory that is protected against program or erase commands as specified by the values in BP1, and BP0 bits of the Status Register.  |
| V <sub>CC</sub> | Power  | <b>Device core power supply:</b> Source voltage.  |
| V <sub>SS</sub> | Ground | <b>Ground:</b> Reference for the V <sub>CC</sub> supply voltage.  |



## SPI Modes

These devices can be driven by a microcontroller with its serial peripheral interface (SPI) running in either of the following two SPI modes:

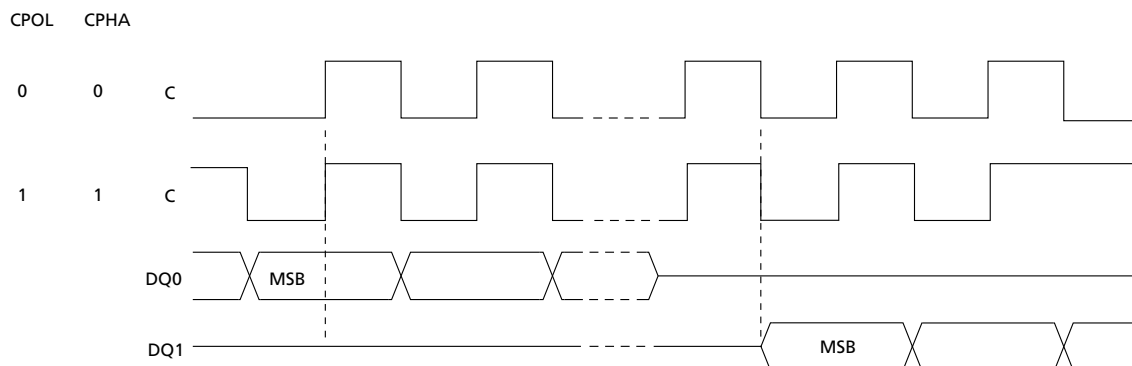
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of serial clock (C), and output data is available from the falling edge of C.

The difference between the two modes is the clock polarity when the bus master is in STANDBY mode and not transferring data:

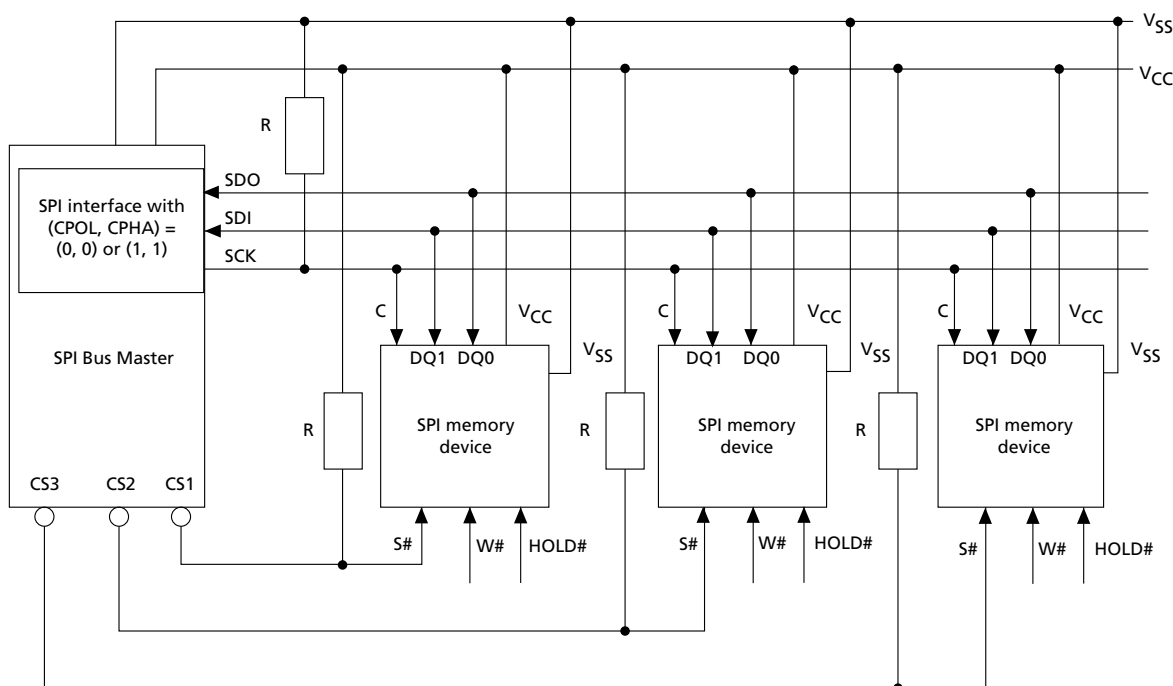
- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

**Figure 3: SPI Modes Supported**



Because only one device is selected at a time, only one device drives the serial data output (DQ1) line at a time, while the other devices are HIGH-Z. An example of three devices connected to an MCU on an SPI bus is shown here.

**Figure 4: Bus Master and Memory Devices on the SPI Bus**



- Notes:
1. WRITE PROTECT (W#) and HOLD# should be driven HIGH or LOW as appropriate.
  2. Resistors (R) ensure that the memory device is not selected if the bus master leaves the S# line HIGH-Z.
  3. The bus master may enter a state where all I/O are HIGH-Z at the same time; for example, when the bus master is reset. Therefore, C must be connected to an external pull-down resistor so that when all I/O are HIGH-Z, S# is pulled HIGH while C is pulled LOW. This ensures that S# and C do not go HIGH at the same time and that the  $t_{SHCH}$  requirement is met.
  4. The typical value of R is 100 k $\Omega$ , assuming that the time constant  $R \times C_p$  ( $C_p$  = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus HIGH-Z.
  5. Example: Given that  $C_p = 50$  pF ( $R \times C_p = 5\mu s$ ), the application must ensure that the bus master never leaves the SPI bus HIGH-Z for a time period shorter than 5 $\mu s$ .

## Operating Features

### Page Programming

To program one data byte, two commands are required: WRITE ENABLE, which is one byte, and a PAGE PROGRAM sequence, which is four bytes plus data. This is followed by the internal PROGRAM cycle of duration  $t_{PP}$ . To spread this overhead, the PAGE PROGRAM command allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided they lie in consecutive addresses on the same page of memory. To optimize timings, it is recommended to use the PAGE PROGRAM command to program all consecutive targeted bytes in a single sequence than to use several PAGE PROGRAM sequences with each containing only a few bytes.

### Sector Erase, Bulk Erase

The PAGE PROGRAM command allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time using the SECTOR ERASE command, or throughout the entire memory using the BULK ERASE command. This starts an internal ERASE cycle of duration  $t_{SE}$  or  $t_{BE}$ . The ERASE command must be preceded by a WRITE ENABLE command.

### Polling during a Write, Program, or Erase Cycle

An improvement in the time to complete the following commands can be achieved by not waiting for the worst case delay ( $t_W$ ,  $t_{PP}$ ,  $t_{SE}$ , or  $t_{BE}$ ).

- WRITE STATUS REGISTER
- PROGRAM
- ERASE (SECTOR ERASE, BULK ERASE)

The write in progress (WIP) bit is provided in the status register so that the application program can monitor this bit in the status register, polling it to establish when the previous WRITE cycle, PROGRAM cycle, or ERASE cycle is complete.

### Active Power, Standby Power, and Deep Power-Down

When chip select ( $S\#$ ) is LOW, the device is selected, and in the ACTIVE POWER mode. When  $S\#$  is HIGH, the device is deselected, but could remain in the ACTIVE POWER mode until all internal cycles have completed (PROGRAM, ERASE, WRITE STATUS REGISTER). The device then goes in to the STANDBY POWER mode. The device consumption drops to  $I_{CC1}$ .

The DEEP POWER-DOWN mode is entered when the DEEP POWER-DOWN command is executed. The device consumption drops further to  $I_{CC2}$ . The device remains in this mode until the RELEASE FROM DEEP POWER-DOWN command is executed. While in the DEEP POWER-DOWN mode, the device ignores all WRITE, PROGRAM, and ERASE commands. This provides an extra software protection mechanism when the device is not in active use, by protecting the device from inadvertent WRITE, PROGRAM, or ERASE operations. For further information, see the DEEP POWER DOWN command.

## Status Register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific commands. For a detailed description of the status register bits, see READ STATUS REGISTER (page 20).

## Data Protection by Protocol

Non-volatile memory is used in environments that can include excessive noise. The following capabilities help protect data in these noisy environments.

Power on reset and an internal timer ( $t_{PUW}$ ) can provide protection against inadvertent changes while the power supply is outside the operating specification.

PROGRAM, ERASE, and WRITE STATUS REGISTER commands are checked before they are accepted for execution to ensure they consist of a number of clock pulses that is a multiple of eight.

All commands that modify data must be preceded by a WRITE ENABLE command to set the write enable latch (WEL) bit.

In addition to the low power consumption feature, the DEEP POWER-DOWN mode offers extra software protection since all PROGRAM, and ERASE commands are ignored when the device is in this mode.

## Software Data Protection

Memory can be configured as read-only using the block protect bits (BP1, BP0) as shown in the Protected Area Sizes table.

## Hardware Data Protection

Hardware data protection is implemented using the write protect signal applied on the W# pin. This freezes the status register in a read-only mode. In this mode, the block protect (BP) bits and the status register write disable bit (SRWD) are protected.

**Table 3: Protected Area Sizes**

| Status Register Content |          | Memory Content               |                               |
|-------------------------|----------|------------------------------|-------------------------------|
| BP Bit 1                | BP Bit 0 | Protected Area               | Unprotected Area              |
| 0                       | 0        | none                         | All sectors (sectors 0 to 3)  |
| 0                       | 1        | Upper 4th (sector 3)         | Lower 3/4ths (sectors 0 to 2) |
| 1                       | 0        | Upper half (sectors 2 and 3) | Lower half (sectors 0 and 1)  |
| 1                       | 1        | All sectors (sectors 0 to 3) | none                          |

Note: 1. 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP1, BP0) are 0.

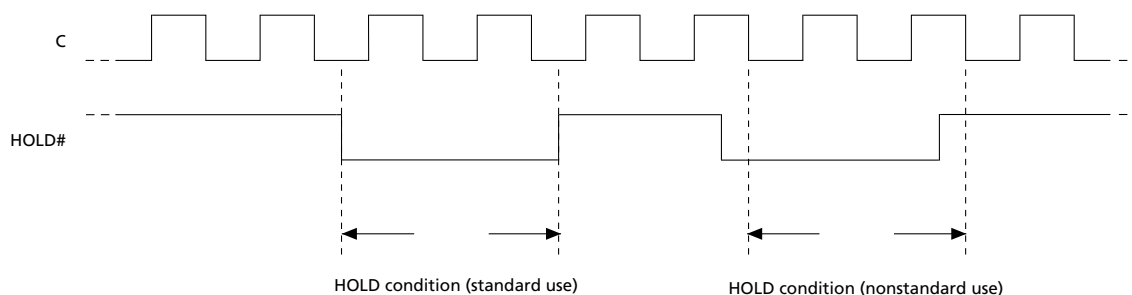
## Hold Condition

The HOLD# signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal LOW does not terminate any WRITE STATUS REGISTER, PROGRAM, or ERASE cycle that is currently in progress.

To enter the hold condition, the device must be selected, with S# LOW. The hold condition starts on the falling edge of the HOLD# signal, if this coincides with serial clock (C) being LOW. The hold condition ends on the rising edge of the HOLD# signal, if this coincides with C being LOW. If the falling edge does not coincide with C being LOW, the hold condition starts after C next goes LOW. Similarly, if the rising edge does not coincide with C being LOW, the hold condition ends after C next goes LOW.

During the hold condition, DQ1 is HIGH impedance while DQ0 and C are Don't Care. Typically, the device remains selected with S# driven LOW for the duration of the hold condition. This ensures that the state of the internal logic remains unchanged from the moment of entering the hold condition. If S# goes HIGH while the device is in the hold condition, the internal logic of the device is reset. To restart communication with the device, it is necessary to drive HOLD# HIGH, and then to drive S# LOW. This prevents the device from going back to the hold condition.

**Figure 5: Hold Condition Activation**



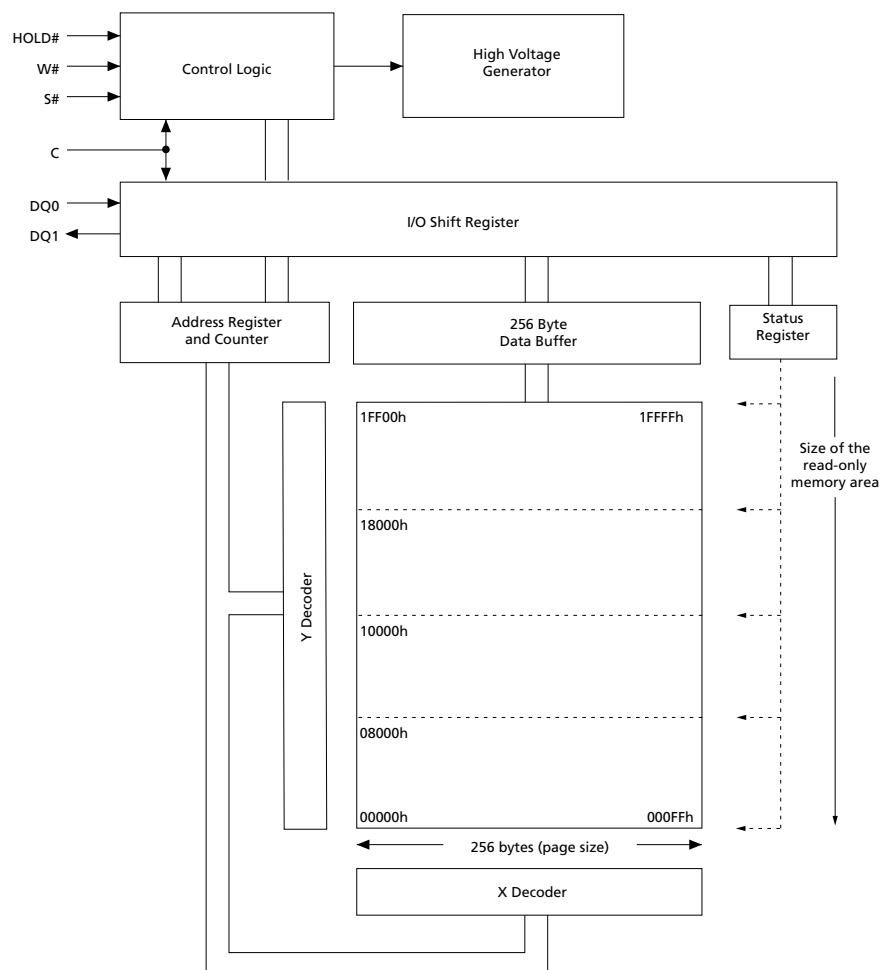
## Configuration and Memory Map

### Memory Configuration and Block Diagram

Each page of memory can be individually programmed; bits are programmed from 1 to 0. The device is sector or bulk-erasable, but not page-erasable; bits are erased from 0 to 1. The memory is configured as follows:

- 131,072 bytes (8 bits each)
- 4 sectors (256Kb, 32,768 bytes each)
- 512 pages (256 bytes each)

**Figure 6: Block Diagram**







## Memory Map – 1Mb Density

**Table 4: Sectors 3:0**

| Sector | Address Range |           |
|--------|---------------|-----------|
|        | Start         | End       |
| 3      | 0001 8000     | 0001 FFFF |
| 2      | 0001 0000     | 0001 7FFF |
| 1      | 0008 0000     | 0000 FFFF |
| 0      | 0000 0000     | 0000 7FFF |

## Command Set Overview

All commands, addresses, and data are shifted in and out of the device, most significant bit first.

Serial data input DQ0 is sampled on the first rising edge of serial clock (C) after chip select (S#) is driven LOW. Then, the one-byte command code must be shifted in to the device, most significant bit first, on DQ1, each bit being latched on the rising edges of C.

Every command sequence starts with a one-byte command code. Depending on the command, this command code might be followed by address or data bytes, by address and data bytes, or by neither address or data bytes. For the following commands, the shifted-in command sequence is followed by a data-out sequence. S# can be driven HIGH after any bit of the data-out sequence is being shifted out.

- READ DATA BYTES (READ)
- READ DATA BYTES at HIGHER SPEED
- READ STATUS REGISTER
- READ IDENTIFICATION
- RELEASE from DEEP POWER-DOWN

For the following commands, S# must be driven HIGH exactly at a byte boundary. That is, after an exact multiple of eight clock pulses following S# being driven LOW, S# must be driven HIGH. Otherwise, the command is rejected and not executed.

- PAGE PROGRAM
- SECTOR ERASE
- BULK ERASE
- WRITE STATUS REGISTER
- WRITE ENABLE
- WRITE DISABLE
- DEEP POWER-DOWN

All attempts to access the memory array are ignored during a WRITE STATUS REGISTER command cycle, a PROGRAM command cycle, or an ERASE command cycle. In addition, the internal cycle for each of these commands continues unaffected.

**Table 5: Command Set Codes**

| Command Name                    | One-Byte<br>Command Code |     | Bytes   |       |               |
|---------------------------------|--------------------------|-----|---------|-------|---------------|
|                                 |                          |     | Address | Dummy | Data          |
| WRITE ENABLE                    | 0000<br>0110             | 06h | 0       | 0     | 0             |
| WRITE DISABLE                   | 0000<br>0100             | 04h | 0       | 0     | 0             |
| READ IDENTIFICATION             | 1001<br>1111             | 9Fh | 0       | 0     | 1 to 20       |
|                                 | 1001<br>1110             | 9Eh |         |       | 1 to 20       |
| READ STATUS REGISTER            | 0000<br>0101             | 05h | 0       | 0     | 1 to $\infty$ |
| WRITE STATUS REGISTER           | 0000<br>0001             | 01h | 0       | 0     | 1             |
| READ DATA BYTES                 | 0000<br>0011             | 03h | 3       | 0     | 1 to $\infty$ |
| READ DATA BYTES at HIGHER SPEED | 0000<br>1011             | 0Bh | 3       | 1     | 1 to $\infty$ |
| PAGE PROGRAM                    | 0000<br>0010             | 02h | 3       | 0     | 1 to 256      |
| SECTOR ERASE                    | 1101<br>1000             | D8h | 3       | 0     | 0             |
| BULK ERASE                      | 1100<br>0111             | C7h | 0       | 0     | 0             |
| DEEP POWER-DOWN                 | 1011<br>1001             | B9h | 0       | 0     | 0             |
| RELEASE from DEEP POWER-DOWN    | 1010<br>1011             | ABh | 0       | 0     | 0             |

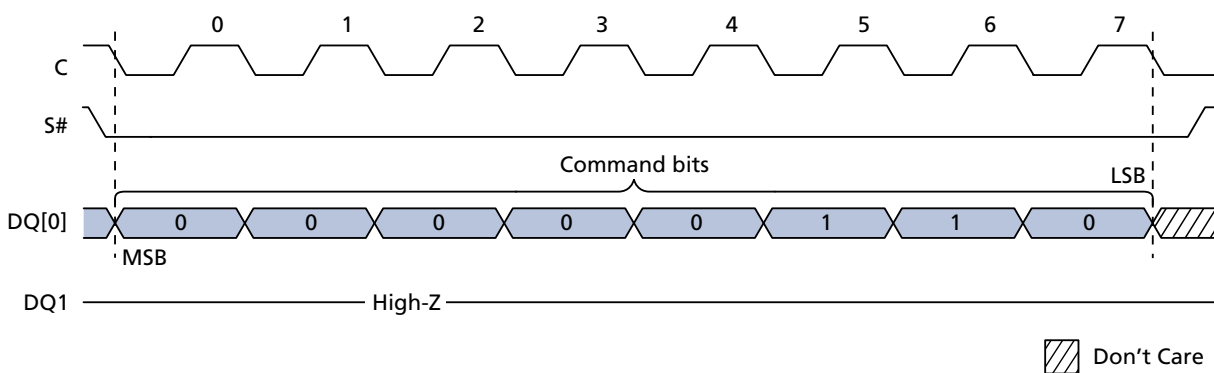
## WRITE ENABLE

The WRITE ENABLE command sets the write enable latch (WEL) bit.

The WEL bit must be set before execution of every PROGRAM, ERASE, and WRITE command.

The WRITE ENABLE command is entered by driving chip select (S#) LOW, sending the command code, and then driving S# HIGH.

**Figure 7: WRITE ENABLE Command Sequence**



## WRITE DISABLE

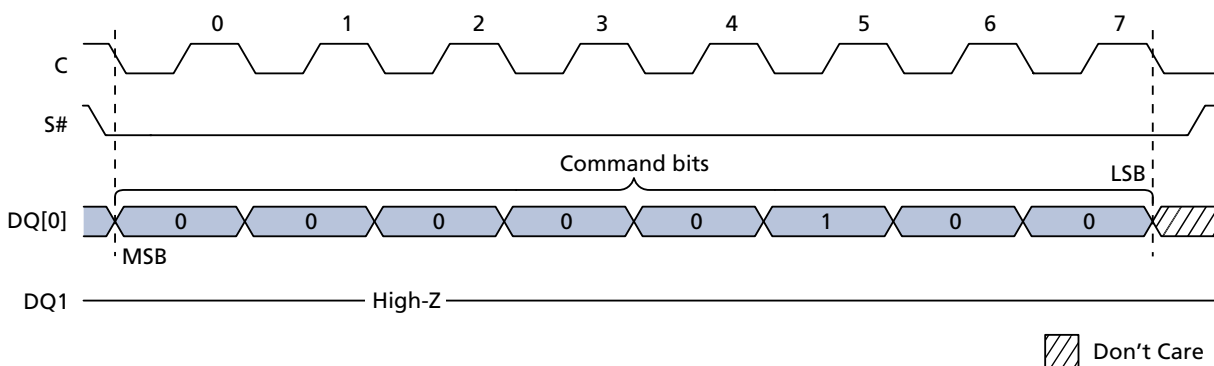
The WRITE DISABLE command resets the write enable latch (WEL) bit.

The WRITE DISABLE command is entered by driving chip select (S#) LOW, sending the command code, and then driving S# HIGH.

The WEL bit is reset under the following conditions:

- Power-up
- Completion of any ERASE operation
- Completion of any PROGRAM operation
- Completion of any WRITE REGISTER operation
- Completion of WRITE DISABLE operation

**Figure 8: WRITE DISABLE Command Sequence**



## READ IDENTIFICATION

The READ IDENTIFICATION command reads the following device identification data:

- Manufacturer identification (1 byte): This is assigned by JEDEC.
- Device identification (2 bytes): This is assigned by device manufacturer; the first byte indicates memory type and the second byte indicates device memory capacity.
- A Unique ID code (UID) (17 bytes, 16 available upon customer request): The first byte contains length of data to follow; the remaining 16 bytes contain optional Customized Factory Data (CFD) content.

**Table 6: READ IDENTIFICATION Data Out Sequence**

| Manufacturer Identification | Device Identification |                 | UID        |             |
|-----------------------------|-----------------------|-----------------|------------|-------------|
|                             | Memory Type           | Memory Capacity | CFD Length | CFD Content |
| 20h                         | 20h                   | 11h             | 10h        | 16 bytes    |

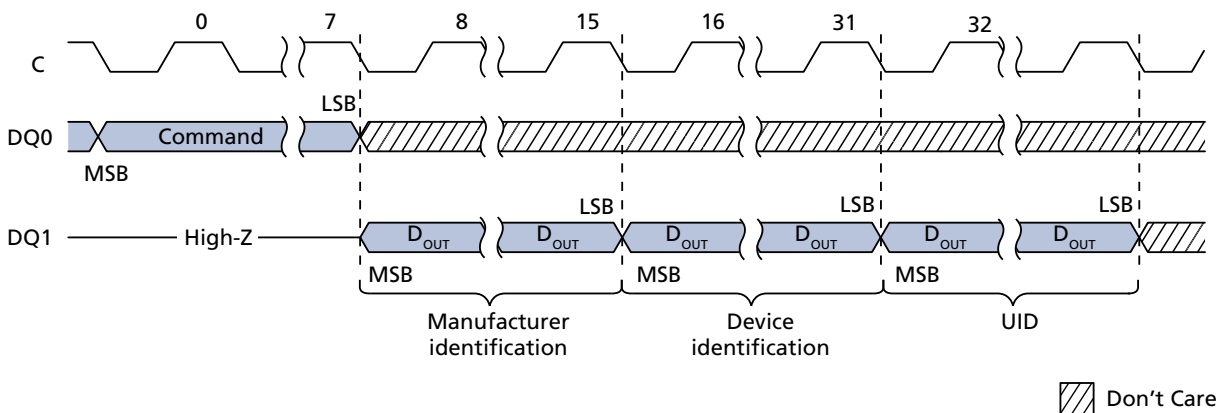
Note: 1. The CFD bytes are read-only and can be programmed with customer data upon demand. If customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero.

A READ IDENTIFICATION command is not decoded while an ERASE or PROGRAM cycle is in progress and has no effect on a cycle in progress. The READ IDENTIFICATION command must not be issued while the device is in DEEP POWER-DOWN mode.

The device is first selected by driving S# LOW. Then the 8-bit command code is shifted in and content is shifted out on DQ1 as follows: the 24-bit device identification that is stored in the memory, the 8-bit CFD length, followed by 16 bytes of CFD content. Each bit is shifted out during the falling edge of serial clock (C).

The READ IDENTIFICATION command is terminated by driving S# HIGH at any time during data output. When S# is driven HIGH, the device is put in the STANDBY POWER mode and waits to be selected so that it can receive, decode, and execute commands.

**Figure 9: READ IDENTIFICATION Command Sequence**

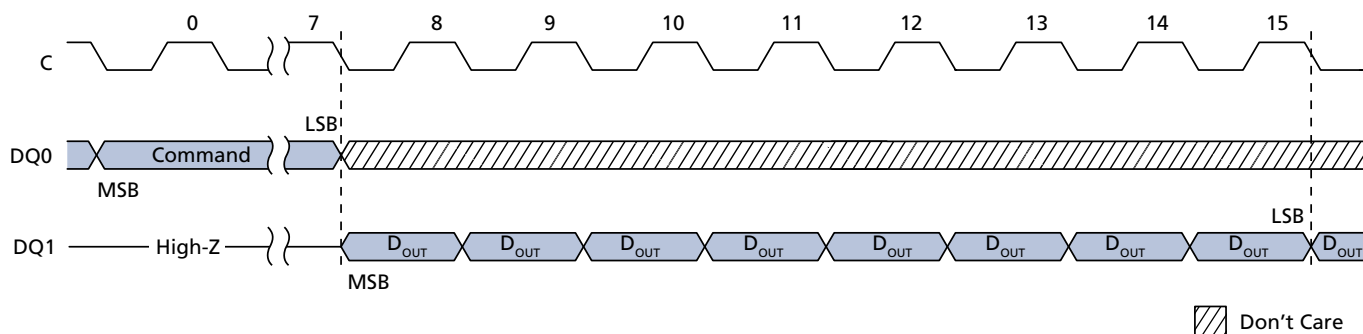




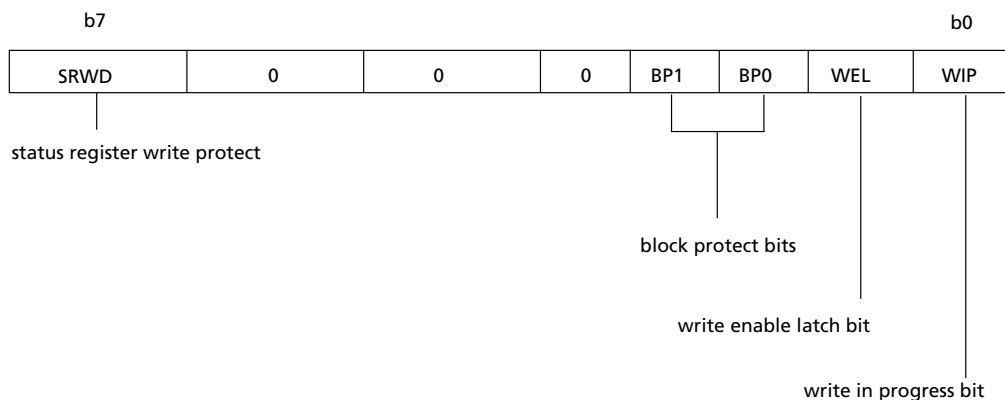
## READ STATUS REGISTER

The READ STATUS REGISTER command allows the status register to be read. The status register may be read at any time, even while a PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new command to the device. It is also possible to read the status register continuously.

**Figure 10: READ STATUS REGISTER Command Sequence**



**Figure 11: Status Register Format**



**WIP Bit**

The write in progress (WIP) bit indicates whether the memory is busy with a WRITE STATUS REGISTER cycle, a PROGRAM cycle, or an ERASE cycle. When the WIP bit is set to 1, a cycle is in progress; when the WIP bit is set to 0, a cycle is not in progress.

**WEL Bit**

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When the WEL bit is set to 1, the internal write enable latch is set; when the WEL bit is set to 0, the internal write enable latch is reset and no WRITE STATUS REGISTER, PROGRAM, or ERASE command is accepted.

**Block Protect Bits**

The block protect bits are non-volatile. They define the size of the area to be software protected against PROGRAM and ERASE commands. The block protect bits are written with the WRITE STATUS REGISTER command.

When one or more of the block protect bits is set to 1, the relevant memory area, as defined in the Protected Area Sizes table, becomes protected against PAGE PROGRAM and SECTOR ERASE commands. The block protect bits can be written provided that the HARDWARE PROTECTED mode has not been set. The BULK ERASE command is executed only if all block protect bits are 0.

**SRWD Bit**

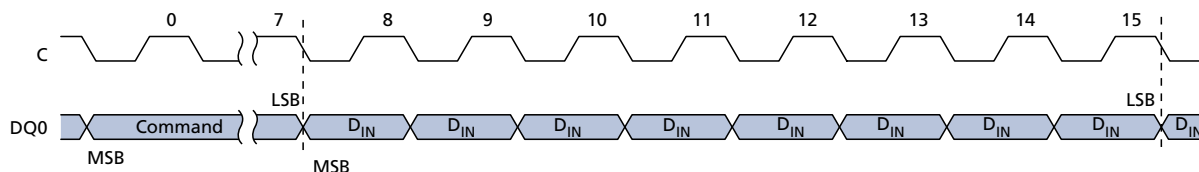
The status register write disable (SRWD) bit is operated in conjunction with the write protect (W#) signal. When the SRWD bit is set to 1 and W# is driven LOW, the device is put in the hardware protected mode. In the hardware protected mode, the non-volatile bits of the status register (SRWD, and the block protect bits) become read-only bits and the WRITE STATUS REGISTER command is no longer accepted for execution.

## WRITE STATUS REGISTER

The WRITE STATUS REGISTER command allows new values to be written to the status register. Before the WRITE STATUS REGISTER command can be accepted, a WRITE ENABLE command must have been executed previously. After the WRITE ENABLE command has been decoded and executed, the device sets the write enable latch (WEL) bit.

The WRITE STATUS REGISTER command is entered by driving chip select (S#) LOW, followed by the command code and the data byte on serial data input (DQ0). The WRITE STATUS REGISTER command has no effect on b6, b5, b4, b1, and b0 of the status register. The status register b6, b5, and b4 are always read as '0'. S# must be driven HIGH after the eighth bit of the data byte has been latched in. If not, the WRITE STATUS REGISTER command is not executed.

**Figure 12: WRITE STATUS REGISTER Command Sequence**



As soon as S# is driven HIGH, the self-timed WRITE STATUS REGISTER cycle is initiated; its duration is  $t_W$ . While the WRITE STATUS REGISTER cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit. The WIP bit is 1 during the self-timed WRITE STATUS REGISTER cycle, and is 0 when the cycle is completed. Also, when the cycle is completed, the WEL bit is reset.

The WRITE STATUS REGISTER command allows the user to change the values of the block protect bits (BP1, BP0). Setting these bit values defines the size of the area that is to be treated as read-only, as defined in the Protected Area Sizes table.

The WRITE STATUS REGISTER command also allows the user to set and reset the status register write disable (SRWD) bit in accordance with the write protect (W#) signal. The SRWD bit and the W# signal allow the device to be put in the HARDWARE PROTECTED (HPM) mode. The WRITE STATUS REGISTER command is not executed once the HPM is entered. The options for enabling the status register protection modes are summarized here.

**Table 7: Status Register Protection Modes**

| W#<br>Signal | SRWD<br>Bit | Protection<br>Mode (PM)             | Status Register<br>Write Protection | Memory Content           |                      | Notes    |
|--------------|-------------|-------------------------------------|-------------------------------------|--------------------------|----------------------|----------|
|              |             |                                     |                                     | Protected<br>Area        | Unprotected<br>Area  |          |
| 1            | 0           | SOFTWARE<br>PROTECTED mode<br>(SPM) | Software protection                 | Commands not<br>accepted | Commands<br>accepted | 1, 2, 3  |
| 0            | 0           |                                     |                                     |                          |                      |          |
| 1            | 1           |                                     |                                     |                          |                      |          |
| 0            | 1           | HARDWARE<br>PROTECTED mode<br>(HPM) | Hardware protection                 | Commands not<br>accepted | Commands<br>accepted | 3, 4, 5, |

- Notes:
1. Software protection: status register is writable (SRWD, BP1, and BP0 bit values can be changed) if the WRITE ENABLE command has set the WEL bit.
  2. PAGE PROGRAM, SECTOR ERASE, AND BULK ERASE commands are not accepted.
  3. PAGE PROGRAM and SECTOR ERASE commands can be accepted.
  4. Hardware protection: status register is not writable (SRWD, BP1, and BP0 bit values cannot be changed).
  5. PAGE PROGRAM, SECTOR ERASE, AND BULK ERASE commands are not accepted.

When the SRWD bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the WEL bit has been set previously by a WRITE ENABLE command, regardless of whether the W# signal is driven HIGH or LOW. When the status register SRWD bit is set to 1, two cases need to be considered depending on the state of the W# signal:

- If the W# signal is driven HIGH, it is possible to write to the status register provided that the WEL bit has been set previously by a WRITE ENABLE command.
- If the W# signal is driven LOW, it is not possible to write to the status register even if the WEL bit has been set previously by a WRITE ENABLE command. Therefore, attempts to write to the status register are rejected, and are not accepted for execution. The result is that all the data bytes in the memory area that have been put in SPM by the status register block protect bits (BP1, BP0) are also hardware protected against data modification.

Regardless of the order of the two events, the HPM can be entered in either of the following ways:

- Setting the status register SRWD bit after driving the W# signal LOW
- Driving the W# signal LOW after setting the status register SRWD bit.

The only way to exit the HPM is to pull the W# signal HIGH. If the W# signal is permanently tied HIGH, the HPM can never be activated. In this case, only the SPM is available, using the status register block protect bits (BP1, BP0).

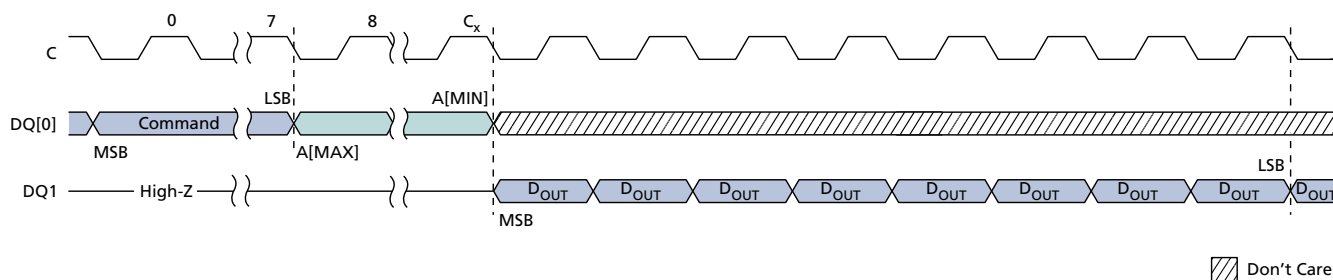
## READ DATA BYTES

The device is first selected by driving chip select (S#) LOW. The command code for READ DATA BYTES is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of serial clock (C). Then the memory contents at that address is shifted out on serial data output (DQ1), each bit being shifted out at a maximum frequency  $f_R$  during the falling edge of C.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Therefore, the entire memory can be read with a single READ DATA BYTES command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ DATA BYTES command is terminated by driving S# HIGH. S# can be driven HIGH at any time during data output. Any READ DATA BYTES command issued while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected without any effect on the cycle that is in progress.

**Figure 13: READ DATA BYTES Command Sequence**



Note: 1.  $C_x = 7 + (A[MAX] + 1)$ .

Note: 1.  $C_x = 7 + (A[\text{MAX}] + 1)$ .