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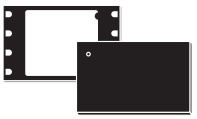
M25P64

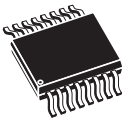
64 Mbit, low voltage, Serial Flash memory with 75 MHz SPI bus interface

Features

- 64 Mbit of Flash memory
- 2.7 V to 3.6 V single supply voltage
- SPI bus compatible serial interface
- 75 MHz clock rate (maximum)
- Page Program (up to 256 Bytes)
  - in 1.4 ms (typical)
  - in 0.35 ms (typical with V_{PP} = 9 V)
- Sector Erase (512 Kbit)
- Bulk Erase (64 Mbit)
- Electronic Signatures
  - JEDEC standard two-Byte signature (2017h)
  - RES instruction, one-Byte, signature (16h), for backward compatibility
  - Unique ID code (UID) with 16 bytes readonly: available upon customer request
- Hardware Write Protection: protected area size defined by three non-volatile bits (BP0, BP1 and BP2)
- More than 100 000 Erase/Program cycles per sector
- More than 20-year data retention
- Packages
  - RoHS compliant
- Automotive certified parts available



VDFPN8 (ME)
8 × 6 mm (MLP8)



SO16 (MF)
300 mils width

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1 Description

The M25P64 is a 64 Mbit (8M x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus instructions allowing clock frequency up to 75 MHz.(1)

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

An enhanced Fast Program/Erase mode is available to speed up operations in factory environment. The device enters this mode whenever the V_{PPH} voltage is applied to the Write Protect/Enhanced Program Supply Voltage pin ($\overline{W}/V_{PP}$).(2)

The memory is organized as 128 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 32768 pages, or 8388608 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

In order to meet environmental requirements, Numonyx offers the M25P64 in Lead-free and RoHS compliant packages.

Note: Important: This datasheet details the functionality of the M25P64 devices, based on the previous process or based on the current T9HX process (available since March 2008). The new device in T9HX is backward compatible with the old one and it includes these additional features:

- improved max frequency (Fast Read) to 75 MHz

- UID/CFD protection feature

1. 75 MHz operation is available only for process technology T9HX devices, identified by process identification digit "4" in the device marking.
2. Avoid applying VPPH to the W/VPP pin during Bulk Erase with process technology T9HX devices, identified by process identification digit "4" in the device marking.

Figure 1. Logic diagram

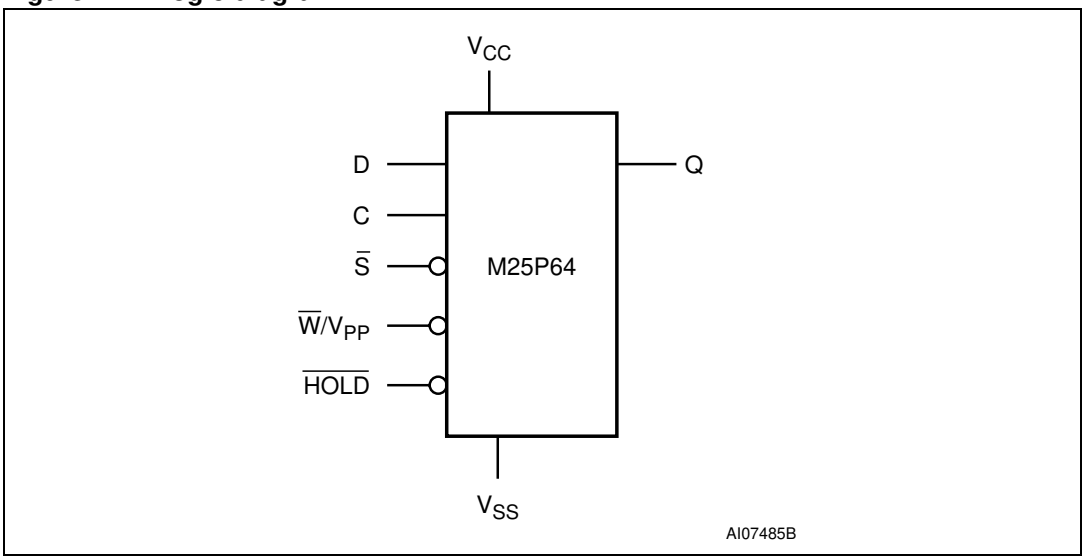
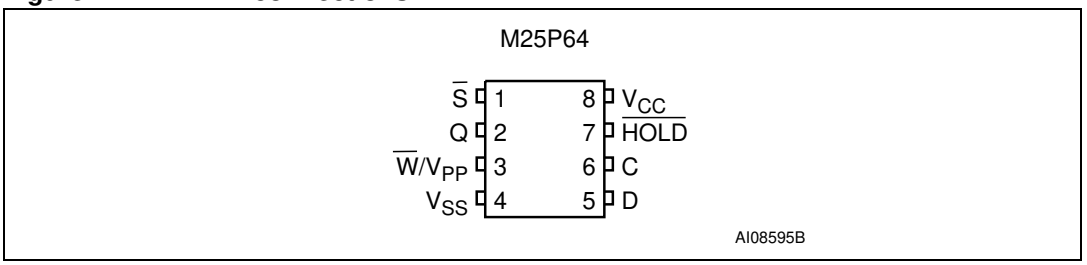


Table 1. Signal names

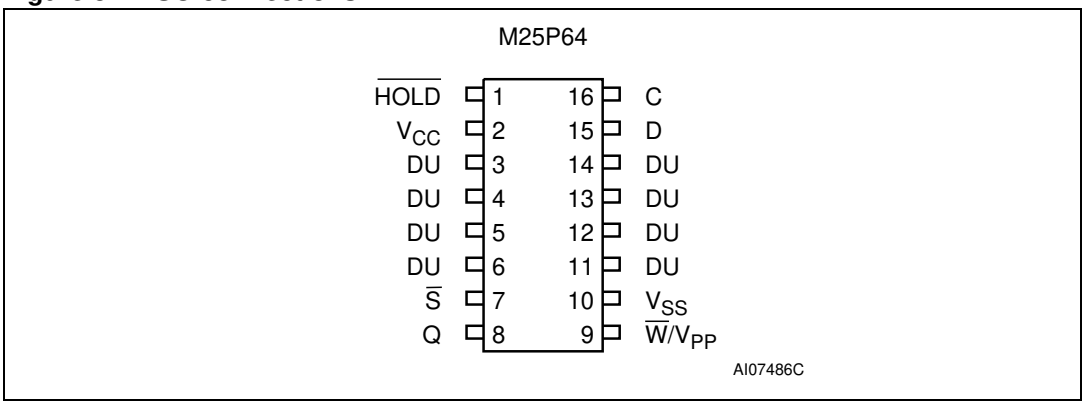
Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
S	Chip Select	Input
$\overline{W}/V_{PP}$	Write Protect/Enhanced Program Supply Voltage	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply Voltage	
V_{SS}	Ground	

Figure 2. VDFPN connections



1. There is an exposed central pad on the underside of the VDFPN package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Section 11: Package mechanical* for package dimensions, and how to identify pin-1.

Figure 3. SO connections



1. DU = Don't Use
2. See *Section 11: Package mechanical* for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write Protect/Enhanced Program supply voltage ($\overline{W}/V_{PP}$)

$\overline{W}/V_{PP}$ is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If the $\overline{W}/V_{PP}$ input is kept in a low voltage range (0V to V_{CC}) the pin is seen as a control input. This input signal is used to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).

If V_{PP} is in the range of V_{PPH} it acts as an additional power supply pin. In this case V_{PP} must be stable until the Program/Erase algorithm is completed.(1)

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

1. Avoid applying VPPH to the W/VPP pin during Bulk Erase with process technology T9HX devices, identified by process identification digit "4" in the device marking.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

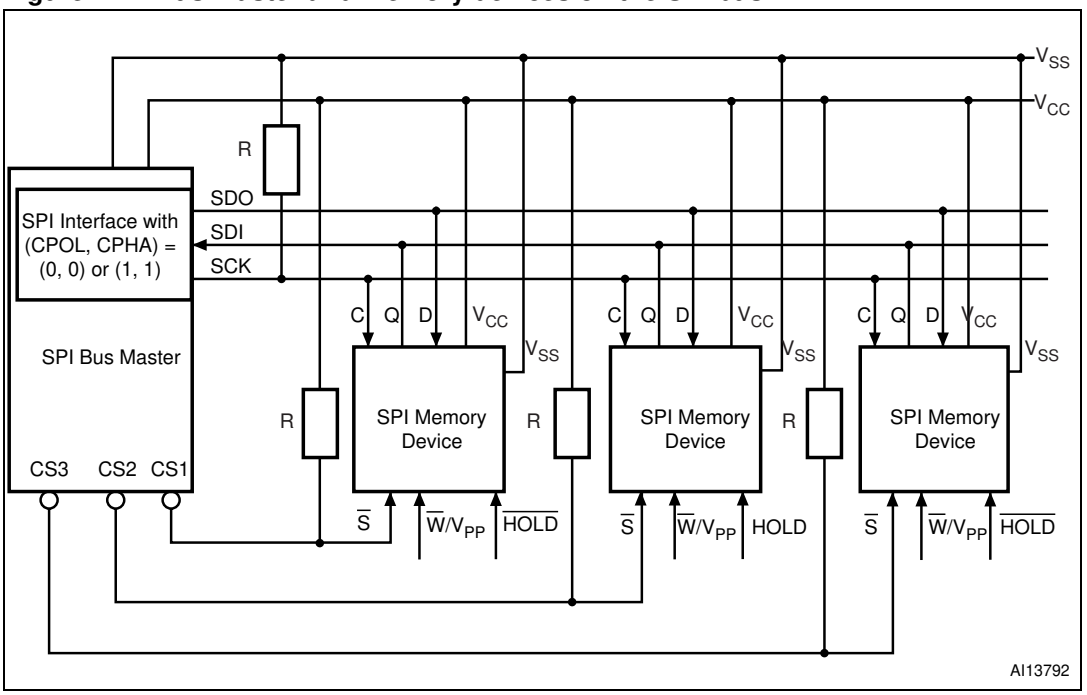
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. Bus master and memory devices on the SPI bus

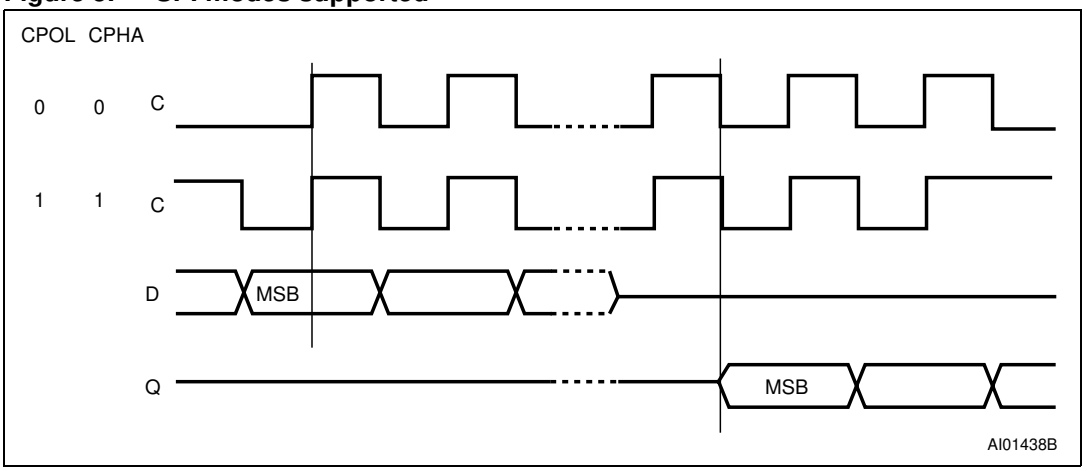


1. The Write Protect ($\overline{W}/V_{PP}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 4 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 4*) ensure that the M25P64 is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the Bus Master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$ (C_p = parasitic capacitance of the bus line) is shorter than the time during which the Bus Master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the Bus Master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 5. SPI modes supported



4 Operating features

4.1 Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted Bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few Bytes (see *Page Program (PP)* and *Table 16: AC characteristics*).

4.2 Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration t_{SE} or t_{BE}).

The Erase instruction must be preceded by a Write Enable (WREN) instruction.

4.3 Polling during a Write, Program or Erase cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

4.4 Fast Program/Erase mode

The Fast Program/Erase mode is used to speed up programming/erasing. The device enters the Fast Program/Erase mode during the Page Program, Sector Erase, or Bulk Erase(1) instruction whenever a voltage equal to V_{PPH} is applied to the $\overline{W}/V_{PP}$ pin.

The use of the Fast Program/Erase mode requires specific operating conditions in addition to the normal ones (V_{CC} must be within the normal operating range):

- the voltage applied to the $\overline{W}/V_{PP}$ pin must be equal to V_{PPH} (see *Table 10*)
- ambient temperature, T_A must be 25°C ±10°C,
- the cumulated time during which $\overline{W}/V_{PP}$ is at V_{PPH} should be less than 80 hours

1. Avoid applying VPPH to the W/VPP pin during Bulk Erase with process technology T9HX devices, identified by process identification digit "4" in the device marking.

4.5 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Standby Power mode. The device consumption drops to I_{CC1}.

4.6 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. For a detailed description of the Status Register bits, see *Section 6.4: Read Status Register (RDSR)*.

4.7 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P64 features the following data protection mechanisms:

- Power On Reset and an internal timer (t_{PUW}) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}/V_{PP}$) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).

Table 2. Protected area sizes

Status Register content			Memory content	
BP2 Bit	BP1 Bit	BP0 Bit	Protected area	Unprotected area
0	0	0	none	All sectors(1) (128 sectors: 0 to 127)
0	0	1	Upper 64th (2 sectors: 126 and 127)	Lower 63/64ths (126 sectors: 0 to 125)
0	1	0	Upper 32nd (4 sectors: 124 to 127)	Lower 31/32nds (124 sectors: 0 to 123)
0	1	1	Upper sixteenth (8 sectors: 120 to 127)	Lower 15/16ths (120 sectors: 0 to 119)
1	0	0	Upper eighth (16 sectors: 112 to 127)	Lower seven-eighths (112 sectors: 0 to 111)
1	0	1	Upper quarter (32 sectors: 96 to 127)	Lower three-quarters (96 sectors: 0 to 95)
1	1	0	Upper half (64 sectors: 64 to 127)	Lower half (64 sectors: 0 to 63)
1	1	1	All sectors (128 sectors: 0 to 127)	none

1. The device is ready to accept a Bulk Erase instruction, if and only if, all Block Protect (BP2, BP1, BP0) are 0.

4.8 Hold Condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) Low.

The Hold condition starts on the falling edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in *Figure 6*).

The Hold condition ends on the rising edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low.

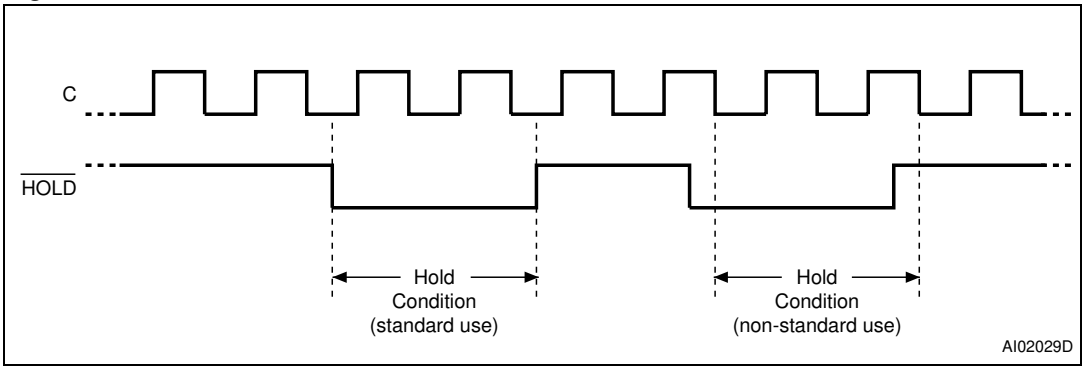
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. (This is shown in *Figure 6*).

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select ($\overline{\text{S}}$) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select ($\overline{\text{S}}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{\text{HOLD}}$) High, and then to drive Chip Select ($\overline{\text{S}}$) Low. This prevents the device from going back to the Hold condition.

Figure 6. Hold condition activation



5 Memory organization

The memory is organized as:

- 8388608 bytes (8 bits each)
- 128 sectors (512 Kbits, 65536 bytes each)
- 32768 pages (256 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable (bits are erased from 0 to 1) but not Page Erasable.

Figure 7. Block diagram

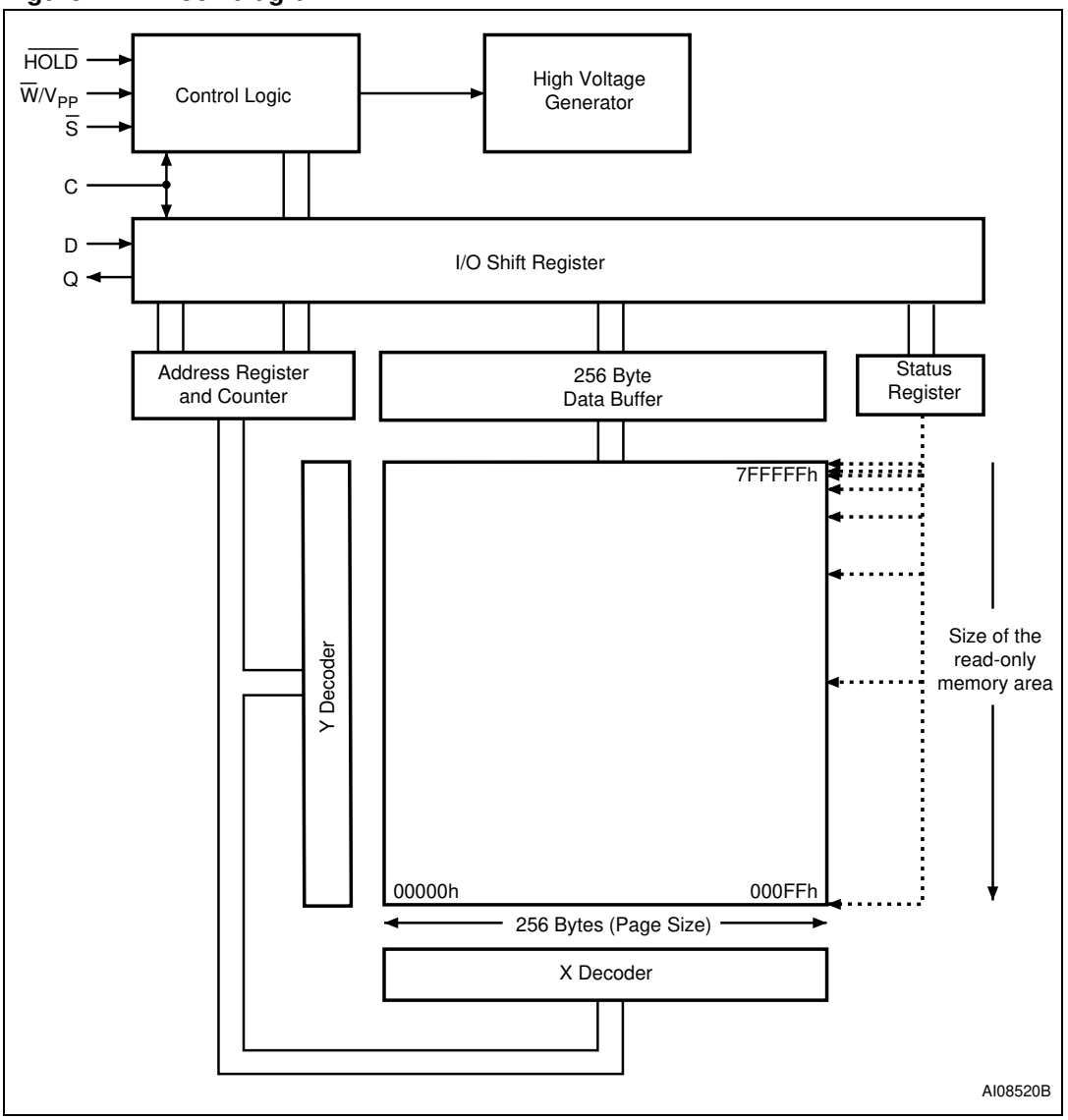


Table 3. Memory organization

Sector	Address range	
127	7F0000h	7FFFFFh
126	7E0000h	7EFFFFh
125	7D0000h	7DFFFFh
124	7C0000h	7CFFFFh
123	7B0000h	7BFFFFh
122	7A0000h	7AFFFFh
121	790000h	79FFFFh
120	780000h	78FFFFh
119	770000h	77FFFFh
118	760000h	76FFFFh
117	750000h	75FFFFh
116	740000h	74FFFFh
115	730000h	73FFFFh
114	720000h	72FFFFh
113	710000h	71FFFFh
112	700000h	70FFFFh
111	6F0000h	6FFFFFh
110	6E0000h	6EFFFFh
109	6D0000h	6DFFFFh
108	6C0000h	6CFFFFh
107	6B0000h	6BFFFFh
106	6A0000h	6AFFFFh
105	690000h	69FFFFh
104	680000h	68FFFFh
103	670000h	67FFFFh
102	660000h	66FFFFh
101	650000h	65FFFFh
100	640000h	64FFFFh
99	630000h	63FFFFh
98	620000h	62FFFFh
97	610000h	61FFFFh
96	600000h	60FFFFh
95	5F0000h	5FFFFFh
94	5E0000h	5EFFFFh
93	5D0000h	5DFFFFh

Table 3. Memory organization (continued)

Sector	Address range	
92	5C0000h	5CFFFFh
91	5B0000h	5BFFFFh
90	5A0000h	5AFFFFh
89	590000h	59FFFFh
88	580000h	58FFFFh
87	570000h	57FFFFh
86	560000h	56FFFFh
85	550000h	55FFFFh
84	540000h	54FFFFh
83	530000h	53FFFFh
82	520000h	52FFFFh
81	510000h	51FFFFh
80	500000h	50FFFFh
79	4F0000h	4FFFFFh
78	4E0000h	4EFFFFh
77	4D0000h	4DFFFFh
76	4C0000h	4CFFFFh
75	4B0000h	4BFFFFh
74	4A0000h	4AFFFFh
73	490000h	49FFFFh
72	480000h	48FFFFh
71	470000h	47FFFFh
70	460000h	46FFFFh
69	450000h	45FFFFh
68	440000h	44FFFFh
67	430000h	43FFFFh
66	420000h	42FFFFh
65	410000h	41FFFFh
64	400000h	40FFFFh
63	3F0000h	3FFFFFh
62	3E0000h	3EFFFFh
61	3D0000h	3DFFFFh
60	3C0000h	3CFFFFh
59	3B0000h	3BFFFFh
58	3A0000h	3AFFFFh

Table 3. Memory organization (continued)

Sector	Address range	
57	390000h	39FFFFh
56	380000h	38FFFFh
55	370000h	37FFFFh
54	360000h	36FFFFh
53	350000h	35FFFFh
52	340000h	34FFFFh
51	330000h	33FFFFh
50	320000h	32FFFFh
49	310000h	31FFFFh
48	300000h	30FFFFh
47	2F0000h	2FFFFFh
46	2E0000h	2EFFFFh
45	2D0000h	2DFFFFh
44	2C0000h	2CFFFFh
43	2B0000h	2BFFFFh
42	2A0000h	2AFFFFh
41	290000h	29FFFFh
40	280000h	28FFFFh
39	270000h	27FFFFh
38	260000h	26FFFFh
37	250000h	25FFFFh
36	240000h	24FFFFh
35	230000h	23FFFFh
34	220000h	22FFFFh
33	210000h	21FFFFh
32	200000h	20FFFFh
31	1F0000h	1FFFFFh
30	1E0000h	1EFFFFh
29	1D0000h	1DFFFFh
28	1C0000h	1CFFFFh
27	1B0000h	1BFFFFh
26	1A0000h	1AFFFFh
25	190000h	19FFFFh
24	180000h	18FFFFh
23	170000h	17FFFFh

Table 3. Memory organization (continued)

Sector	Address range	
22	160000h	16FFFFh
21	150000h	15FFFFh
20	140000h	14FFFFh
19	130000h	13FFFFh
18	120000h	12FFFFh
17	110000h	11FFFFh
16	100000h	10FFFFh
15	0F0000h	0FFFFFh
14	0E0000h	0EFFFFh
13	0D0000h	0DFFFFh
12	0C0000h	0CFFFFh
11	0B0000h	0BFFFFh
10	0A0000h	0AFFFFh
9	090000h	09FFFFh
8	080000h	08FFFFh
7	070000h	07FFFFh
6	060000h	06FFFFh
5	050000h	05FFFFh
4	040000h	04FFFFh
3	030000h	03FFFFh
2	020000h	02FFFFh
1	010000h	01FFFFh
0	000000h	00FFFFh

6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 4*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR), Read Identification (RDID) or Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN) or Write Disable (WRDI), Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
PP	Page Program	0000 0010	02h	3	0	1 to 256
SE	Sector Erase	1101 1000	D8h	3	0	0
BE	Bulk Erase	1100 0111	C7h	0	0	0
RES	Read Electronic Signature	1010 1011	ABh	0	3	1 to ∞

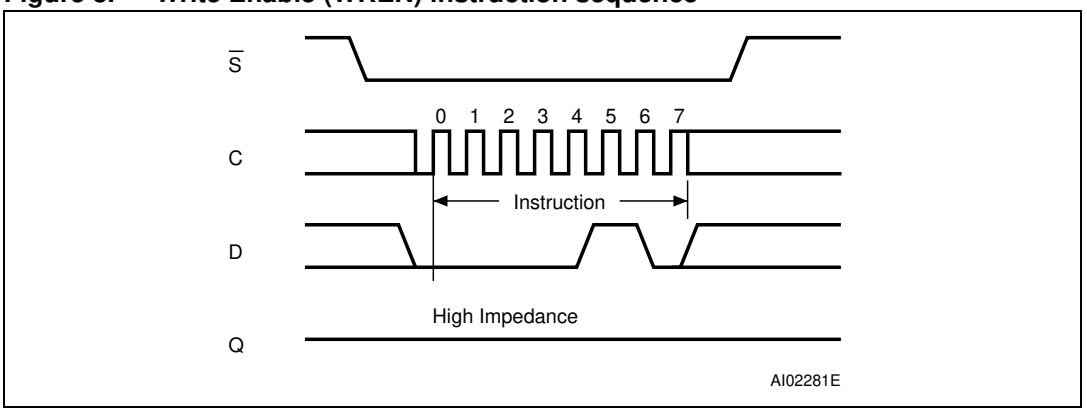
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 8*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 8. Write Enable (WREN) instruction sequence



6.2 Write Disable (WRDI)

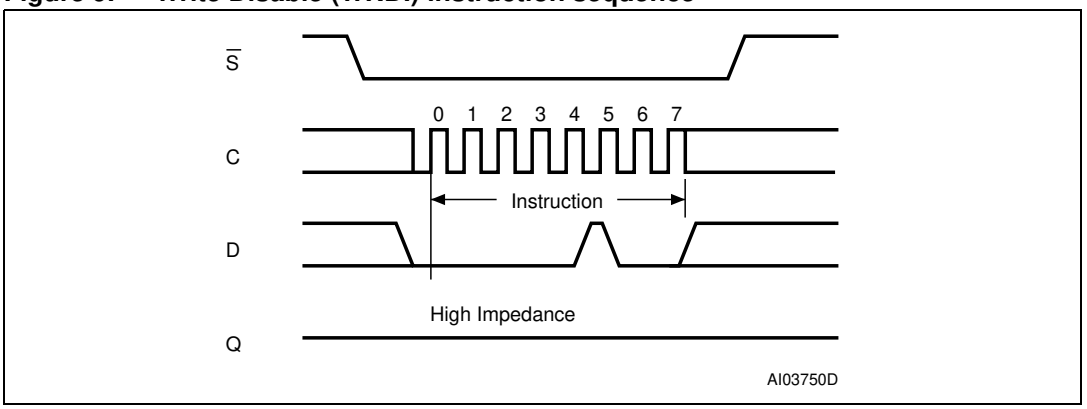
The Write Disable (WRDI) instruction (*Figure 9*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

Figure 9. Write Disable (WRDI) instruction sequence



6.3 Read Identification (RDID)

The read identification (RDID) instruction allows to read the device identification data:

- Manufacturer identification (1 byte)
- Device identification (2 bytes)
- A unique ID code (UID) (17 bytes, of which 16 available upon customer request).(1)

The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (20h), and the memory capacity of the device in the second byte (17h). The UID contains the length of the following data in the first byte (set to 10h) and 16 bytes of the optional customized factory data (CFD) content. The CFD bytes are read-only and can be programmed with customers data upon their demand. If the customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero (00h).

Any read identification (RDID) instruction while an erase or program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The read identification (RDID) instruction should not be issued while the device is in deep power-down mode.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification, stored in the memory, the 8-bit CFD length followed by 16 bytes of CFD content will be shifted out on serial data output (DQ1). Each bit is shifted out during the falling edge of Serial Clock (C). The instruction sequence is shown in *Figure 10*.

The read identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output. When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. Once in the standby power mode, the device waits to be selected so that it can receive, decode, and execute instructions.

Table 5. Read identification (RDID) data-out sequence

Manufacturer identification	Device identification		UID	
	Memory type	Memory capacity	CFD length	CFD content
20h	20h	17h	10h	16 bytes

1. The UID feature is available only for process technology T9HX devices, identified by process identification digit "4" in the device marking.