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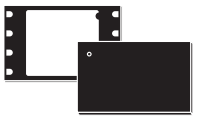
M25PX64

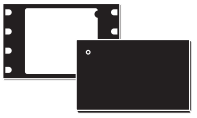
64-Mbit, dual I/O, 4-Kbyte subsector erase, serial flash memory with 75 MHz SPI bus interface

Features

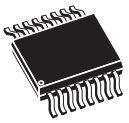
- SPI bus compatible serial interface
- 75 MHz (maximum) clock frequency
- 2.7 V to 3.6 V single supply voltage
- Dual input/output instructions resulting in an equivalent clock frequency of 150 MHz:
  - Dual output fast read instruction
  - Dual input fast program instruction
- Whole memory continuously read by sending once a fast read or a dual output fast read instruction and an address
- 64 Mbit Flash memory
  - Uniform 4-Kbyte subsectors
  - Uniform 64-Kbyte sectors
- Additional 64-byte user-lockable, one-time programmable (OTP) area
- Erase capability
  - Subsector (4-Kbyte) granularity
  - Sector (64-Kbyte) granularity
  - Bulk erase (64 Mbits) in 68 s (typical)
- Write protections
  - Software write protection applicable to every 64-Kbyte sector (volatile lock bit)
  - Hardware write protection: protected area size defined by three non-volatile bits (BP0, BP1 and BP2)
- Deep power-down mode: 5 µA (typical)
- Electronic signature
  - JEDEC standard two-byte signature (7117h)
  - Unique ID code (UID) with 16 bytes read-only, available upon customer request
- More than 100 000 write cycles per sector
- More than 20 years data retention
- Packages
  - RoHS compliant



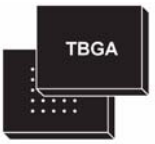
VDFPN8 (ME)
8 × 6 mm (MLP8)



VDFPN8 (MD)
8 × 6 mm (MLP8)
(with reduced D2 dimension)



SO16 (MF)
300 mils width



TBGA24 (ZM) 6x8 mm

- Automotive Certified Parts Available

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1 Description

The M25PX64 is a 64-Mbit (8 Mbits x 8) serial flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The M25PX64 supports two new, high-performance dual input/output instructions:

- Dual output fast read (DOFR) instruction used to read data at up to 75 MHz by using both pin DQ1 and pin DQ0 as outputs
- Dual input fast program (DIFP) instruction used to program data at up to 75 MHz by using both pin DQ1 and pin DQ0 as inputs

These new instructions double the transfer bandwidth for read and program operations.

The memory can be programmed 1 to 256 bytes at a time, using the page program instruction.

The memory is organized as 128 sectors that are further divided into 16 subsectors each (2048 subsectors in total).

The memory can be erased a 4-Kbyte subsector at a time, a 64-Kbyte sector at a time, or as a whole. It can be write protected by software using a mix of volatile and non-volatile protection features, depending on the application needs. The protection granularity is of 64 Kbytes (sector granularity).

The M25PX64 has 64 one-time-programmable bytes (OTP bytes) that can be read and programmed using two dedicated instructions, Read OTP (ROTP) and Program OTP (POTP), respectively. These 64 bytes can be permanently locked by a particular program OTP (POTP) sequence. Once they have been locked, they become read-only and this state cannot be reverted.

Further features are available as additional security options. More information on these security features is available, upon completion of an NDA (nondisclosure agreement), and are, therefore, not described in this datasheet. For more details of this option contact your nearest Numonyx sales office.

Figure 1. Logic diagram

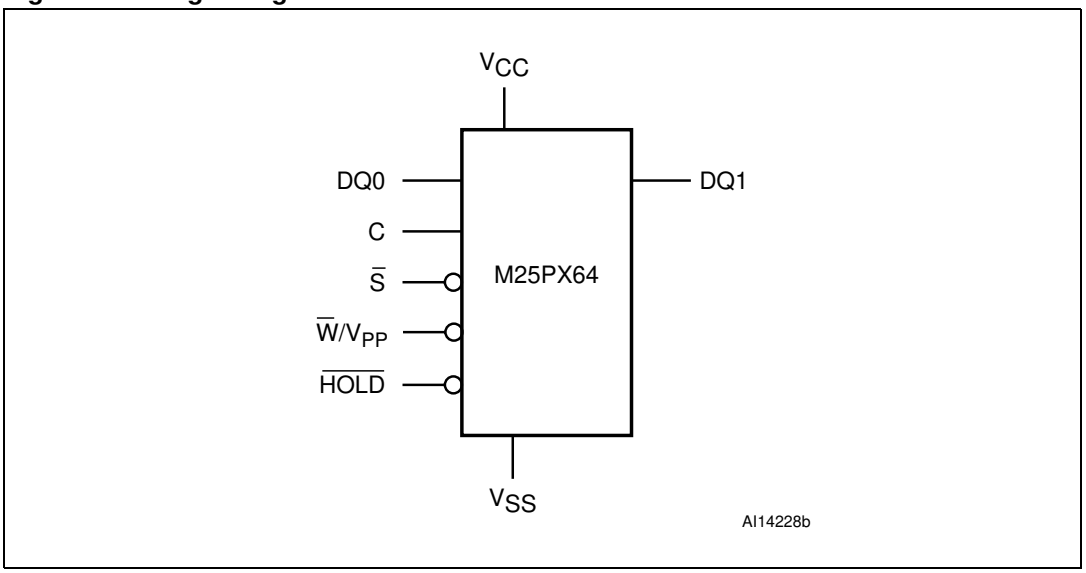
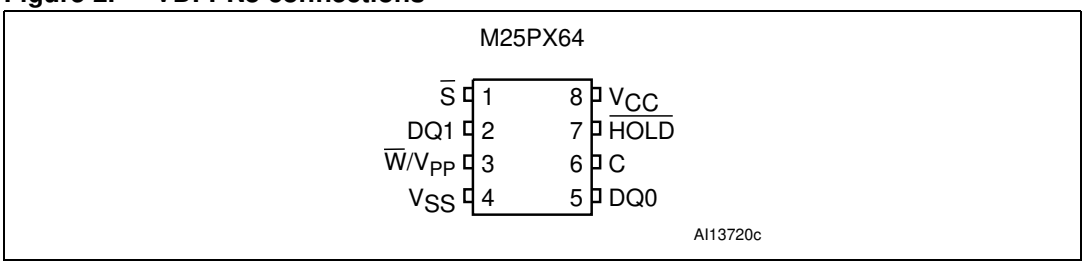


Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
DQ0	Serial Data input	I/O(1)
DQ1	Serial Data output	I/O(2)
$\overline{S}$	Chip Select	Input
$\overline{W}/V_{PP}$	Write Protect/Enhanced Program supply voltage	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	–
V_{SS}	Ground	–

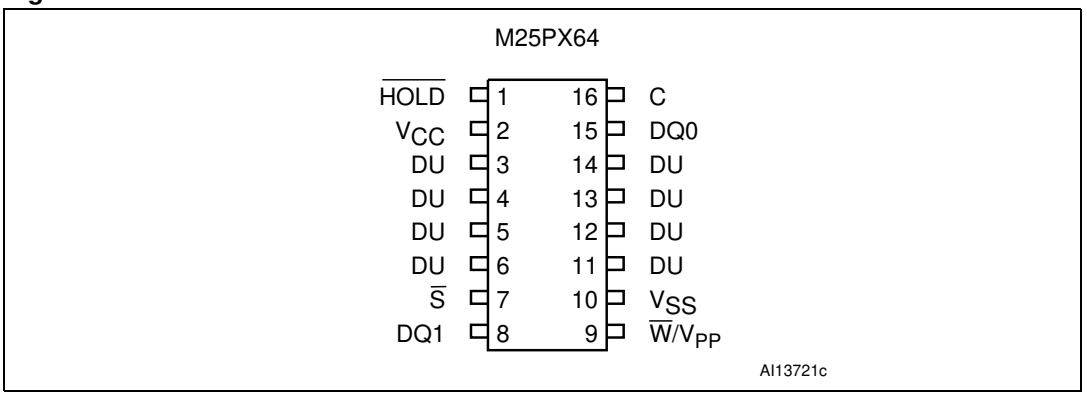
1. Serves as an output during dual output fast read (DOFR) instructions.
2. Serves as an input during dual input fast program (DIFP) instructions.

Figure 2. VDFPN8 connections



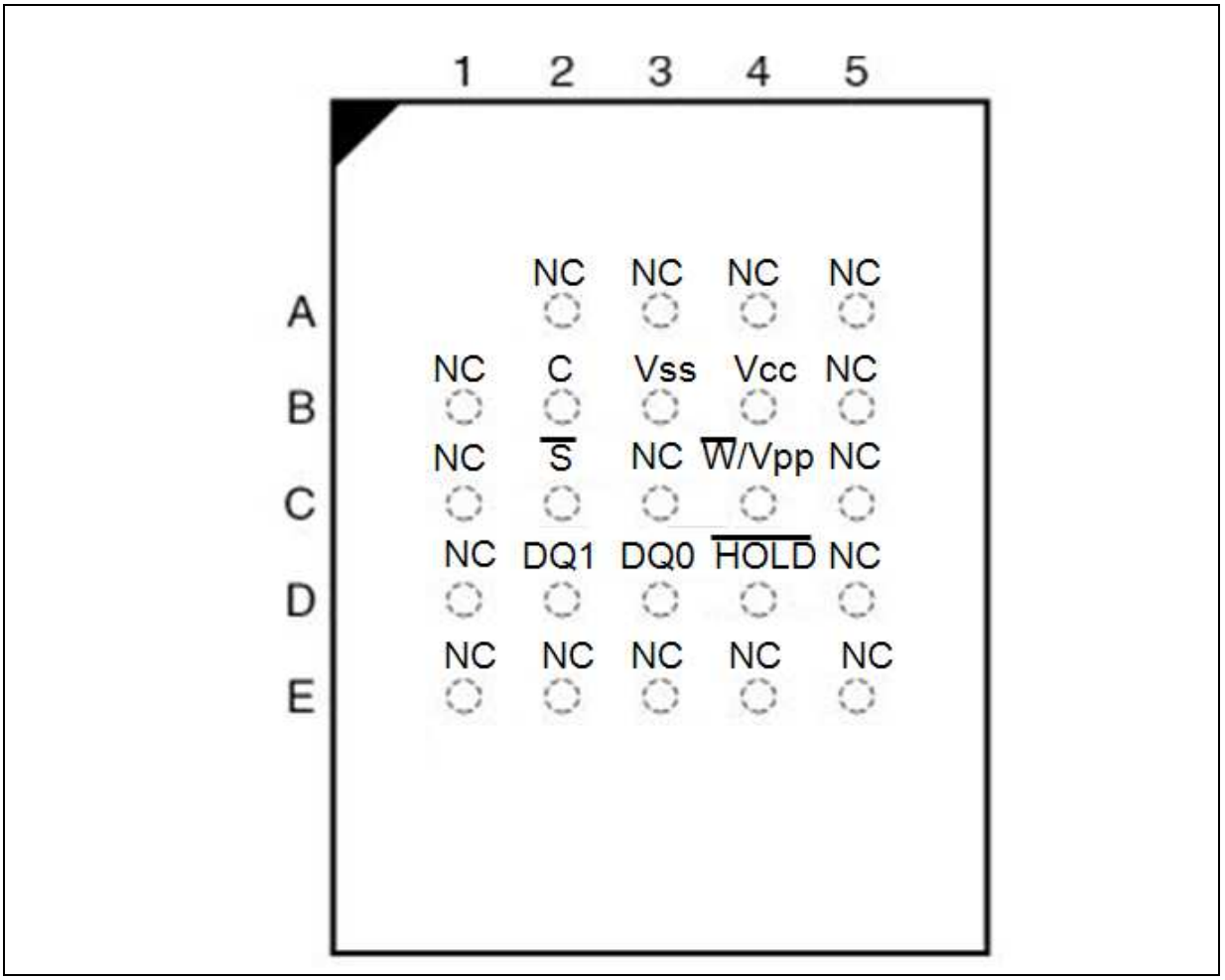
1. There is an exposed central pad on the underside of the VDFPN8 package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

Figure 3. SO16 connections



1. DU = don't use.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

Figure 4. BGA 6x8 24 ball ballout



Note: 1 NC = No Connection

2 See Section 11: Package mechanical.

2 Signal descriptions

2.1 Serial data output (DQ1)

This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (C).

During the dual input fast program (DIFP) instruction, pin DQ1 is used as an input. It is latched on the rising edge of the Serial Clock (C).

2.2 Serial data input (DQ0)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

During the dual output fast read (DOFR) instruction, pin DQ0 is used as an output. Data are shifted out on the falling edge of the Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (DQ0) are latched on the rising edge of Serial Clock (C). Data on serial data output (DQ1) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and serial data output (DQ1) is at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

To start the hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write protect/enhanced program supply voltage ($\overline{W}/V_{PP}$)

$\overline{W}/V_{PP}$ is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If the $\overline{W}/V_{PP}$ input is kept in a low voltage range (0 V to V_{CC}) the pin is seen as a control input. This input signal is used to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the status register. See *Table 9*).

If V_{PP} is in the range of V_{PPH} (as defined in *Table 15*) it acts as an additional power supply.(1)

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

1. Avoid applying V_{PPH} to the $\overline{W}$/VPP pin during Bulk Erase.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

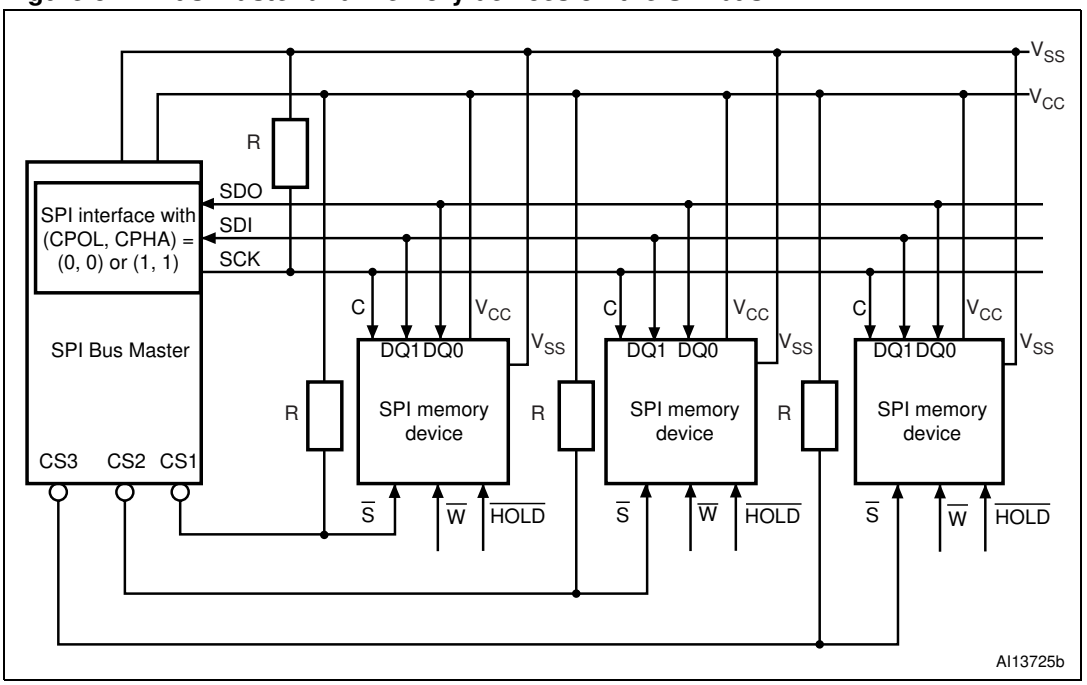
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 6*, is the clock polarity when the bus master is in standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. Bus master and memory devices on the SPI bus

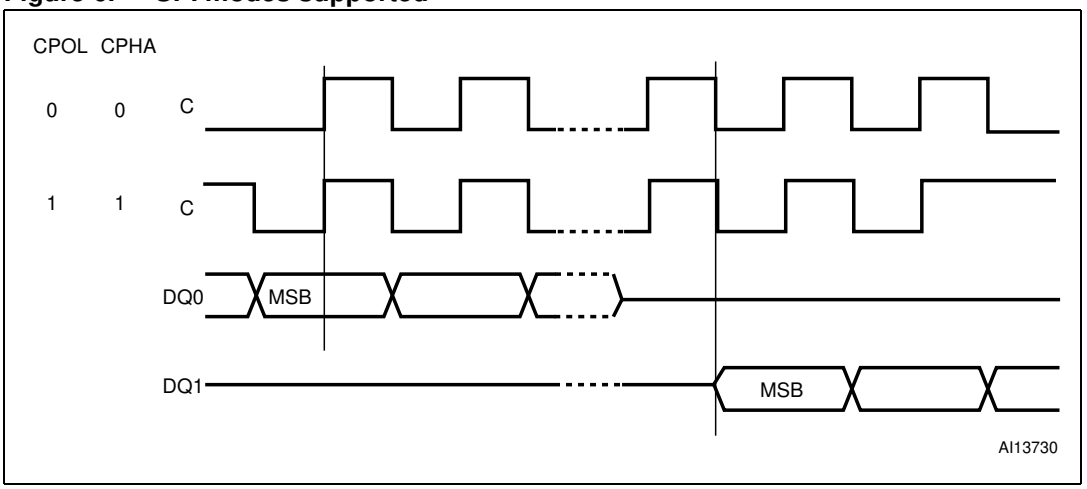


1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 5 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the serial data output (DQ1) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 5*) ensure that the M25PX64 is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$ (C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 6. SPI modes supported



4 Operating features

4.1 Page programming

To program one data byte, two instructions are required: write enable (WREN), which is one byte, and a page program (PP) sequence, which consists of four bytes plus data. This is followed by the internal program cycle (of duration t_{PP}).

To spread this overhead, the page program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from ‘1’ to ‘0’), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Page program (PP)* and *Table 18: AC characteristics*).

4.2 Dual input fast program

The dual input fast program (DIFP) instruction makes it possible to program up to 256 bytes using two input pins at the same time (by changing bits from ‘1’ to ‘0’).

For optimized timings, it is recommended to use the dual input fast program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several dual input fast program (DIFP) sequences each containing only a few bytes (see *Section 6.12: Dual input fast program (DIFP)*).

4.3 Subsector erase, sector erase and bulk erase

The page program (PP) instruction allows bits to be reset from ‘1’ to ’0’. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a subsector at a time, using the subsector erase (SSE) instruction, a sector at a time, using the sector erase (SE) instruction, or throughout the entire memory, using the bulk erase (BE) instruction. This starts an internal erase cycle (of duration t_{SSE}, t_{SE} or t_{BE}).

The erase instruction must be preceded by a write enable (WREN) instruction.

4.4 Polling during a write, program or erase cycle

A further improvement in the time to write status register (WRSR), program OTP (POTP), program (PP), dual input fast program (DIFP) or erase (SSE, SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SSE}, t_{SE}, or t_{BE}). The write in progress (WIP) bit is provided in the status register so that the application program can monitor its value, polling it to establish when the previous write cycle, program cycle or erase cycle is complete.

4.5 Active power, standby power and deep power-down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write status register). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

The deep power-down mode is entered when the specific instruction (the deep power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the release from deep power-down (RDP) instruction) is executed.

While in the deep power-down mode, the device ignores all write, program and erase instructions (see *Section 6.18: Deep power-down (DP)*), this can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent write, program or erase instructions.

4.6 Status register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.4: Read status register (RDSR)* for a detailed description of the status register bits.

4.7 Protection modes

There are protocol-related and specific hardware and software protection modes. They are described below.

4.7.1 Protocol-related protections

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25PX64 features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification
- Program, erase and write status register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write disable (WRDI) instruction completion
  - Write status register (WRSR) instruction completion
  - Write to lock register (WRLR) instruction completion
  - Program OTP (POTP) instruction completion
  - Page program (PP) instruction completion
  - Dual input fast program (DIFP) instruction completion
  - Subsector erase (SSE) instruction completion
  - Sector erase (SE) instruction completion
  - Bulk erase (BE) instruction completion
- In addition to the low power consumption feature, the deep power-down mode offers extra software protection, as all write, program and erase instructions are ignored.

4.7.2 Specific hardware and software protection

There are two software protected modes, SPM1 and SPM2, that can be combined to protect the memory array as required. The SPM2 can be locked by hardware with the help of the $\overline{W}$ input pin.

SPM1 and SPM2

- The first software protected mode (SPM1) is managed by specific lock registers assigned to each 64-Kbyte sector.

  The lock registers can be read and written using the read lock register (RDLR) and write to lock register (WRLR) instructions.

  In each lock register two bits control the protection of each sector: the write lock bit and the lock down bit.

  – Write lock bit:

    The write lock bit determines whether the contents of the sector can be modified (using the write, program or erase instructions). When the write lock bit is set to '1', the sector is write protected – any operations that attempt to change the data in the sector will fail. When the write lock bit is reset to '0', the sector is not write protected by the lock register, and may be modified.

  – Lock down bit:

    The lock down bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the lock down bit is set to '1', further modification to the write lock and lock down bits cannot be performed. A power-up is required before changes to these bits can be made. When the lock down bit is reset to '0', the write lock and lock down bits can be changed.

  The definition of the lock register bits is given in *Table 9: Lock register out*.

Table 2. Software protection truth table (sectors 0 to 127, 64-Kbyte granularity)

Sector lock register		Protection status
Lock down bit	Write lock bit	
0	0	Sector unprotected from program/erase/write operations, protection status reversible
0	1	Sector protected from program/erase/write operations, protection status reversible
1	0	Sector unprotected from program/erase/write operations, Sector protection status cannot be changed except by a power-up.
1	1	Sector protected from program/erase/write operations, Sector protection status cannot be changed except by a power-up.

- the second software protected mode (SPM2) uses the block protect bits (see *Section 6.4.3: BP2, BP1, BP0 bits*) and the top/bottom bit (see *Section 6.4.4: Top/bottom bit*) to allow part of the memory to be configured as read-only.

Table 3. Protected area sizes

Status register contents				Memory content	
TB bit	BP bit 2	BP bit 1	BP bit 0	Protected area	Unprotected area
0	0	0	0	none	All sectors(1) (128 sectors: 0 to 127)
0	0	0	1	Upper 64th (2 sectors: 126 and 127)	Lower 63/64ths (126 sectors: 0 to 125)
0	0	1	0	Upper 32nd (4 sectors: 124 to 127)	Lower 31/32nds (124 sectors: 0 to 123)
0	0	1	1	Upper 16th (8 sectors: 120 to 127)	Lower 15/16ths (120 sectors: 0 to 119)
0	1	0	0	Upper 8th (16 sectors: 56 to 63)	Lower 7/8ths (112 sectors: 0 to 111)
0	1	0	1	Upper quarter (32 sectors: 96 to 127)	Lower three-quarters (96 sectors: 0 to 95)
0	1	1	0	Upper half (64 sectors: 64 to 127)	Lower half (64 sectors: 0 to 63)
0	1	1	1	All sectors (128 sectors: 0 to 127)	none
1	0	0	0	none	All sectors(1) (128 sectors: 0 to 128)
1	0	0	1	Lower 64th (2 sectors: 0 to1)	Upper 63/64ths (126 sectors: 2 to 127)
1	0	1	0	Lower 32nd (4 sectors: 0 to 3)	Upper 31/32nds (124 sectors: 4 to 127)
1	0	1	1	Lower 16th (8 sectors: 0 to 7)	Upper 15/16ths (120 sectors: 8 to 127)
1	1	0	0	Lower 8th (16 sectors: 0 to15)	Upper 7/8ths (112 sectors: 16 to 127)
1	1	0	1	Lower 4th (32 sectors: 0 to 31)	Upper 3/4ths (96 sectors: 32 to 127)
1	1	1	0	Lower half (64 sectors: 0 to 63)	Upper half (64 sectors: 64 to 127)
1	1	1	1	All sectors (128 sectors: 0 to 127)	none

1. The device is ready to accept a bulk erase instruction if, and only if, all block protect (BP2, BP1, BP0) are 0.

As a second level of protection, the Write Protect signal (applied on the $\overline{W}/V_{PP}$ pin) can freeze the status register in a read-only mode. In this mode, the block protect bits (BP2, BP1, BP0) and the status register write disable bit (SRWD) are protected. For more details, see *Section 6.5: Write status register (WRSR)*.

4.8 Hold condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any write status register, program or erase cycle that is currently in progress.

To enter the hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) Low.

The hold condition starts on the falling edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in *Figure 7*).

The hold condition ends on the rising edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low.

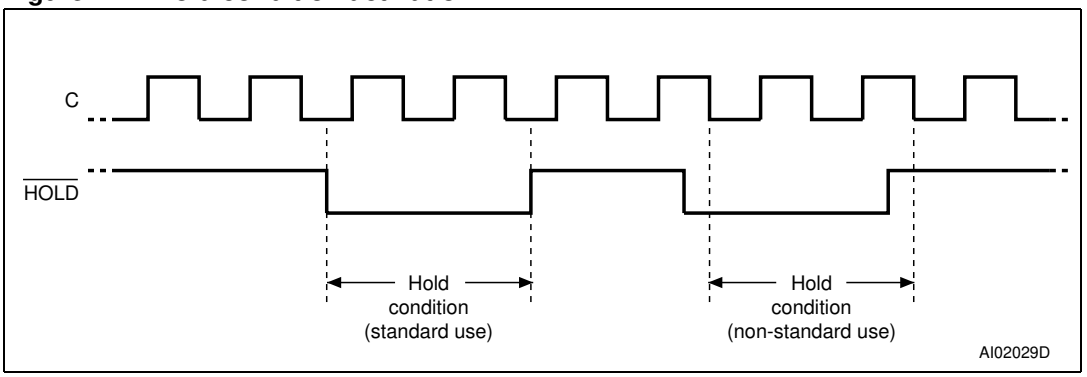
If the falling edge does not coincide with Serial Clock (C) being Low, the hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the hold condition ends after Serial Clock (C) next goes Low (this is shown in *Figure 7*).

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

Normally, the device is kept selected, with Chip Select ($\overline{\text{S}}$) driven Low, for the whole duration of the hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the hold condition.

If Chip Select ($\overline{\text{S}}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{\text{HOLD}}$) High, and then to drive Chip Select ($\overline{\text{S}}$) Low. This prevents the device from going back to the hold condition.

Figure 7. Hold condition activation



5 Memory organization

The memory is organized as:

- 8 388 608 bytes (8 bits each)
- 2048 subsectors (4 Kbytes each)
- 128 sectors (64 Kbytes each)
- 32768 pages (256 bytes each)
- 64 OTP bytes located outside the main memory array.

Each page can be individually programmed (bits are programmed from ‘1’ to ‘0’). The device is subsector, sector or bulk erasable (bits are erased from ‘0’ to ‘1’) but not page erasable.

Figure 8. Block diagram

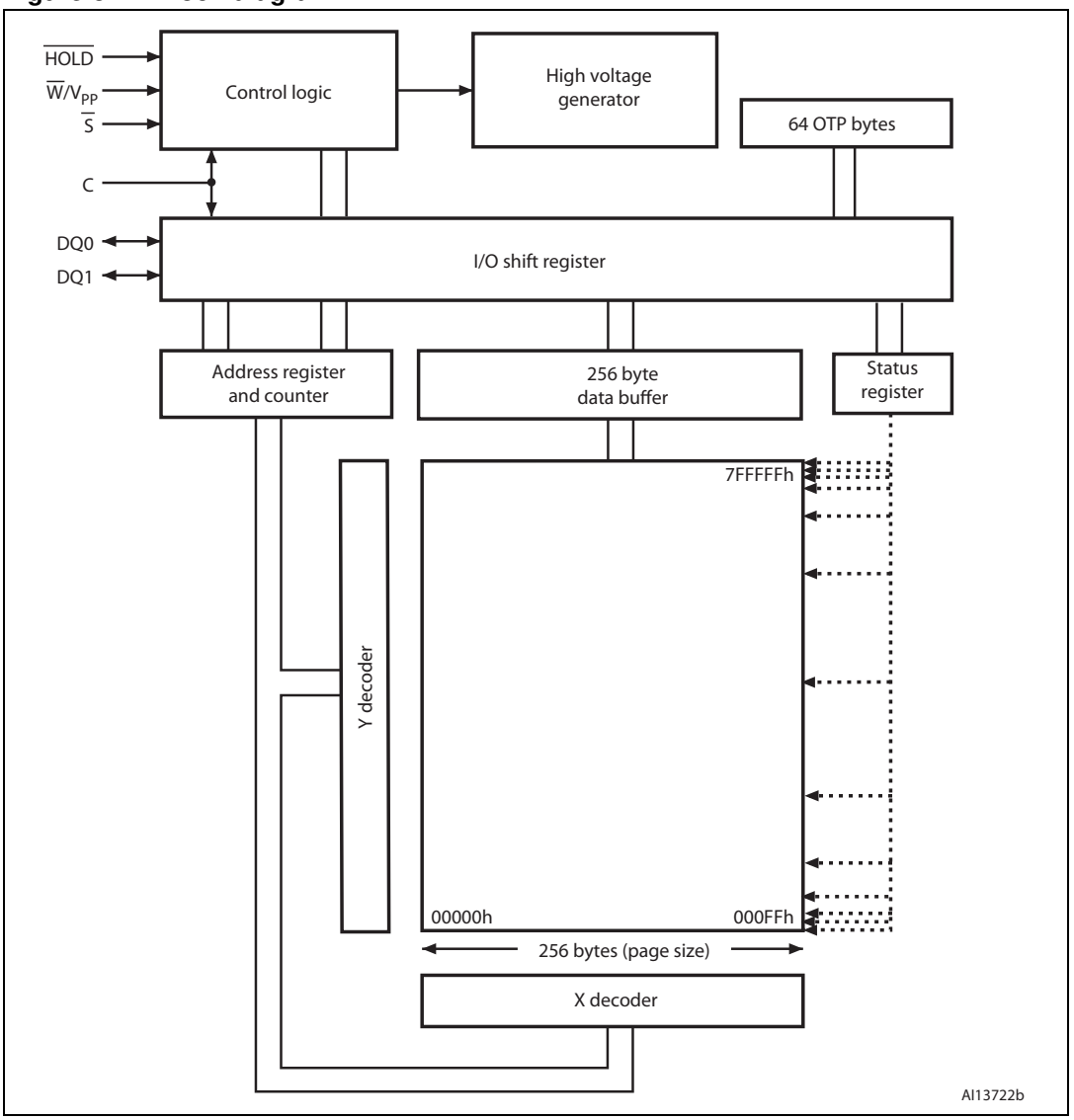


Table 4. Memory organization

Sector	Subsector	Address range	
127	2047	7FF000h	7FFFFFh
	⋮	⋮	⋮
	2032	7F0000h	7F0FFFh
126	2031	7EF000h	7EFFFFh
	⋮	⋮	⋮
	2016	7E0000h	7E0FFFh
125	2015	7DF000h	7DFFFFh
	⋮	⋮	⋮
	2000	7D0000h	7D0FFFh
124	1999	7CF000h	7CFFFFh
	⋮	⋮	⋮
	1984	7C0000h	7C0FFFh
123	1983	7BF000h	7BFFFFh
	⋮	⋮	⋮
	1968	7B0000h	7B0FFFh
122	1967	7AF000h	7AFFFFh
	⋮	⋮	⋮
	1952	7A0000h	7A0FFFh
121	1951	79F000h	79FFFFh
	⋮	⋮	⋮
	1936	790000h	790FFFh
120	1935	78F000h	78FFFFh
	⋮	⋮	⋮
	1920	780000h	780FFFh
119	1919	77F000h	77FFFFh
	⋮	⋮	⋮
	1904	770000h	770FFFh
118	1903	76F000h	76FFFFh
	⋮	⋮	⋮
	1888	760000h	760FFFh
117	1887	75F000h	75FFFFh
	⋮	⋮	⋮
	1872	750000h	750FFFh
116	1871	74F000h	74FFFFh
	⋮	⋮	⋮
	1856	740000h	740FFFh
115	1855	73F000h	73FFFFh
	⋮	⋮	⋮
	1840	730000h	730FFFh
114	1839	72F000h	72FFFFh
	⋮	⋮	⋮
	1824	720000h	720FFFh
113	1823	71F000h	71FFFFh
	⋮	⋮	⋮
	1808	710000h	710FFFh
112	1807	70F000h	70FFFFh
	⋮	⋮	⋮
	1792	700000h	700FFFh
111	1791	6FF000h	6FFFFFh
	⋮	⋮	⋮
	1776	6F0000h	6F0FFFh
110	1775	6EF000h	6EFFFFh
	⋮	⋮	⋮
	1760	6E0000h	6E0FFFh
109	1759	6DF000h	6DFFFFh
	⋮	⋮	⋮
	1744	6D0000h	6D0FFFh
108	1743	6CF000h	6CFFFFh
	⋮	⋮	⋮
	1728	6C0000h	6C0FFFh
107	1727	6BF000h	6BFFFFh
	⋮	⋮	⋮
	1712	6B0000h	6B0FFFh
106	1711	6AF000h	6AFFFFh
	⋮	⋮	⋮
	1696	6A0000h	6A0FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
105	1695	69F000h	69FFFFh
	⋮	⋮	⋮
	1680	690000h	690FFFh
104	1679	68F000h	68FFFFh
	⋮	⋮	⋮
	1664	680000h	680FFFh
103	1663	67F000h	67FFFFh
	⋮	⋮	⋮
	1648	670000h	670FFFh
102	1647	66F000h	66FFFFh
	⋮	⋮	⋮
	1632	660000h	660FFFh
101	1631	65F000h	65FFFFh
	⋮	⋮	⋮
	1616	650000h	650FFFh
100	1615	64F000h	64FFFFh
	⋮	⋮	⋮
	1600	640000h	640FFFh
99	1599	63F000h	63FFFFh
	⋮	⋮	⋮
	1584	630000h	630FFFh
98	1583	62F000h	62FFFFh
	⋮	⋮	⋮
	1568	620000h	620FFFh
97	1567	61F000h	61FFFFh
	⋮	⋮	⋮
	1552	610000h	610FFFh
96	1551	60F000h	60FFFFh
	⋮	⋮	⋮
	1536	600000h	600FFFh
95	1535	5FF000h	5FFFFFh
	⋮	⋮	⋮
	1520	5F0000h	5F0FFFh
94	1519	5EF000h	5EFFFFh
	⋮	⋮	⋮
	1504	5E0000h	5E0FFFh
93	1503	5DF000h	5DFFFFh
	⋮	⋮	⋮
	464	5D0000h	5D0FFFh
92	1487	5CF000h	5CFFFFh
	⋮	⋮	⋮
	1472	5C0000h	5C0FFFh
91	1471	5BF000h	5BFFFFh
	⋮	⋮	⋮
	1456	5B0000h	5B0FFFh
90	1455	5AF000h	5AFFFFh
	⋮	⋮	⋮
	1440	5A0000h	5A0FFFh
89	1439	59F000h	59FFFFh
	⋮	⋮	⋮
	1424	590000h	590FFFh
88	1423	58F000h	58FFFFh
	⋮	⋮	⋮
	1408	580000h	580FFFh
87	1407	57F000h	57FFFFh
	⋮	⋮	⋮
	1392	570000h	570FFFh
86	1391	56F000h	56FFFFh
	⋮	⋮	⋮
	1376	560000h	560FFFh
85	1375	55F000h	55FFFFh
	⋮	⋮	⋮
	1360	550000h	550FFFh
84	1359	54F000h	54FFFFh
	⋮	⋮	⋮
	1344	540000h	540FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
83	1343	53F000h	53FFFFh
	⋮	⋮	⋮
	1328	530000h	530FFFh
82	1327	52F000h	52FFFFh
	⋮	⋮	⋮
	1312	520000h	520FFFh
81	1311	51F000h	51FFFFh
	⋮	⋮	⋮
	1296	510000h	510FFFh
80	1295	50F000h	50FFFFh
	⋮	⋮	⋮
	1280	500000h	500FFFh
79	1279	4FF000h	4FFFFFh
	⋮	⋮	⋮
	1264	4F0000h	4F0FFFh
78	1263	4EF000h	4EFFFFh
	⋮	⋮	⋮
	1248	4E0000h	4E0FFFh
77	1247	4DF000h	4DFFFFh
	⋮	⋮	⋮
	1232	4D0000h	4D0FFFh
76	1231	4CF000h	4CFFFFh
	⋮	⋮	⋮
	1216	4C0000h	4C0FFFh
75	1215	4BF000h	4BFFFFh
	⋮	⋮	⋮
	1200	4B0000h	4B0FFFh
74	1199	4AF000h	4AFFFFh
	1184	4A0000h	4A0FFFh
73	1183	49F000h	49FFFFh
	⋮	⋮	⋮
	1168	490000h	490FFFh

Sector	Subsector	Address range	
72	1167	48F000h	48FFFFh
	⋮	⋮	⋮
	1152	480000h	480FFFh
71	1151	47F000h	47FFFFh
	⋮	⋮	⋮
	1136	470000h	470FFFh
70	1135	46F000h	46FFFFh
	⋮	⋮	⋮
	1120	460000h	460FFFh
69	1119	45F000h	45FFFFh
	⋮	⋮	⋮
	1104	450000h	450FFFh
68	1103	44F000h	44FFFFh
	⋮	⋮	⋮
	1088	440000h	440FFFh
67	1087	43F000h	43FFFFh
	⋮	⋮	⋮
	1072	430000h	430FFFh
66	1071	42F000h	42FFFFh
	⋮	⋮	⋮
	1056	420000h	420FFFh
65	1055	41F000h	41FFFFh
	⋮	⋮	⋮
	1040	410000h	410FFFh
64	1039	40F000h	40FFFFh
	⋮	⋮	⋮
	1024	400000h	400FFFh
63	1023	3FF000h	3FF000h
	⋮	⋮	⋮
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	⋮	⋮	⋮
	992	3E0000h	3E0FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
61	991	3DF000h	3DFFFFh
	⋮	⋮	⋮
	976	3D0000h	3D0FFFh
60	975	3CF000h	3CFFFFh
	⋮	⋮	⋮
	960	3C0000h	3C0FFFh
59	959	3BF000h	3BFFFFh
	⋮	⋮	⋮
	944	3B0000h	3B0FFFh
58	943	3AF000g	3AFFFFh
	⋮	⋮	⋮
	928	3A0000h	3A0FFFh
57	927	39F000h	39FFFFh
	⋮	⋮	⋮
	912	390000h	390FFFh
56	911	38F000h	38FFFFh
	⋮	⋮	⋮
	896	380000h	380FFFh
55	895	37F000h	37FFFFh
	⋮	⋮	⋮
	880	370000h	370FFFh
54	879	36F000h	36FFFFh
	⋮	⋮	⋮
	864	360000h	360FFFh
53	863	35F000h	35FFFFh
	⋮	⋮	⋮
	848	350000h	350FFFh
52	847	34F000h	34FFFFh
	⋮	⋮	⋮
	832	340000h	340FFFh
51	831	33F000h	33FFFFh
	⋮	⋮	⋮
	816	330000h	330FFFh

Sector	Subsector	Address range	
50	815	32F000h	32FFFFh
	⋮	⋮	⋮
	800	320000h	320FFFh
49	799	31F000h	31FFFFh
	⋮	⋮	⋮
	784	310000h	310FFFh
48	783	30F000h	30FFFFh
	⋮	⋮	⋮
	768	300000h	300FFFh
47	767	2FF000h	2FFFFFh
	⋮	⋮	⋮
	752	2F0000h	2F0FFFh
46	751	2EF000h	2EFFFFh
	⋮	⋮	⋮
	736	2E0000h	2E0FFFh
45	735	2DF000h	2DFFFFh
	⋮	⋮	⋮
	720	2D0000h	2D0FFFh
44	719	2CF000h	2CFFFFh
	⋮	⋮	⋮
	704	2C0000h	2C0FFFh
43	703	2BF000h	2BFFFFh
	⋮	⋮	⋮
	688	2B0000h	2B0FFFh
42	687	2AF000h	2AFFFFh
	⋮	⋮	⋮
	672	2A0000h	2A0FFFh
41	671	29F000h	29FFFFh
	⋮	⋮	⋮
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	⋮	⋮	⋮
	640	280000h	280FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
39	639	27F000h	27FFFFh
	⋮	⋮	⋮
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	⋮	⋮	⋮
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	⋮	⋮	⋮
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	⋮	⋮	⋮
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	⋮	⋮	⋮
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	⋮	⋮	⋮
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	⋮	⋮	⋮
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	⋮	⋮	⋮
	512	200000h	200FFFh
31	511	1FF000h	1FFFFFh
	⋮	⋮	⋮
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	⋮	⋮	⋮
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	⋮	⋮	⋮
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	⋮	⋮	⋮
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	⋮	⋮	⋮
	288	120000h	120FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh
15	255	FF000h	FFFFFh
	⋮	⋮	⋮
	240	F0000h	F0FFFh
14	239	EF000h	EFFFFh
	⋮	⋮	⋮
	224	E0000h	E0FFFh
13	223	DF000h	DFFFFh
	⋮	⋮	⋮
	208	D0000h	D0FFFh
12	207	CF000h	CFFFFh
	⋮	⋮	⋮
	192	C0000h	C0FFFh
11	191	BF000h	BFFFFh
	⋮	⋮	⋮
	176	B0000h	B0FFFh
10	175	AF000h	AFFFFh
	160	A0000h	A0FFFh
9	159	9F000h	9FFFFh
	⋮	⋮	⋮
	144	90000h	90FFFh
8	143	8F000h	8FFFFh
	⋮	⋮	⋮
	128	80000h	80FFFh
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh