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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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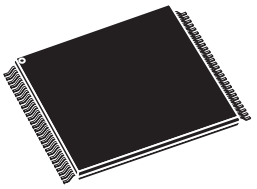
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

M29DW127G

128-Mbit (8 Mbit x16 or 16 Mbit x8 , multiple bank, page, dual boot) 3 V supply flash memory

Features

- Supply voltage
  - V_{CC} = 2.7 to 3.6 V for program, erase and read
  - V_{CCQ} = 1.65 to 3.6 V for I/O buffers
  - V_{PPH} = 12 V for fast program (optional)
- Asynchronous random/page read
  - Page width: 8 words / 16 bytes
  - Page access: 25 ns
  - Random access: 60 or 70, 80 ns
- Enhanced Buffered Program commands
  - 256 words
- Programming time
  - 15 µs per byte/word (typical)
  - 32-word write buffer
  - Chip program time: 5 s with V_{PPH} and 8 s without V_{PPH}
- Erase verify
- Memory blocks
  - Quadruple bank memory array: 16 Mbit+48 Mbit+48 Mbit+16 Mbit
  - Parameter blocks (at top and bottom)
- Dual operation
  - while program or erase in one bank, read in any of the other banks
- Program/erase suspend and resume modes
  - Read from any block during program suspend
  - Read and program another block during erase suspend
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer/ Enhanced Buffered Program commands
  - Faster production/batch programming
  - Faster block and chip erase
- Common flash interface
  - 64-bit security code



TSOP56 (NF)
14 x 20 mm

TBGA64 (ZA)
10 x 13 mm

- 100,000 program/erase cycles per block
- Low power consumption
  - Standby and automatic standby
- Hardware block protection
  - V_{PP}/$\overline{WP}$ pin for fast program and write protect of the four outermost parameter blocks
- Security features
  - Volatile protection
  - Non-volatile protection
  - Password protection
  - Additional block protection
- Extended memory block
  - Extra block (128-word / 256-byte factory locked and 128-word / 256-byte customer lockable) used as security block or to store additional information
- Electronic signature
  - Manufacturer code: 0020h
  - Device code: 227Eh+2220h+2204h
- ECOPACK® packages available

Contents

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1 Description

The M29DW127G is a 128-Mbit (8 Mbit x16 / 16 Mbit x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. At power-up the memory defaults to its read mode.

The M29DW127G features an asymmetrical block architecture, with 8 parameter and 62 main blocks, divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank. The bank architecture is summarized in *Table 2*. Four of the parameter blocks are at the top of the memory address space, and four are at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The Chip Enable, Output Enable and Write Enable signals control the bus operations of the memory. They allow simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the memory array. The device also features a write to buffer program capability that improves the programming throughput by programming in one shot a buffer of 32 words / 64 bytes. The enhanced buffered program feature is also available to speed up programming throughput, allowing 256 words to be programmed at once (only available in x16 mode). The $V_{PP}/\overline{WP}$ signal can be used to enable faster programming of the device.

The M29DW127G has one extra 256-word block in x16 mode or one extra 512-byte block in x8 mode (extended block, 128 words / 256 bytes factory locked and 128 words / 256 bytes customer lockable) that can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently, so it is possible to preserve valid data while old data is erased.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection
  - The $V_{PP}/\overline{WP}$ provides a hardware protection of the four outermost parameter blocks (two at the top and two at the bottom of the address space)
- Software protection
  - Volatile protection
  - Non-volatile protection
  - Password protection
- Additional protection features are available upon customer request.

The memory is offered in TSOP56 (14 x 20 mm) and TBGA64 (10 x 13 mm, 1 mm pitch) packages. The memory is delivered with all the bits erased (set to ‘1’).

Table 1. Signal names

Name	Description	Direction
A0-A22	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or address input	I/O
$\overline{E}$	Chip enable	Input
$\overline{G}$	Output enable	Input
$\overline{W}$	Write enable	Input
$\overline{RP}$	Reset	Input
$R\overline{B}$	Ready/busy output	Output
$\overline{BYTE}$	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
$V_{PP}/\overline{WP}$(1)	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

1. $V_{PP}/\overline{WP}$ may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

Figure 1. Logic diagram

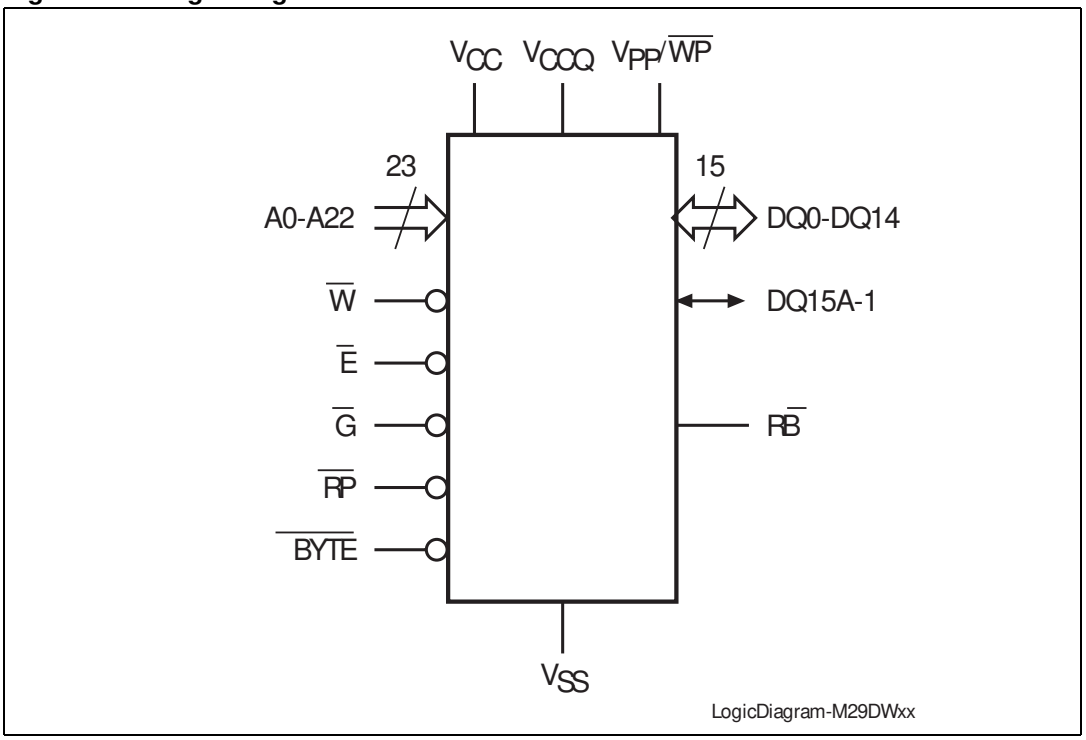


Table 2. Bank architecture

Bank	Bank size	Parameter blocks		Main blocks	
		N. of blocks	Block size	N. of blocks	Block size
A	16 Mbit	4	32 Kwords / 64 Kbytes	7	128 Kwords / 256 Kbytes
B	48 Mbit	—	—	24	128 Kwords / 256 Kbytes
C	48 Mbit	—	—	24	128 Kwords / 256 Kbytes
D	16 Mbit	4	32 Kwords / 64 Kbytes	7	128 Kwords / 256 Kbytes

Figure 2. TSOP connections

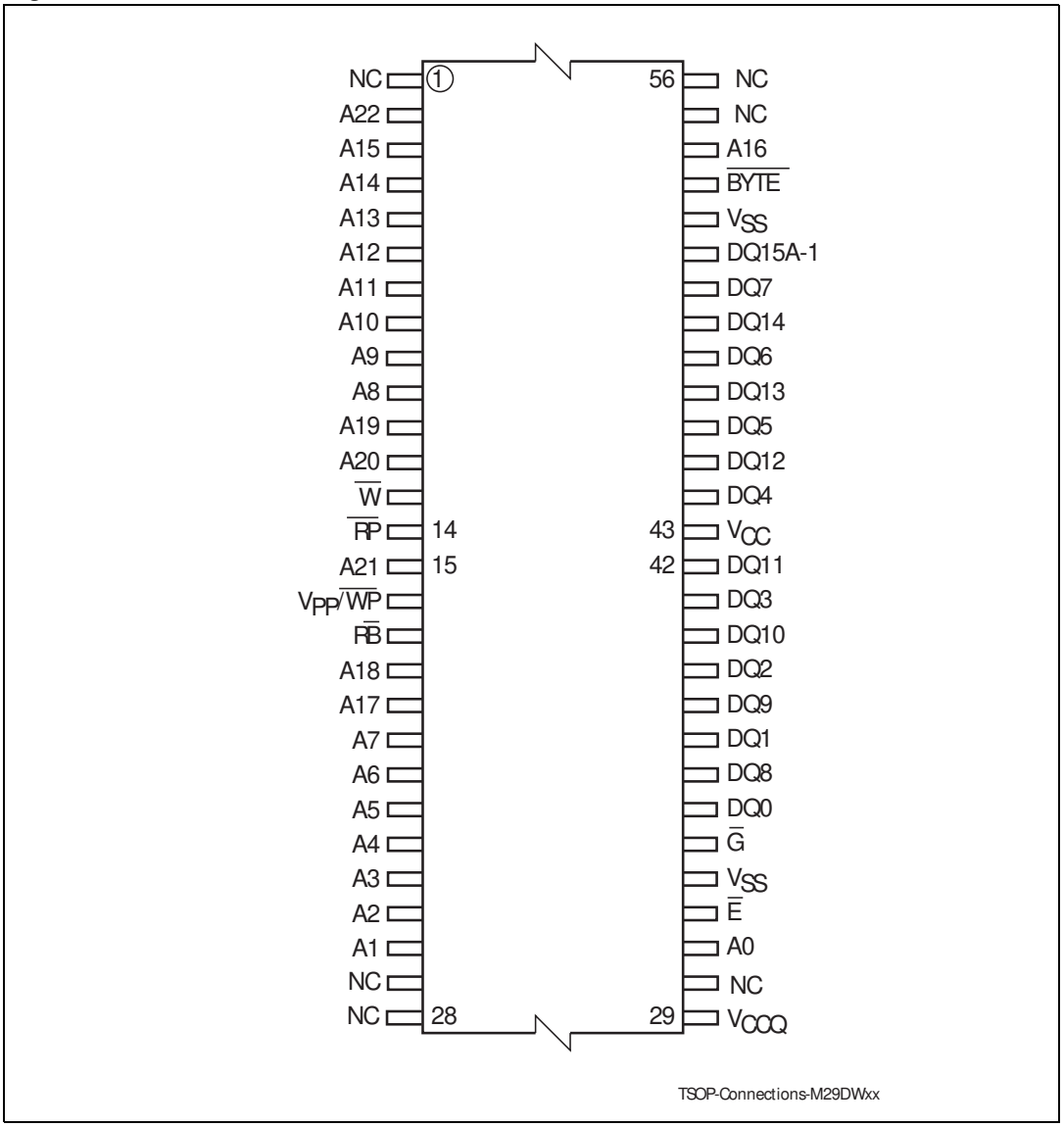


Figure 3. TBGA connections (top view through package)

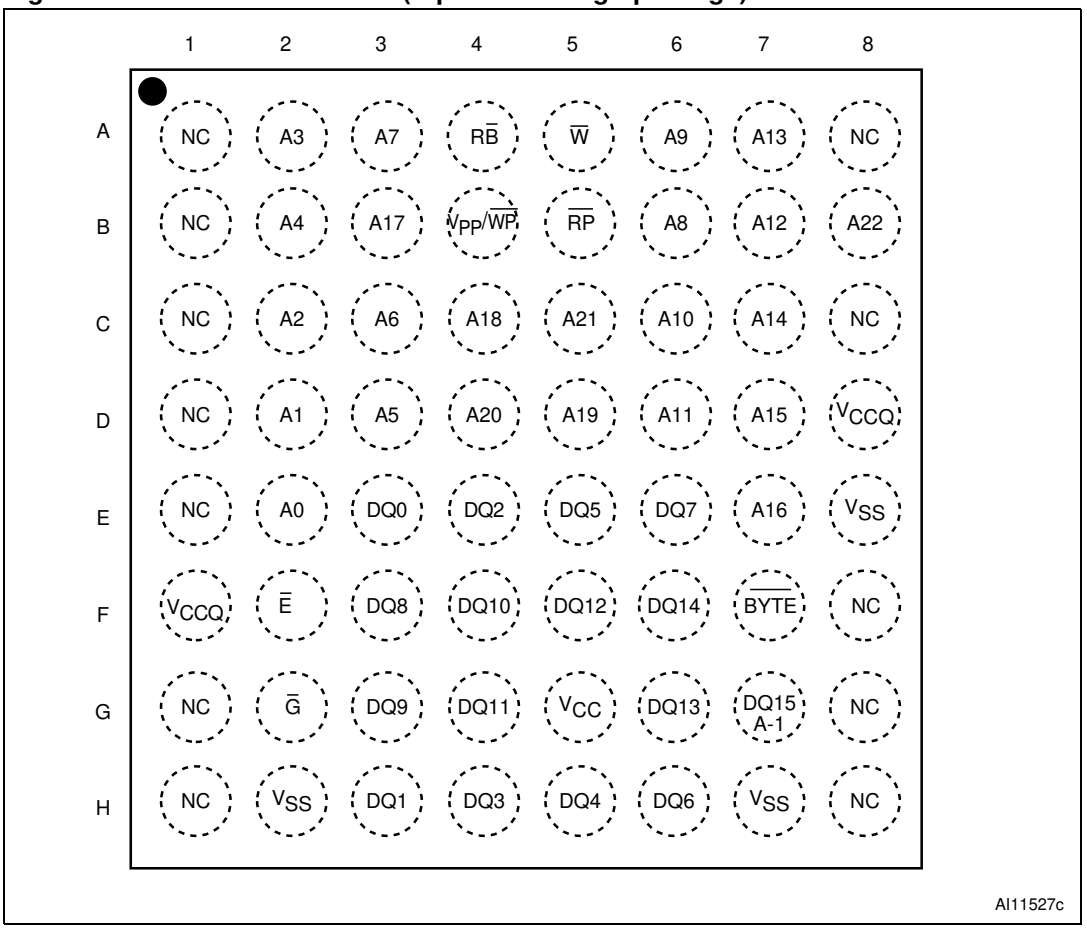


Figure 4. Block addresses (x8 mode)

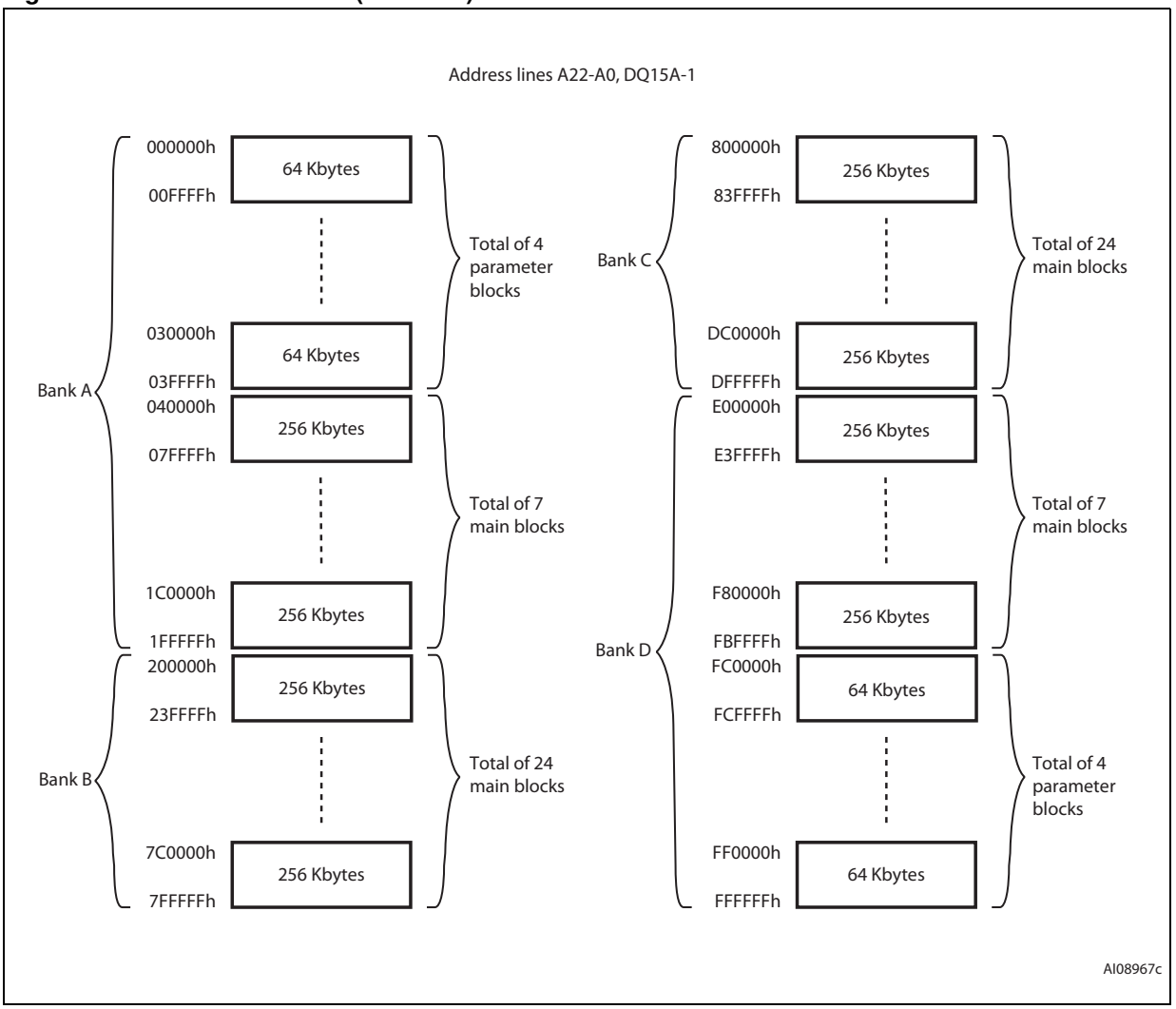
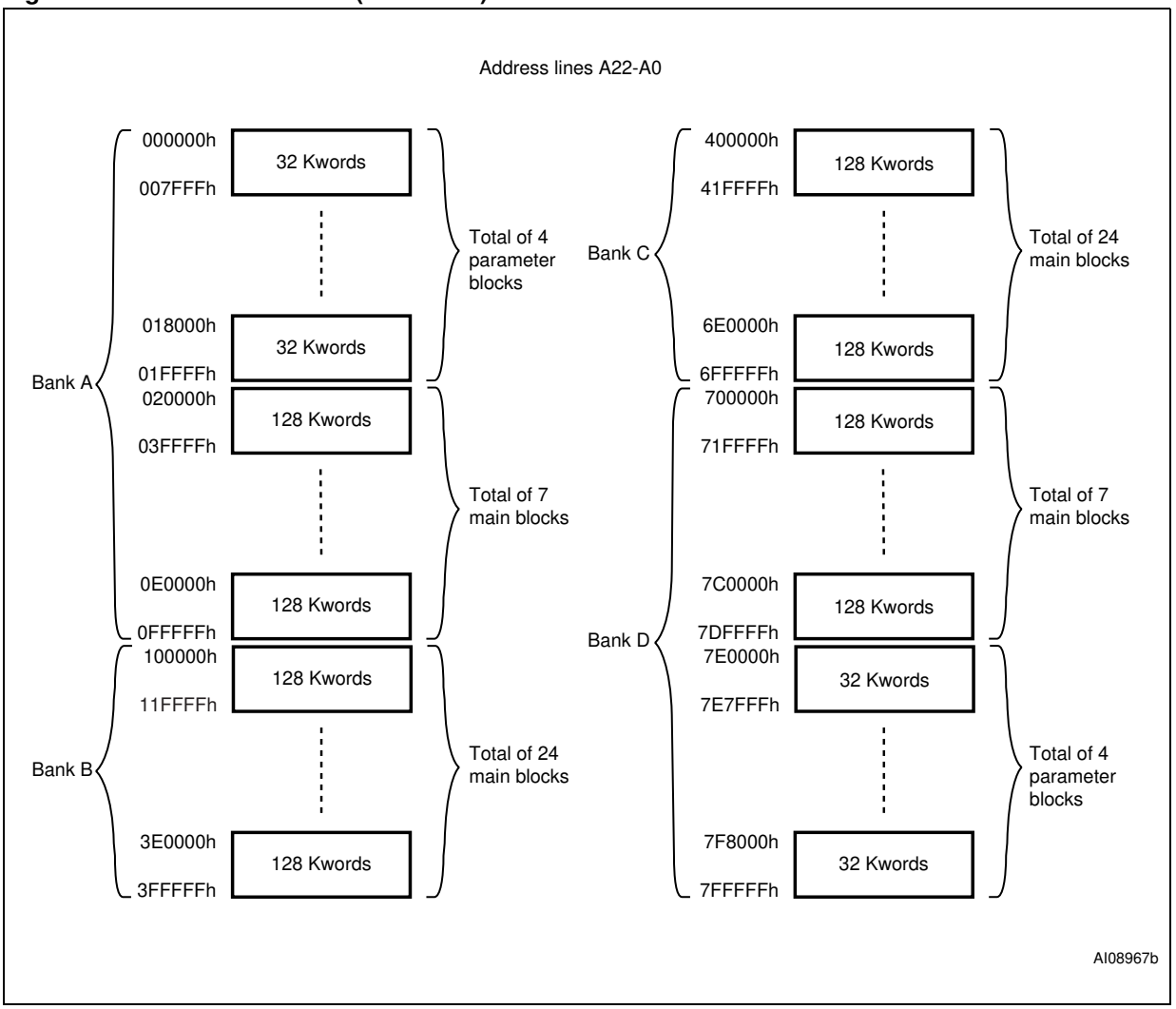


Figure 5. Block addresses (x16 mode)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A22)

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The data I/O outputs the data stored at the selected address during a bus read operation. During bus write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The data I/O outputs the data stored at the selected address during a bus read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During bus write operations the command register does not use these bits. When reading the status register these bits should be ignored.

2.4 Data inputs/outputs or address inputs (DQ15A–1)

When the device is in x 16 bus mode, this pin behaves as a data input/output pin (as DQ8-DQ14). When the device operates in x 8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the data input/output to include this pin when the device operates in x 16 bus mode and references to the address inputs to include this pin when the device operates in x 8 bus mode except when stated explicitly otherwise.

2.5 Chip Enable ($\overline{E}$)

The Chip Enable pin, $\overline{E}$, activates the memory, allowing bus read and bus write operations to be performed. When chip enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable ($\overline{G}$)

The Output Enable pin, $\overline{G}$, controls the bus read operation of the memory.

2.7 Write Enable ($\overline{W}$)

The Write Enable pin, $\overline{W}$, controls the bus write operation of the memory's command interface.

2.8 V_{PP}/write protect ($V_{PP}/\overline{WP}$)

The V_{PP}/write protect pin provides two functions. The V_{PPH} function allows the memory to use an external high voltage power supply to reduce the time required for program operations. This is achieved by bypassing the unlock cycles.

The write protect function provides a hardware method of protecting the four outermost blocks, that is the two 32-kword blocks at the top and the two 32-kword blocks at the bottom of the address space (see *Section 1: Description*). When V_{PP}/write protect is Low, V_{IL}, the 4 outermost blocks are protected. Program and erase operations on this block are ignored while V_{PP}/write protect is Low.

When V_{PP}/write protect is High, V_{IH}, the memory reverts to the previous protection status of the four outermost blocks. Program and erase operations can now modify the data in these blocks unless the blocks are protected using block protection.

When V_{PP}/write protect is raised to V_{PPH} the memory automatically enters the unlock bypass mode (see *Section 7.2.6*).

When V_{PP}/write protect is raised to V_{PPH}, the execution time of the command is lower (see *Table 18: Program, erase times and program, erase endurance cycles*).

When V_{PP}/write protect returns to V_{IH} or V_{IL} normal operation resumes. During unlock bypass program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 25: Accelerated program timing waveforms*).

Never raise V_{PP}/write protect to V_{PPH} from any mode except read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/write protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 28: DC characteristics*).

The V_{PP}/write protect pin may be left floating or unconnected because it features an internal pull-up.

Refer to *Table 3* for a summary of $V_{PP}/\overline{WP}$ functions.

Table 3. $V_{PP}/\overline{WP}$ functions

$V_{PP}/\overline{WP}$	Function
V_{IL}	Four outermost blocks(1) protected.
V_{IH}	Four outermost blocks(1) unprotected unless a software protection is activated (see *Section 5: Hardware protection*).
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming.

1. Two at the top and two at the bottom of the address space.

2.9 Reset ($\overline{RP}$)

The reset pin can be used to apply a hardware reset to the memory.

A hardware reset is achieved by holding reset Low, V_{IL}, for at least t_{PLPX}. After reset goes High, V_{IH}, the memory will be ready for bus read and bus write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/busy output (RB)*, *Table 32: Reset AC characteristics*, *Figure 23* and *Figure 24* for more details.

2.10 Ready/busy output ($\overline{RB}$)

The ready/busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations ready/busy is Low, V_{OL} (see *Table 21: Status register bits*). Ready/busy is high-impedance during read mode, auto select mode and erase suspend mode.

After a hardware reset, bus read and bus write operations cannot begin until ready/busy becomes high-impedance. See *Table 32: Reset AC characteristics*, *Figure 23* and *Figure 24*.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/word organization select ($\overline{BYTE}$)

It is used to switch between the x8 and x16 bus modes of the memory. When byte/word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (read, program and erase).

The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus write operations from accidentally damaging the data during power-up, power-down and power surges. If the program/erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 28: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins both of which must be connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are bus read (random and page modes), bus write, output disable, standby and automatic standby.

Dual operations are possible in the M29DW127G, thanks to its multiple bank architecture. While programming or erasing in one bank, read operations are possible in any of the other banks. Write operations are only allowed in one bank at a time.

See *Table 4: Bus operations, 8-bit mode on page 20* and *Table 5: Bus operations, 16-bit mode on page 20* for a summary. Typical glitches of less than 5 ns on chip enable, write enable, and reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus read

Bus read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in page mode where data is internally read and stored in a page buffer. The page has a size of 8 words (or 16 bytes) and is addressed by the address inputs A2-A0 in x16 mode and A2-A0 plus DQ15A-1 in x8 mode.

A valid bus read operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 14: Random read AC waveforms (8-bit mode) on page 65*, *Figure 15: Random read AC waveforms (16-bit mode) on page 65*, and *Table 29: Read AC characteristics on page 69* for details of when the output becomes valid.

3.2 Bus write

Bus write operations write to the command interface. A valid bus write operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole bus write operation.

For details on AC characteristics (write enabled and chip enabled controlled), see the following figures and tables:

- *Figure 19: Write enable controlled program waveforms (8-bit mode) on page 70*
- *Figure 20: Write enable controlled program waveforms (16-bit mode) on page 71*
- *Table 30: Write AC characteristics, write enable controlled on page 72*
- *Figure 21: Chip enable controlled program waveforms (8-bit mode) on page 73*
- *Figure 22: Chip enable controlled program waveforms (16-bit mode) on page 74*
- *Table 31: Write AC characteristics, chip enable controlled on page 74*

3.3 Output disable

The data inputs/outputs are in the high impedance state when output enable is High, V_{IH}.

3.4 Standby

Driving Chip Enable High, V_{IH}, in read mode, causes the memory to enter standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the supply current to the standby supply current, I_{CC2}, Chip Enable should be held within V_{CC} ± 0.3 V. For the standby current level see *Table 28: DC characteristics*.

During program or erase operations the memory will continue to use the program/erase supply current, I_{CC3}, for program or erase operations until the operation completes.

3.5 Reset

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the standby level, independently from the Chip Enable, Output Enable or Write Enable inputs.

3.6 Automatic standby

Automatic standby allows the memory to achieve low power consumption during read mode.

After a read operation, if CMOS levels (V_{CC} ± 0.3 V) are used to drive the bus and the bus is inactive for t_{AVQV} + 30 ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, I_{CC2} (see *Table 28: DC characteristics*). The data inputs/outputs will still output data if a bus read operation is in progress.

The power supplier of data bus, V_{CCQ}, can have a null consumption (depending on load circuits connected with data bus) when the memory enters automatic standby.

Table 4. Bus operations, 8-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address Inputs	Data inputs/outputs	
						A22-A0, DQ15A-1	DQ14-DQ8	DQ7-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. To write the four outermost parameter blocks (first two and the last two), VPP/WP must be equal to VIH.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Bus operations, 16-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs	Data inputs/outputs
						A22-A0	DQ15A-1, DQ14-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. To write the four outermost parameter blocks (first two and last two), VPP/WP must be equal to VIH.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

4 Auto select mode

The auto select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the extended memory block, and apply/remove block protection. For example, this mode can be used by a programming equipment to automatically match a device and the application code to be programmed.

The auto select mode is entered by issuing the Auto Select command (see *Section 7.1.2: Auto Select command*).

At power-up, the device is in read mode, and can then be put in auto select mode by issuing the Auto Select command.

The device cannot enter auto select mode when a program or erase operation is ongoing ($\overline{RB}$ Low). However, auto select mode can be entered if the erase operation has been suspended by issuing an Erase Suspend command (see *Section 7.1.6*).

The auto select mode is exited by performing a reset. The device is returned to read mode, except if the auto select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the erase or program suspend mode.

4.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 9: Block protection (16-bit mode)* and *Table 6: Read electronic signature, auto select mode method (8-bit mode)* and *Table 7: Read electronic signature, auto select mode method (16-bit mode)*.

4.2 Verify extended memory block protection indicator

The extended memory block is either factory locked or customer lockable.

The protection status of the extended memory block (factory locked or customer lockable) can be accessed by reading the extended memory block protection indicator. See *Table 8: Block protection (8-bit mode)* and *Table 9.: Block protection (16-bit mode)*.

The protection status of the extended memory block is then output on bit DQ7 of the data input/outputs (see *Table 4: Bus operations, 8-bit mode* and *Table 5: Bus operations, 16-bit mode*).

4.3 Verify block protection status

The protection status of a block can be directly accessed by performing a read operation with control signals and addresses set as shown in *Table 8: Block protection (8-bit mode)* and *Table 9: Block protection (16-bit mode)*.

If the block is protected, then 01h is output on data input/outputs DQ0-DQ7, otherwise 00h is output.

Table 6. Read electronic signature, auto select mode method (8-bit mode)

Read cycle[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs		
				A22-A10	A9-A7	A8	A6	A5-A4	A3	A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	20h
Device code (cycle 1)								V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	20h
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	04h

1. X = V_{IL} or V_{IH}. BKA bank address.

Table 7. Read electronic signature, auto select mode method (16-bit mode)

Read cycle[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
				A22-A12	A11-A10	A9	A8	A7-A6	A5-A4	A3	A2	A1	A0	DQ15-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)										V_{IH}	V_{IH}	V_{IH}	V_{IL}	2220h
Device code (cycle 3)										V_{IH}	V_{IH}	V_{IH}	V_{IH}	2204h

1. X = V_{IL} or V_{IH}. BKA bank address.

Table 8. Block protection (8-bit mode)

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs										Data inputs/outputs	
				A22-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Verify extended memory block protection indicator (bit DQ7)	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	X	X	DQ7: 1=factory locked DQ6: 1=customer locked, 0=customer lockable DQ5: 1=reserved, 0=standard DQ4, DQ3-Hardware write protection: 00=WP protects 4 outermost blocks, 11=No WP protection DQ2-DQ0=0
Verify block protection status				BAd								V_{IL}			01h (protected) 00h (unprotected)

1. X = VIL or VIH; BAd = any address in the block; BKA = bank address.

Table 9. Block protection (16-bit mode)

Operation (1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs									Data inputs/outputs
						A22-A12	A11-A10	A9	A8	A7	A6	A5-A4	A3-A2	A1	A0	DQ15-DQ0
Verify extended memory block indicator bit	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	BKA	X	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	DQ15-DQ8=0 DQ7: 1=factory locked DQ6: 1=customer locked, 0=customer lockable DQ5: 1=reserved, 0=standard DQ4, DQ3-Hardware write protection: 00=$\overline{WP}$ protects 4 outermost blocks, 11=No $\overline{WP}$ protection DQ2-DQ0=0
Verify block protection status						BAd									V_{IL}	0000h (unprotected) 0001h (protected)

1. X = V_{IL} or V_{IH}. BAd any address in the block, BKA bank address.

5 Hardware protection

The M29DW127G features hardware protection/unprotection. Refer to *Table 10: Hardware protection* for details on hardware block protection/unprotection using $V_{PP}/\overline{WP}$ and $\overline{RP}$ pins.

5.1 Write protect

The $V_{PP}/\overline{WP}$ pin can be used to protect the four outermost parameter blocks (refer to *Section 2: Signal descriptions* for a detailed description of the signals). When $V_{PP}/\overline{WP}$ is at V_{IL} the four outermost parameter blocks are protected and remain protected regardless of the block protection status or the reset pin state.

Table 10. Hardware protection

$V_{PP}/\overline{WP}$	Function
V_{IL}	4 outermost parameter blocks (first two and last two) protected from program/erase operations
V_{IH}	4 outermost parameter blocks unprotected unless a software activated (see *Section 5: Hardware protection*)
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming

6 Software protection

The M29DW127G has three different software protection modes:

- Volatile protection
- Non-volatile protection
- Password protection

On first use all parts default to operate in non-volatile protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable non-volatile protection mode lock bit or the password protection mode lock bit of the lock register (see *Section 8.1: Lock register*). Programming the non-volatile protection mode lock bit or the password protection mode lock bit to '0' will permanently activate the non-volatile or the password protection mode, respectively. These three bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The non-volatile and password protection modes provide non-volatile protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 7: Read electronic signature, auto select mode method (16-bit mode)*) or by issuing an Auto Select command (see *Table 20: Block protection status*).

For the four outermost blocks (that is the two blocks at the top and the two at the bottom of the address space), an even higher level of block protection can be achieved by locking the blocks using the non-volatile protection and then by holding the $V_{PP}/\overline{WP}$ pin Low.

6.1 Volatile protection mode

The volatile protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile protection bits, NVPBs, cleared (erased to '1') (see *Section 6.2: Non-volatile protection mode* and *Section 7.3.5: Non-volatile protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to '0') or cleared (erased to '1'), thus placing each block in the protected or unprotected state respectively. The VPBs can be set (programmed to '0') or cleared (erased to '1') as often as needed.

The default values of the volatile protections are set through the VLBB (volatile lock boot bit) of the lock register (see *Table 19: Lock register bits*).