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Micron Parallel NOR Flash Embedded Memory

M29DW256G X16 Multiple Bank, Page, Dual Boot 3V Supply Flash Memory

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
  - V_{PPH} = 9V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8 words
  - Page access: 25ns, 30ns
  - Random access: 70ns, 80ns
- Fast program commands: 32-word
- Enhanced buffered program commands: 256-word
- Program time
  - 16µs per byte/word TYP
  - Chip program time: 10 s with V_{PPH} and 16s without V_{PPH}
- Memory organization
  - Quadruple bank memory array: 32Mb + 96Mb + 96Mb + 32Mb with parameter blocks at top and bottom
  - Dual operation: program/erase in one bank while reading in any other bank
- Program/erase controller
  - Embedded word program algorithms
- Program/erase suspend and resume capability
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, write to buffer, and enhanced buffer program commands
  - Fast buffered/batch programming
  - Fast block/chip erase
- V_{PP}/WP# pin for fast program and write
  - Protects the four outermost parameter blocks
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - Programmed or locked at the factory or by the customer
  - 128 word factory locked and 128 word customer lockable
- Common flash interface
  - 64-bit security code
- Low power consumption: standby and automatic mode
- 100,000 minimum PROGRAM/ERASE cycles per block
- Data retention: 20 years (TYP)
- Fortified BGA, TBGA, and TSOP packages
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Automotive certified parts available
  - Automotive device grade: temperature –40°C to +85°C (automotive grade certified)
- Root part number
  - M29DW256G
- Device code
  - 227Eh + 223Ch + 2202h

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Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details	Notes
Device Type	M29	
Architecture	D = Dual operation	
Operating Voltage	W = VCC = 2.7 to 3.6V	
Device function	256G = 256Mb (x16) page, dual boot	
Speed	70 = 70ns	1, 2
	7A = 70ns	1, 2
Package	NF = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant	
	ZA = 64-pin TBGA, 10mm x 13mm, lead-free, halogen-free, RoHS-compliant	
	ZS = 64-pin Fortified BGA, 11mm x 13mm, lead-free, halogen-free, RoHS-compliant	
Temperature Range	1 = 0 to 70°C	
	6 = –40°C to +85°C	
Shipping Options	E = RoHS-compliant package, standard packing	
	F = RoHS-compliant package, tape and reel packing	

Notes: 1. 80ns if VCCQ = 1.65V to VCC.
2. Automotive certified –40°C to +85°C, available only with option 6.

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Description

The M29DW256G is a 256Mb (16Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. At power-up the memory defaults to its read mode.

The M29DW256G features an asymmetrical block architecture, with 8 parameter and 126 main blocks, divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank. Four of the parameter blocks are at the top of the memory address space, and four are at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operations of the memory. They allow simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the memory array. The device also features a write to buffer program capability that improves the programming throughput by programming 32 words in one instance. The enhanced buffered program feature is also available to speed up programming throughput, allowing 256 words to be programmed at once. The V_{PP}/WP# signal can be used to enable faster programming of the device.

The M29DW256G has one extra 256-word extended block that can be accessed using a dedicated command: 128-Word factory locked and 128-Word customer lockable. The extended block can be protected and so is useful for storing security information. However the protection is irreversible; once protected the protection cannot be undone.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection: V_{PP}/WP# provides hardware protection on four outermost parameter blocks (two at the top and two at the bottom of the address space)
- Software protection: Volatile protection, nonvolatile protection, password protection

The memory is offered in TSOP56 (14mm x 20mm), TBGA64 (10mm x 13mm, 1mm pitch), and FBGA (11mm x 13mm) packages. The memory is delivered with all the bits erased (set to ‘1’).

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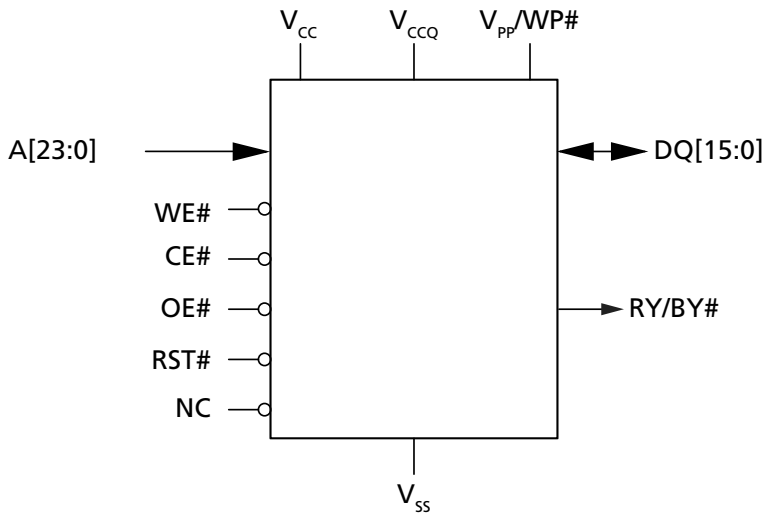
Signals

Table 2: Signal names

Name	Description	Direction
A[23:0]	Address inputs	Inputs
DQ[15:0]	Data inputs/outputs	I/O
CE#	Chip enable	Input
OE#	Output enable	Input
WE#	Write enable	Input
RST#	Reset	Input
RY/BY#	Ready/busy output	Output
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
V_{PP}/WP#	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

Note: 1. [1] V_{PP}/WP# may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

Figure 1: Logic diagram



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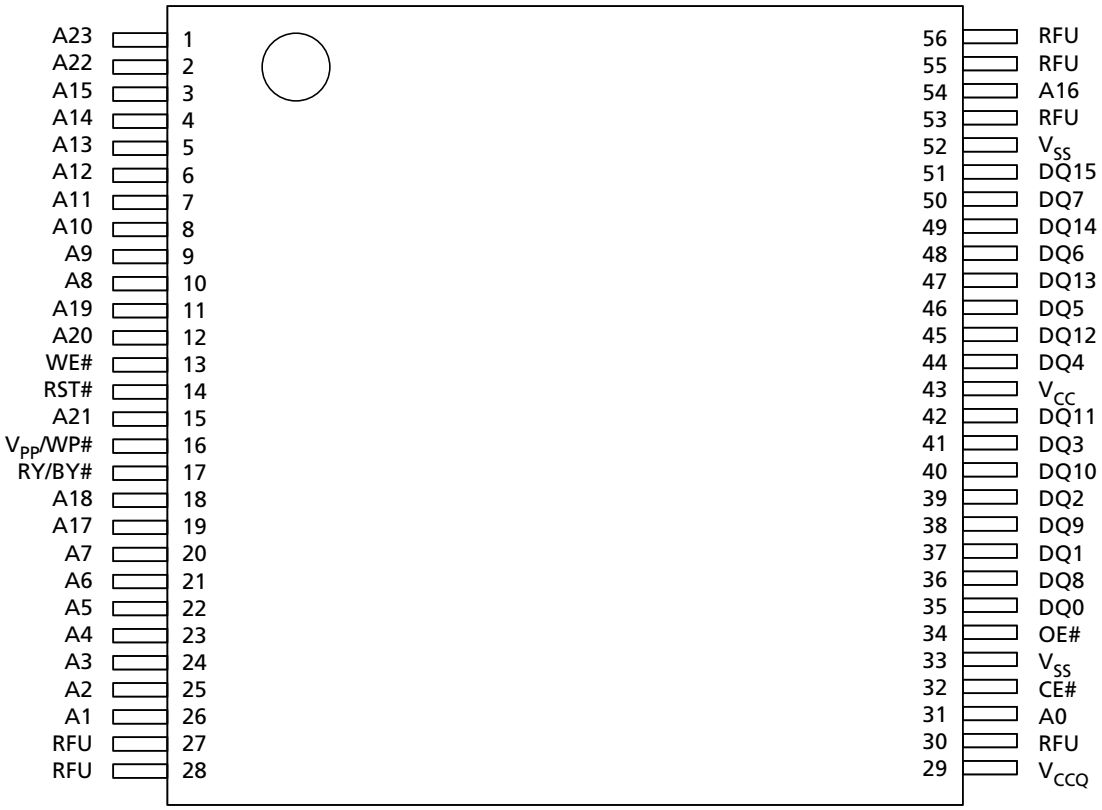
Signal Assignments

Figure 2: 56-Pin TSOP (Top View)



Note: 1. A[23] = A[MAX].

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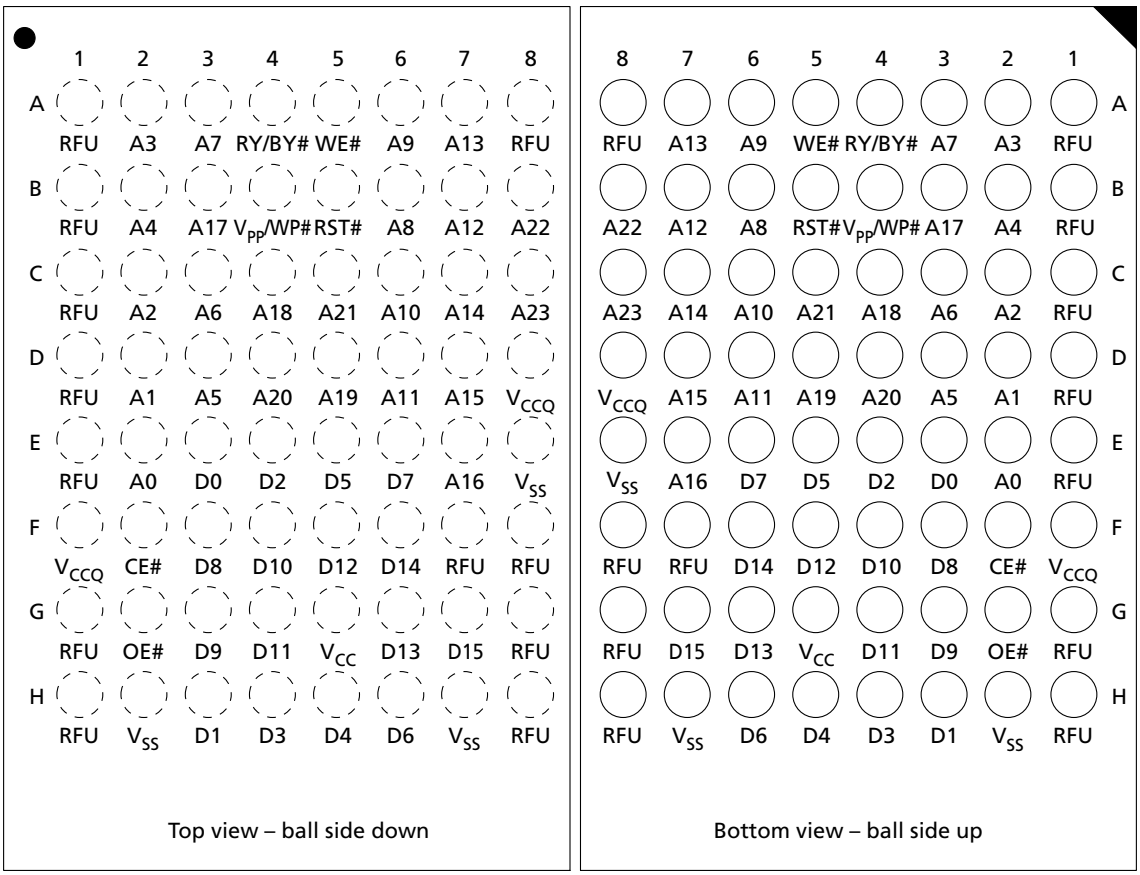
Figure 3: 64-Pin Fortified BGA and 64-Pin TBGA



Note: 1. A[23] = A[MAX].

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Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 3: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
DQ[15:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine. During WRITE operations, bits DQ[15:8] are not used. When reading the status register, these bits should be ignored.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at HIGH-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides two functions. The V_{PPH} function enables the device to bypass unlock cycles and use an external high voltage power supply to reduce time required for PROGRAM operations. Second, When V_{PP}/WP# is LOW, the four outermost blocks of the address space (two 32KW blocks at the top and two 32KW blocks at the bottom) are protected; PROGRAM and ERASE operations are ignored and the blocks remain protected regardless of the block protection status or the RST# pin state. When V_{PP}/WP# is HIGH, the memory reverts to the previous protection status for those blocks (Refer to Hardware Protection and Bypass Operations for details).
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details). The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one or more of the devices is busy.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).

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Table 3: Signal Descriptions (Continued)

Name	Type	Description
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

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Memory Organization

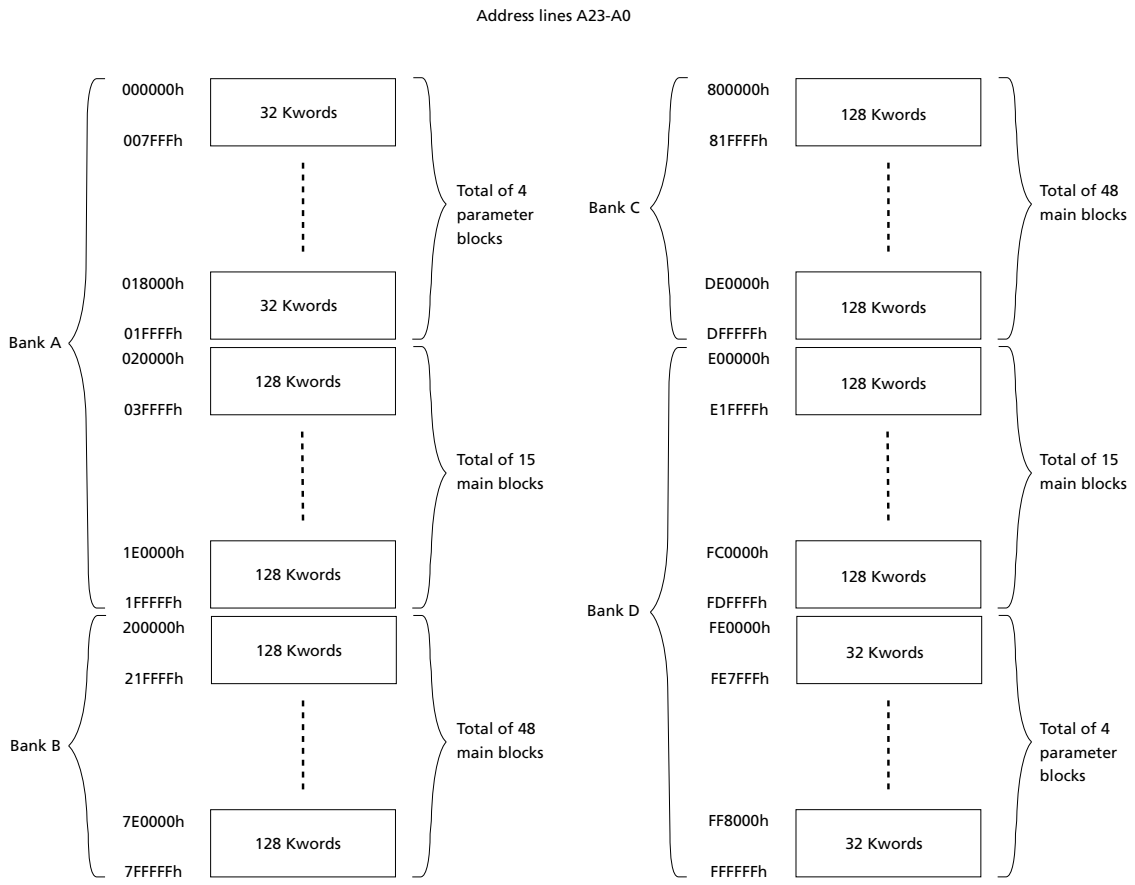
Memory Configuration

The M29DW256G features an asymmetrical block architecture, with 8 parameter and 126 main blocks, divided into four banks providing multiple bank operations. Four parameter blocks are at the top of the memory address space, and four are at the bottom.

Table 4: Bank architecture

Bank	Bank Size	Parameter Blocks		Main Blocks	
		Number of Blocks	Block Size	Number of Blocks	Block Size
A	32Mb	4	32 Kwords	15	128 Kwords
B	96Mb	—	—	48	128 Kwords
C	96Mb	—	—	48	128 Kwords
D	32Mb	4	32 Kwords	15	128 Kwords

Figure 4: Block Addresses



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Block Addresses and Protection Groups

Table 5: Bank A

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
0	Protection Group	32	0000000 - 0007FFF
1	Protection Group	32	0008000 - 000FFFF
2	Protection Group	32	0010000 - 0017FFF
3	Protection Group	32	0018000 - 001FFFF
4	Protection Group	128	0020000 - 003FFFF
5	Protection Group	128	0040000 - 005FFFF
6	Protection Group	128	0060000 - 007FFFF
7	Protection Group	128	0080000 - 009FFFF
8	Protection Group	128	00A0000 - 00BFFFF
9	Protection Group	128	00C0000 - 00DFFFF
10	Protection Group	128	00E0000 - 00FFFFF
11	Protection Group	128	0100000 - 011FFFF
12	Protection Group	128	0120000 - 013FFFF
13	Protection Group	128	0140000 - 015FFFF
14	Protection Group	128	0160000 - 017FFFF
15	Protection Group	128	0180000 - 019FFFF
16	Protection Group	128	01A0000 - 01BFFFF
17	Protection Group	128	01C0000 - 01DFFFF
18	Protection Group	128	01E0000 - 01FFFFF

Table 6: Bank B

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
19	Protection Group	128	0200000 - 021FFFF
20	Protection Group	128	0220000 - 023FFFF
21	Protection Group	128	0240000 - 025FFFF
22	Protection Group	128	0260000 - 027FFFF
23	Protection Group	128	0280000 - 029FFFF
24	Protection Group	128	02A0000 - 02BFFFF
25	Protection Group	128	02C0000 - 02DFFFF
26	Protection Group	128	02E0000 - 02FFFFF
27	Protection Group	128	0300000 - 031FFFF
28	Protection Group	128	0320000 - 033FFFF
29	Protection Group	128	0340000 - 035FFFF
30	Protection Group	128	0360000 - 037FFFF
31	Protection Group	128	0380000 - 039FFFF
32	Protection Group	128	03A0000 - 03BFFFF

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Table 6: Bank B (Continued)

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
33	Protection Group	128	03C0000 - 03DFFFF
34	Protection Group	128	03E0000 - 03FFFFF
35	Protection Group	128	0400000 - 041FFFF
36	Protection Group	128	0420000 - 043FFFF
37	Protection Group	128	0440000 - 045FFFF
38	Protection Group	128	0460000 - 047FFFF
39	Protection Group	128	0480000 - 049FFFF
40	Protection Group	128	04A0000 - 04BFFFF
41	Protection Group	128	04C0000 - 04DFFFF
42	Protection Group	128	04E0000 - 04FFFFF
43	Protection Group	128	0500000 - 051FFFF
44	Protection Group	128	0520000 - 053FFFF
45	Protection Group	128	0540000 - 055FFFF
46	Protection Group	128	0560000 - 057FFFF
47	Protection Group	128	0580000 - 059FFFF
48	Protection Group	128	05A0000 - 05BFFFF
49	Protection Group	128	05C0000 - 05DFFFF
50	Protection Group	128	05E0000 - 05FFFFF
51	Protection Group	128	0600000 - 061FFFF
52	Protection Group	128	0620000 - 063FFFF
53	Protection Group	128	0640000 - 065FFFF
54	Protection Group	128	0660000 - 067FFFF
55	Protection Group	128	0680000 - 06FFFFF
56	Protection Group	128	06A0000 - 06BFFFF
57	Protection Group	128	06C0000 - 06DFFFF
58	Protection Group	128	06E0000 - 06FFFFF
59	Protection Group	128	0700000 - 071FFFF
60	Protection Group	128	0720000 - 073FFFF
61	Protection Group	128	0740000 - 075FFFF
62	Protection Group	128	0760000 - 077FFFF
63	Protection Group	128	0780000 - 079FFFF
64	Protection Group	128	07A0000 - 07BFFFF
65	Protection Group	128	07C0000 - 07DFFFF
66	Protection Group	128	07E0000 - 07FFFFF

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Table 7: Bank C

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
67	Protection Group	128	0800000 - 081FFFF
68	Protection Group	128	0820000 - 083FFFF
69	Protection Group	128	0840000 - 085FFFF
70	Protection Group	128	0860000 - 087FFFF
71	Protection Group	128	0880000 - 089FFFF
72	Protection Group	128	08A0000 - 08BFFFF
73	Protection Group	128	08C0000 - 08DFFFF
74	Protection Group	128	08E0000 - 08FFFFF
75	Protection Group	128	0900000 - 091FFFF
76	Protection Group	128	0920000 - 093FFFF
77	Protection Group	128	0940000 - 095FFFF
78	Protection Group	128	0960000 - 097FFFF
79	Protection Group	128	0980000 - 099FFFF
80	Protection Group	128	09A0000 - 09BFFFF
81	Protection Group	128	09C0000 - 09DFFFF
82	Protection Group	128	09E0000 - 09FFFFF
83	Protection Group	128	0A00000 - 0A1FFFF
84	Protection Group	128	0A20000 - 0A3FFFF
85	Protection Group	128	0A40000 - 0A5FFFF
86	Protection Group	128	0A60000 - 0A7FFFF
87	Protection Group	128	0A80000 - 0A9FFFF
88	Protection Group	128	0AA0000 - 0ABFFFF
89	Protection Group	128	0AC0000 - 0ADFFFF
90	Protection Group	128	0AE0000 - 0AFFFFF
91	Protection Group	128	0B00000 - 0B1FFFF
92	Protection Group	128	0B20000 - 0B3FFFF
93	Protection Group	128	0B40000 - 0B5FFFF
94	Protection Group	128	0B60000 - 0B7FFFF
95	Protection Group	128	0B80000 - 0B9FFFF
96	Protection Group	128	0BA0000 - 0BBFFFF
97	Protection Group	128	0BC0000 - 0BDFFFF
98	Protection Group	128	0BE0000 - 0BFFFFF
99	Protection Group	128	0C00000 - 0C1FFFF
100	Protection Group	128	0C20000 - 0C3FFFF
101	Protection Group	128	0C40000 - 0C5FFFF
102	Protection Group	128	0C60000 - 0C7FFFF
103	Protection Group	128	0C80000 - 0CFFFFF
104	Protection Group	128	0CA0000 - 0CBFFFF

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Table 7: Bank C (Continued)

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
105	Protection Group	128	0CC0000 - 0CDFFFF
106	Protection Group	128	0CE0000 - 0CFFFFF
107	Protection Group	128	0D00000 - 0D1FFFF
108	Protection Group	128	0D20000 - 0D3FFFF
109	Protection Group	128	0D40000 - 0D5FFFF
110	Protection Group	128	0D60000 - 0D7FFFF
111	Protection Group	128	0D80000 - 0D9FFFF
112	Protection Group	128	0DA0000 - 0DBFFFF
113	Protection Group	128	0DC0000 - 0DDFFFF
114	Protection Group	128	0DE0000 - 0DFFFFF

Table 8: Bank D

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
115	Protection Group	128	E00000h-E1FFFFh
116	Protection Group	128	E20000h-E3FFFFh
117	Protection Group	128	E40000h-E5FFFFh
118	Protection Group	128	E60000h-E7FFFFh
119	Protection Group	128	E80000h-E9FFFFh
120	Protection Group	128	EA0000h-EBFFFFh
121	Protection Group	128	EC0000h-EDFFFFh
122	Protection Group	128	EE0000h-EFFFFFh
123	Protection Group	128	F00000h-F1FFFFh
124	Protection Group	128	F20000h-F3FFFFh
125	Protection Group	128	F40000h-F5FFFFh
126	Protection Group	128	F60000h-F7FFFFh
127	Protection Group	128	F80000h-F9FFFFh
128	Protection Group	128	FA0000h-FBFFFFh
129	Protection Group	128	FC0000h-FDFFFFh
130	Protection Group	32	FE0000h-FE7FFFh
131	Protection Group	32	FE8000h-FEFFFFh
132	Protection Group	32	FF0000h-FF7FFFh
133	Protection Group	32	FF8000h-FFFFFFh

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Bus Operations

Table 9: Bus Operations

Notes 1 through 3 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs A[MAX], A[0]	Data Inputs/ Outputs DQ[15:0]
READ	L	L	H	H	X	Cell address	Data output
WRITE	L	H	L	H	X[4]	Command address	Data input[5]
STANDBY	H	X	X	H	X	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z
RESET	X	X	X	L	X	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. Dual operations are possible with the device multiple bank architecture. While programming or erasing in one bank, read operations are possible in any of the other banks. Write operations are only allowed in one bank at a time.
4. To write the four outermost parameter blocks (first two and the last two) V_{PP}/WP# must be equal to V_{IH}.
5. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer. Page size is 8 words and is addressed by address inputs A[2:0].

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Standby and Automatic Standby

Driving CE# HIGH in read mode causes the device to enter standby, and data I/Os to be High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.3V. (See DC Characteristics.)

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During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic standby allows the memory to achieve low power consumption during read mode. After a READ operation, if CMOS levels (VCC ± 0.3 V) are used to drive the bus and the bus is inactive for tAVQV + 30ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, ICC2 (see DC characteristics). The data inputs/outputs still output data if a READ operation is in progress. Depending on load circuits connected with data bus, VCCQ, can have a null consumption when the memory enters automatic standby.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

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Registers

Status Register

Table 10: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM or ERASE operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.

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6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

Table 11: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	No toggle	0	0	2
PROGRAM during ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	–	0	
ENHANCED BUFFERED PROGRAM Entry	Any address	–	Toggle	0	–	–	–	0	
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	0	2
PROGRAM error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
ERASE SUSPEND	Erasing block	1	No toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode					–	High-Z	
BLOCK ERASE error	Good block address	0	Toggle	1	1	No toggle	–	High-Z	
	Faulty block address	0	Toggle	1	1	Toggle	–	High-Z	

Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

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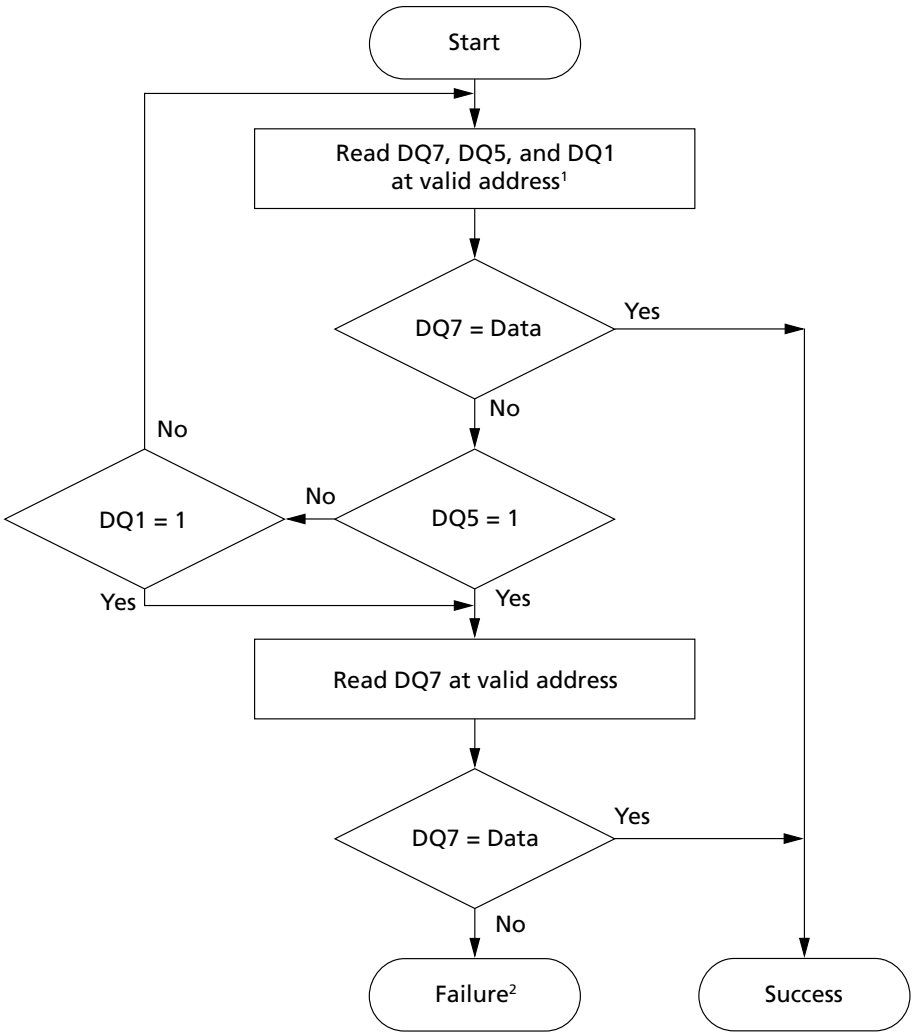
Figure 5: Data Polling Flowchart



Notes:
1. Valid address is the address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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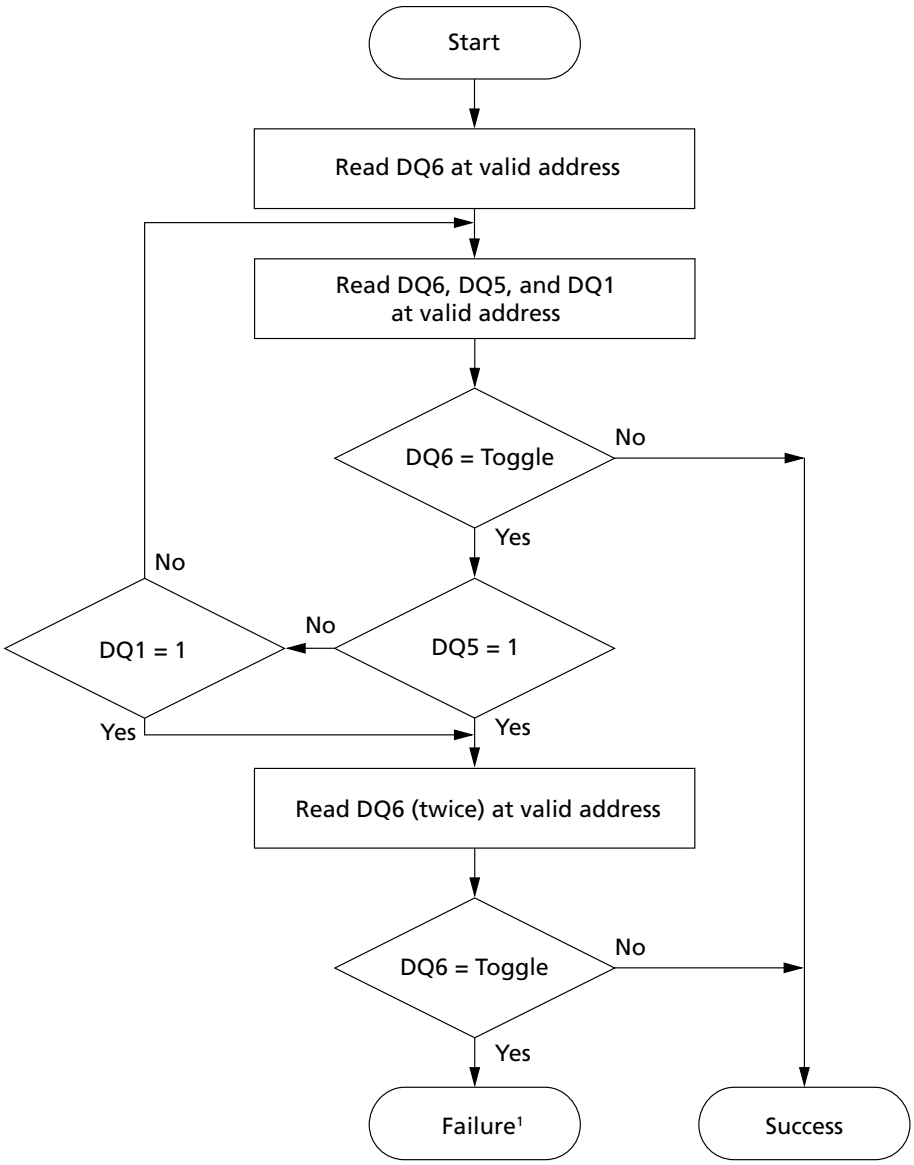
Figure 6: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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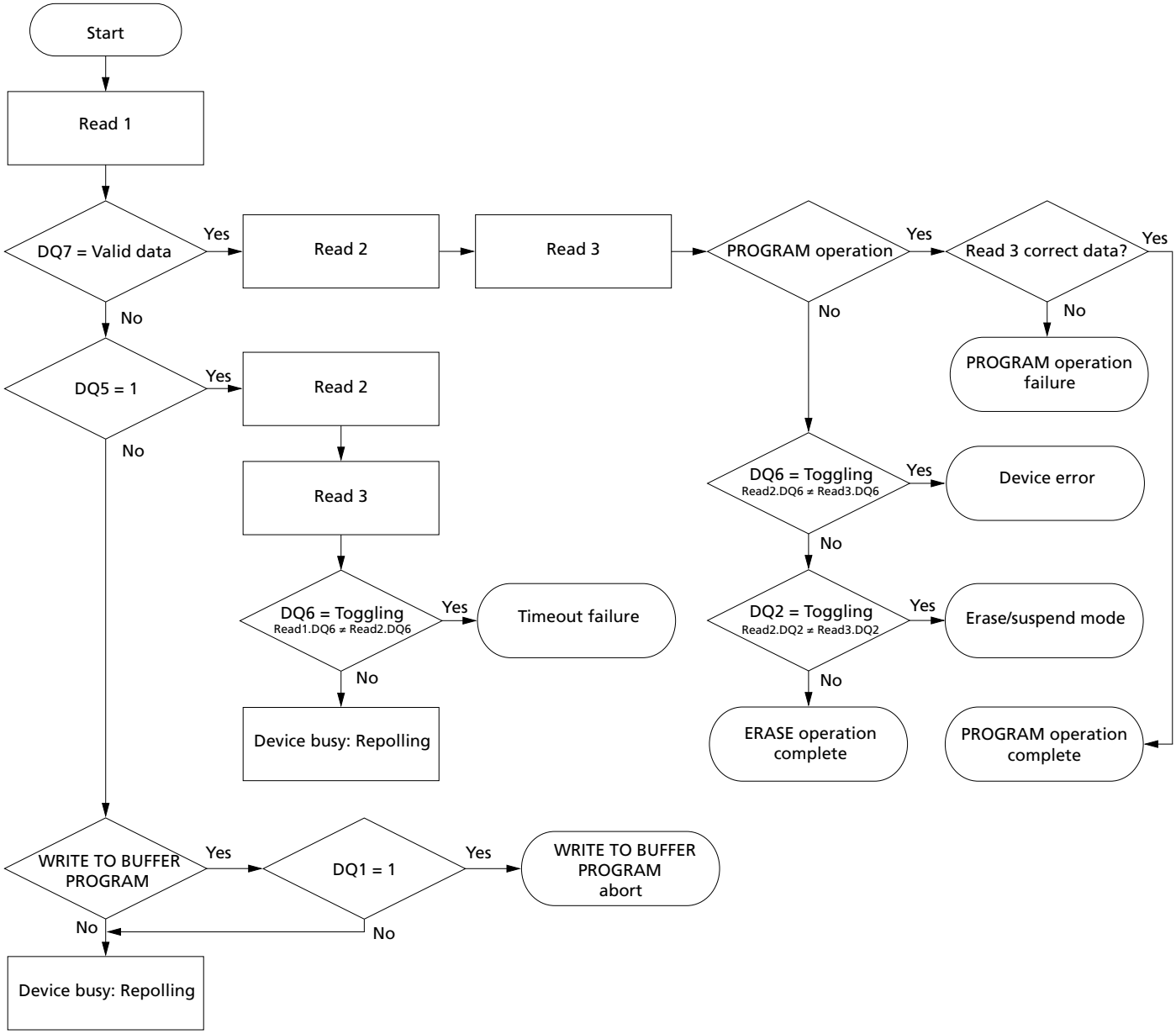
Figure 7: Status Register Polling Flowchart



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Lock Register

Table 12: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ[15:5]	RFU	–	Reserved for future use	2
DQ4	Volatile lock boot bit	Programmable	Sets default values for volatile block protection; when this bit is programmed, blocks are protected at power-up.	
DQ3	RFU	–	Reserved for future use	2
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	3
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	3
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command. It can also be read by applying V_{ID} to A9.	

Notes:
1. The lock register is a 16-bit, one-time programmable register.
2. DQ[15:5] and DQ[3] are reserved and are set to a default value of 1. During programming, they must be held to 1.
3. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Table 13: Block Protection Status

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
0	0	X	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
1	0	X	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.

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