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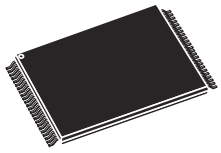
M29DW323DT
M29DW323DB

32 Mbit (4Mb x8 or 2Mb x16, Dual Bank 8:24, Boot Block) 3V Supply Flash Memory

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
  - V_{PP} =12V for Fast Program (optional)
- ACCESS TIME: 70ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
  - Double Word/ Quadruple Byte Program
- MEMORY BLOCKS
  - Dual Bank Memory Array: 8Mbit+24Mbit
  - Parameter Blocks (Top or Bottom Location)
- DUAL OPERATIONS
  - Read in one bank while Program or Erase in other
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- $V_{PP}/\overline{WP}$ PIN for FAST PROGRAM and WRITE PROTECT
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- EXTENDED MEMORY BLOCK
  - Extra block used as security block or to store additional information
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29DW323DT: 225Eh
  - Bottom Device Code M29DW323DB: 225Fh

Figure 1. Packages



TSOP48 (N)
12 x 20mm

TFBGA48 (ZE)
6 x 8mm

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SUMMARY DESCRIPTION

The M29DW323D is a 32 Mbit (4Mb x8 or 2Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode.

The device features an asymmetrical block architecture. The M29DW323D has an array of 8 parameter and 63 main blocks and is divided into two Banks, A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible in Bank B and vice versa. Only one bank at a time is allowed to be in program or erase mode. The bank architecture is summarized in Table 2. M29DW323DT locates the Parameter Blocks at the top of the memory address space while the M29DW323DB locates the Parameter Blocks starting from the bottom.

M29DW323D has an extra 32 KWord (x16 mode) or 64 KByte (x8 mode) block, the Extended Block, that can be accessed using a dedicated command. The Extended Block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently so it is possible to preserve valid data while old data is erased. The blocks can be protected to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12x20mm), and TFBGA48 (6x8mm, 0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

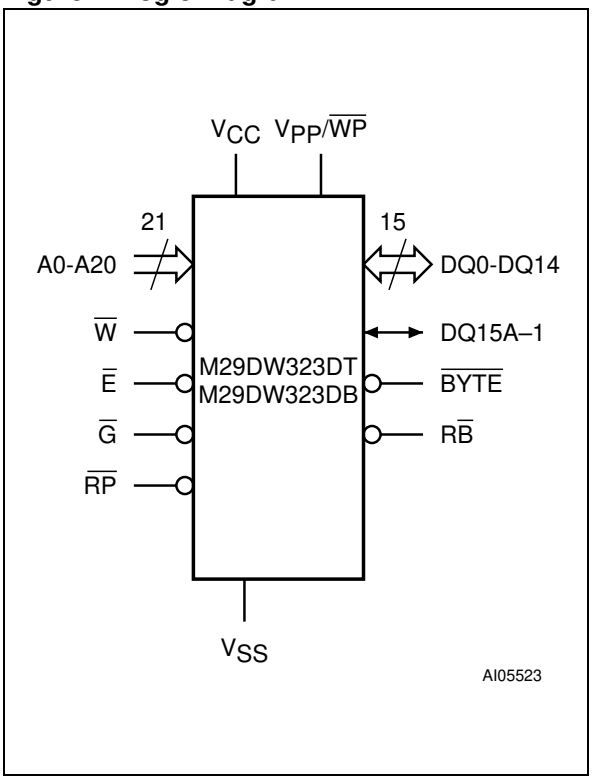


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
$V_{PP}/\overline{WP}$	V_{PP}/Write Protect
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

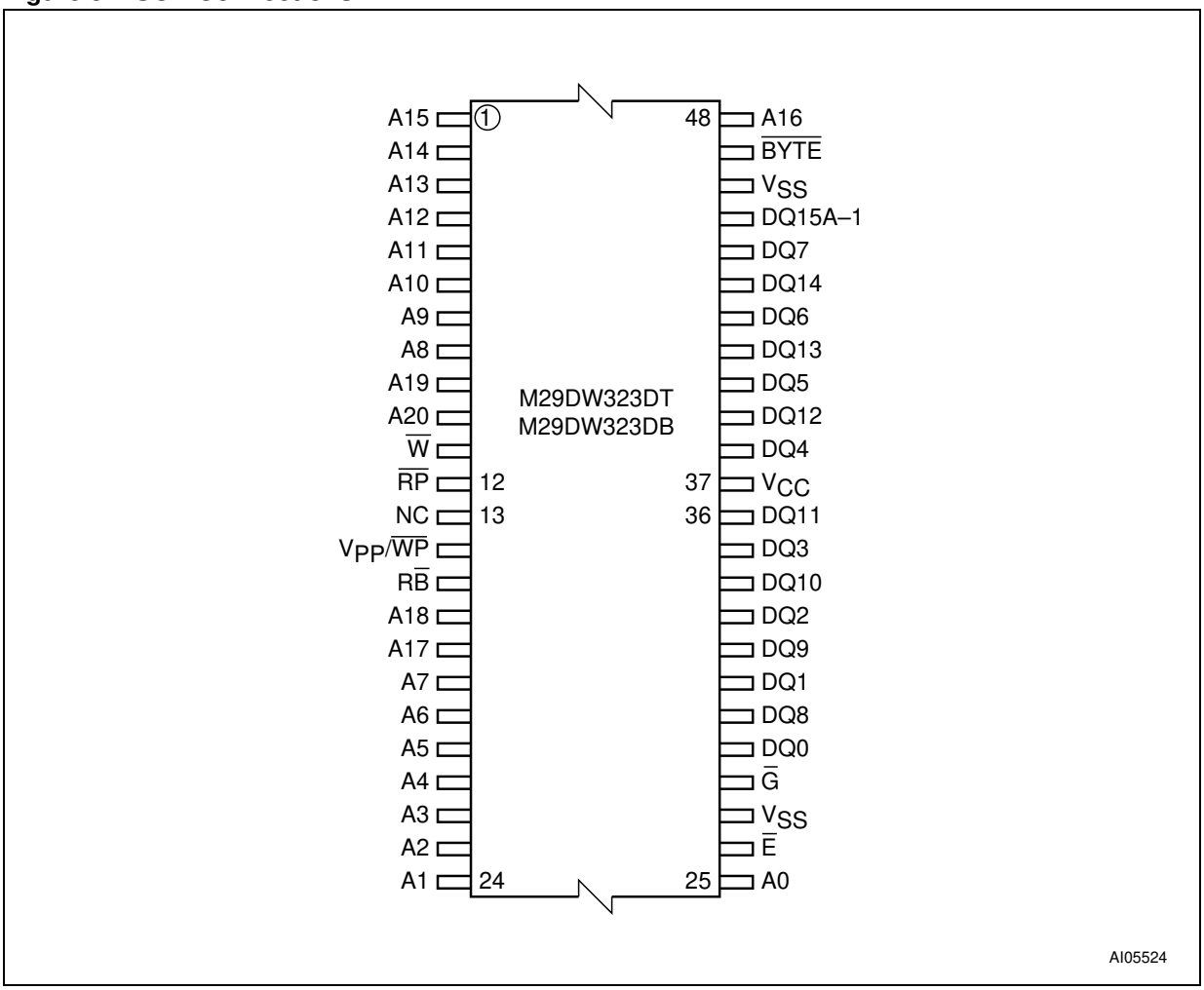


Figure 4. TFBGA48 Connections (Top view through package)

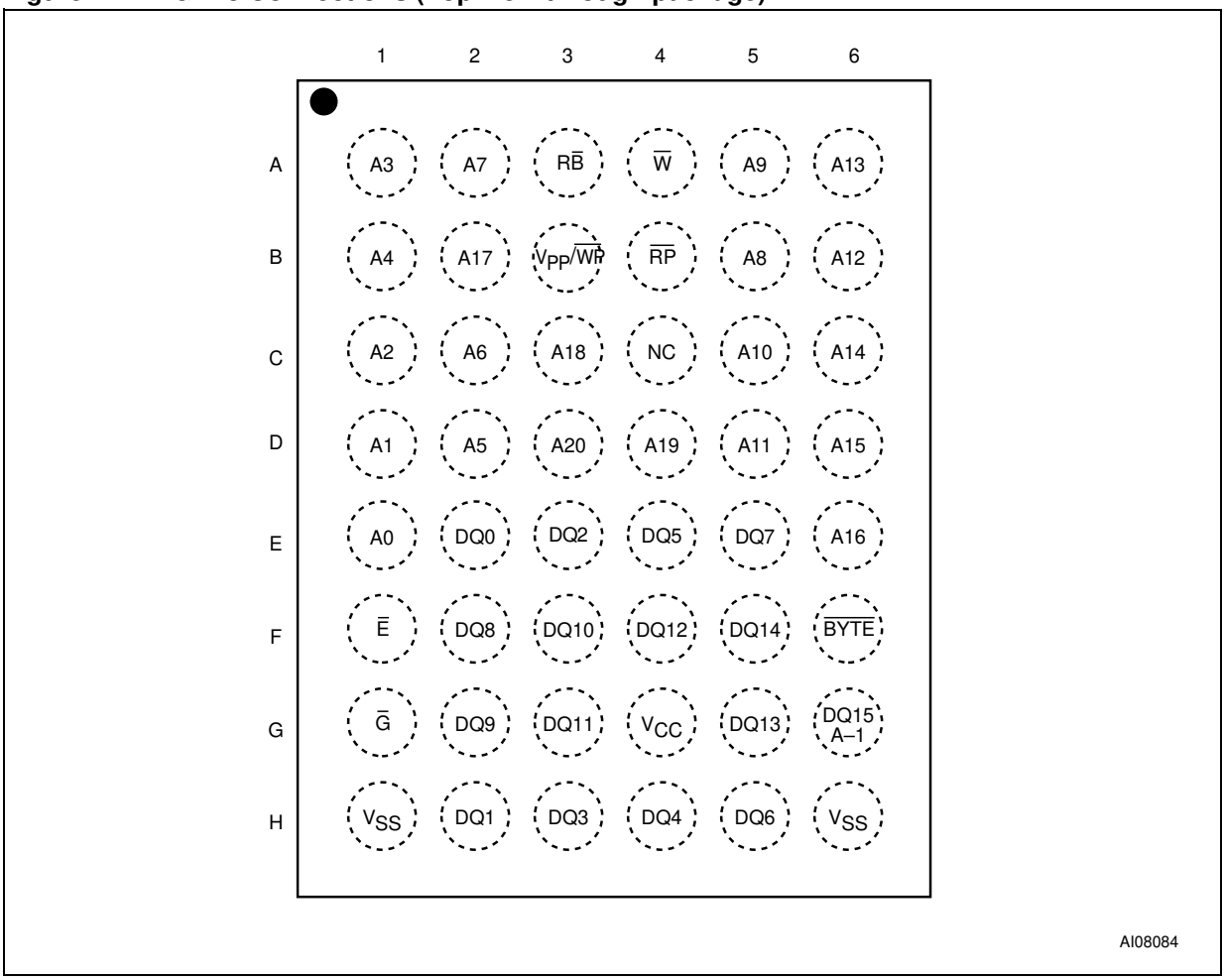
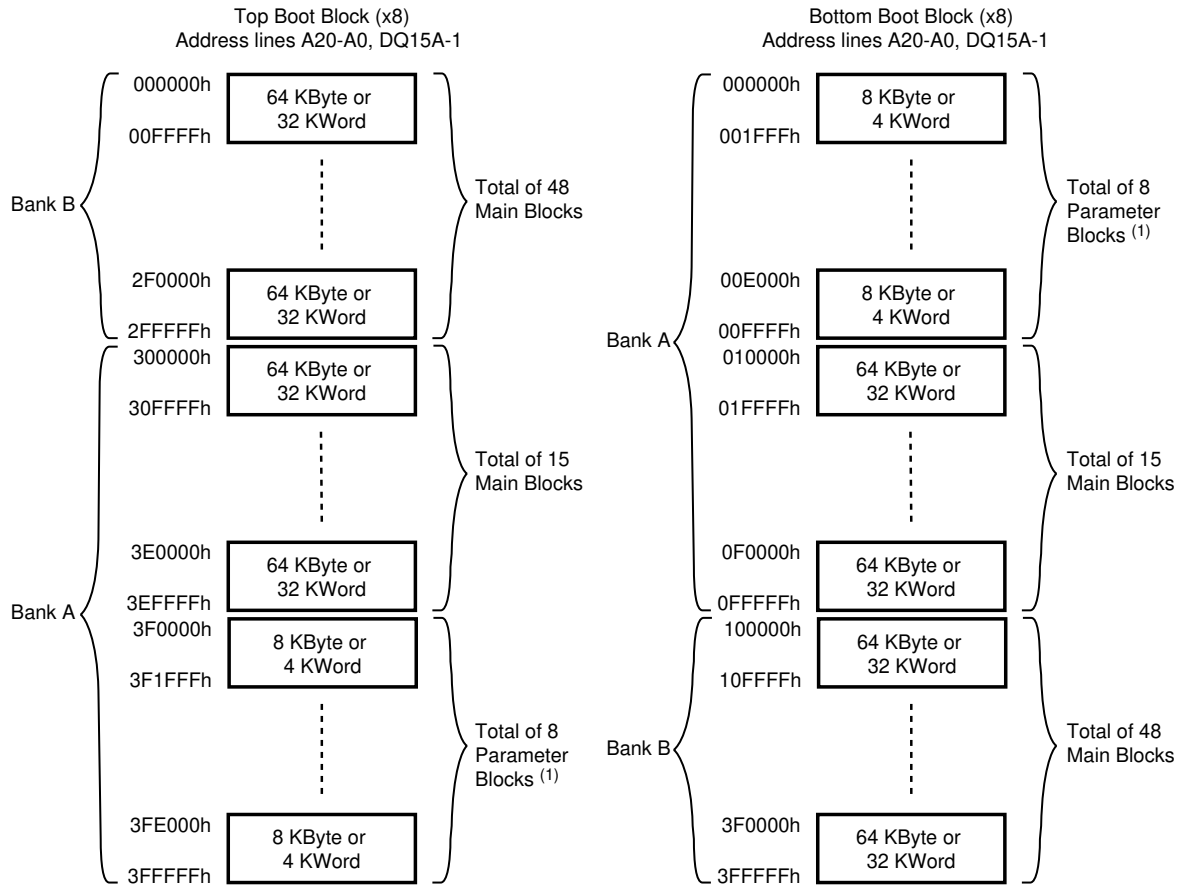


Table 2. Bank Architecture

Bank	Bank Size	Parameter Blocks		Main Blocks	
		No. of Blocks	Block Size	No. of Blocks	Block Size
A	8 Mbit	8	8KByte/ 4 KWord	15	64KByte/ 32 KWord
B	24 Mbit	-		48	64KByte/ 32 KWord

Figure 5. Block Addresses (x8)

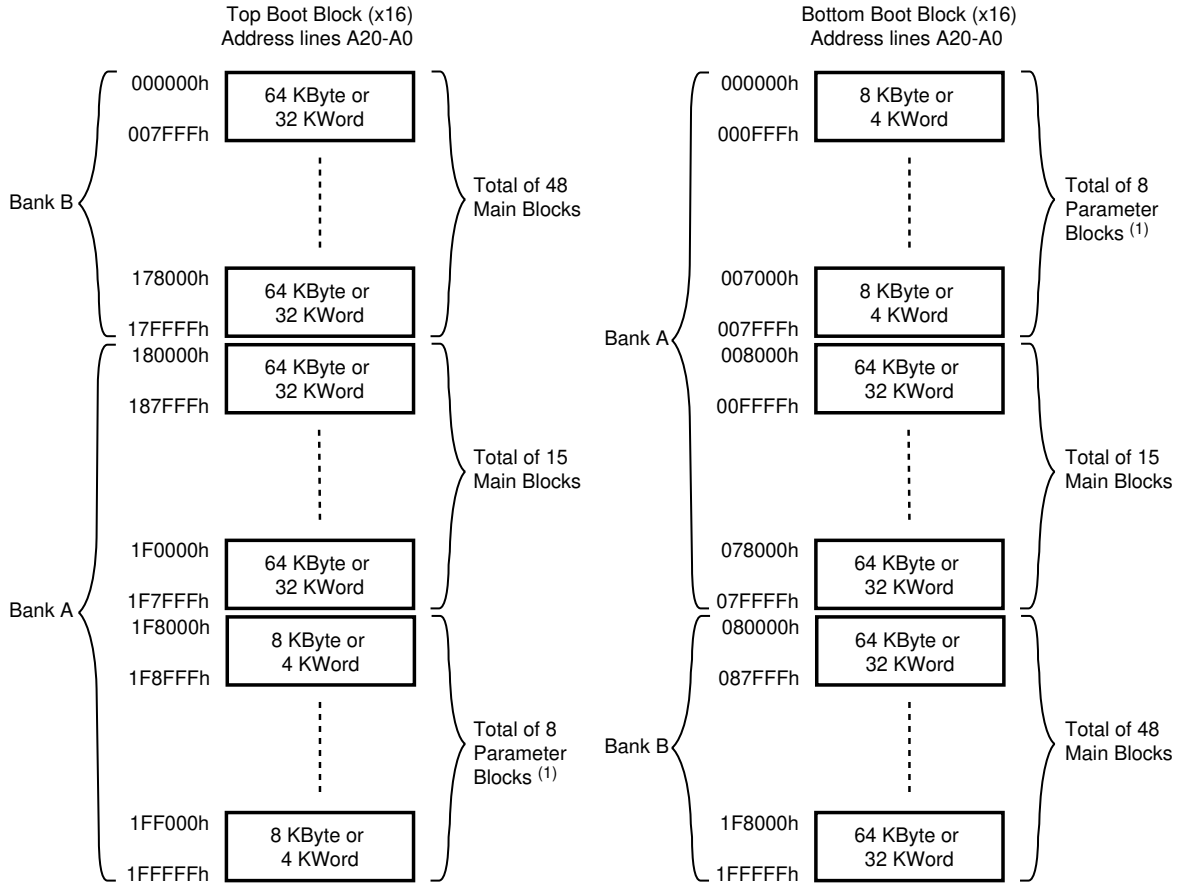


Note 1. Used as Extended Block Addresses in Extended Block mode.

AI05556

Note: Also see APPENDIX A., Table 23. and Table 24. for a full listing of the Block Addresses.

Figure 6. Block Addresses (x16)



Note 1. Used as Extended Block Addresses in Extended Block mode.

AI05555

Note: Also see APPENDIX A., Table 23. and Table 24. for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

Data Inputs/Outputs (DQ0-DQ7). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the Program/Erase Controller.

Data Inputs/Outputs (DQ8-DQ14). The Data I/O outputs the data stored at the selected address during a Bus Read operation when BYTE is High, V_{IH}. When BYTE is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

Data Input/Output or Address Input (DQ15A–1). When BYTE is High, V_{IH}, this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When BYTE is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the addressed Word, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when BYTE is High and references to the Address Inputs to include this pin when BYTE is Low except when stated explicitly otherwise.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

V_{PP}/Write Protect ($V_{PP}/\overline{WP}$). The V_{PP}/Write Protect pin provides two functions. The V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for Program operations. This is achieved by bypassing the unlock cycles and/or using the Double Word or Quadruple Byte Program commands. The Write Protect function provides a hardware method of protecting the two outermost boot blocks.

When V_{PP}/Write Protect is Low, V_{IL}, the memory protects the two outermost boot blocks; Program and Erase operations in these blocks are ignored while V_{PP}/Write Protect is Low, even when $\overline{RP}$ is at V_{ID}.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the two outermost boot blocks. Program and Erase operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

When V_{PP}/Write Protect is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the Command Interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}, see Figure 17.

Never raise V_{PP}/Write Protect to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

The V_{PP}/Write Protect pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

Reset/Block Temporary Unprotect ($\overline{RP}$). The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if $V_{PP}/\overline{WP}$ is at V_{IL}, then the two outermost boot blocks will remain protected even if RP is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, Table 19. and Figure 16., Reset/Block Temporary Unprotect AC Waveforms, for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

Ready/Busy Output ($\overline{RB}$). The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase

operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See Table 19. and Figure 16., Reset/Block Temporary Unprotect AC Waveforms.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Byte/Word Organization Select ($\overline{BYTE}$). The Byte/Word Organization Select pin is used to switch between the x8 and x16 Bus modes of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

V_{CC} Supply Voltage (2.7V to 3.6V). V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase operations, I_{CC3}.

V_{SS} Ground. V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins which must be both connected to the system ground.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby.

The Dual Bank architecture of the M29DW323 allows read/write operations in Bank A, while read operations are being executed in Bank B or vice versa. Write operations are only allowed in one bank at a time.

See Tables 3 and 4, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 11., Read Mode AC Waveforms, and Table 15., Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 12 and 13, Write AC Waveforms, and Tables 16 and 17, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 14., DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Tables 3 and 4, Bus Operations.

Block Protect and Chip Unprotect. Groups of blocks can be protected against accidental Program or Erase. The Protection Groups are shown in APPENDIX A., Tables 23 and 24, Block Addresses. The whole chip can be unprotected to allow the data inside the blocks to be changed.

The V_{PP}/Write Protect pin can be used to protect the two outermost boot blocks. When V_{PP}/Write Protect is at V_{IL} the two outermost boot blocks are protected and remain protected regardless of the Block Protection Status or the Reset/Block Temporary Unprotect pin status.

Block Protect and Chip Unprotect operations are described in APPENDIX D.

Table 3. Bus Operations, $\overline{BYTE} = V_{IL}$

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs DQ15A–1, A0-A20	Data Inputs/Outputs	
					DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Hi-Z	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Hi-Z	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	20h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	5Eh (M29DW323DT) 5Fh (M29DW323DB)
Extended Memory Block Verify Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	81h (factory locked) 01h (not factory locked)

Note: X = V_{IL} or V_{IH}.

Table 4. Bus Operations, $\overline{BYTE} = V_{IH}$

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A20	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	225Eh (M29DW323DT) 225Fh (M29DW323DB)
Extended Memory Block Verify Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	81h (factory locked) 01h (not factory locked)

Note: X = V_{IL} or V_{IH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode. See either Table 5, or 6, depending on the configuration that is being used, for a summary of the commands.

Read/Reset Command

The Read/Reset command returns the memory to its Read mode. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the time-out of a Block erase operation then the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

Auto Select Command

The Auto Select command is used to read the Manufacturer Code, the Device Code, the Block Protection Status and the Extended Memory Block Verify Code. It can be addressed to either Bank. Three consecutive Bus Write operations are required to issue the Auto Select command. The final Write cycle must be addressed to one of the Banks. Once the Auto Select command is issued Bus Read operations to the Bank where the command was issued output the Auto Select data. Bus Read operations to the other Bank will output the contents of the memory array. The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

In Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL} and A19-A20 = Bank Address. The other address bits may be set to either V_{IL} or V_{IH}.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL} and A19-A20 = Bank Address. The other address bits may be set to either V_{IL} or V_{IH}.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, A19-A20 = Bank Address and A12-A18 specifying the address of the block inside the Bank. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

Read CFI Query Command

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. This command is valid when the device is in the Read Array mode, or when the device is in Auto Select mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Auto Select mode.

See APPENDIX B., Tables 25, 26, 27, 28, 29 and 30 for details on the information contained in the Common Flash Interface (CFI) memory area.

Program Command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. After programming has started, Bus Read operations in the Bank being programmed output the Status Register content, while Bus Read operations to the other Bank output the contents of the memory array. See the section on the Status Register for more details. Typical program times are given in Table 7.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Fast Program Commands

There are two Fast Program commands available to improve the programming throughput, by writing several adjacent words or bytes in parallel. The Quadruple Byte Program command is available for x8 operations, while the Double Word Program command is available for x16 operations.

Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend.

Fast Program commands should not be attempted when V_{PP}/WP is not at V_{PP}. Care must be taken because applying a 12V V_{PP} voltage to the VPP/WP pin will temporarily unprotect any protected block.

After programming has started, Bus Read operations in the Bank being programmed output the Status Register content, while Bus Read operations to the other Bank output the contents of the memory array.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Fast Program commands cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Typical Program times are given in Table 7., Program, Erase Times and Program, Erase Endurance Cycles.

Quadruple Byte Program Command. The Quadruple Byte Program command is used to write a page of four adjacent Bytes in parallel. The four bytes must differ only for addresses A0, DQ15A-1. Five bus write cycles are necessary to issue the Quadruple Byte Program command.

- The first bus cycle sets up the Quadruple Byte Program Command.
- The second bus cycle latches the Address and the Data of the first byte to be written.
- The third bus cycle latches the Address and the Data of the second byte to be written.
- The fourth bus cycle latches the Address and the Data of the third byte to be written.
- The fifth bus cycle latches the Address and the Data of the fourth byte to be written and starts the Program/Erase Controller.

Double Word Program Command. The Double Word Program command is used to write a page of two adjacent words in parallel. The two words must differ only for the address A0.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Unlock Bypass Command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the bank enters Unlock Bypass mode. When in Unlock Bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. The Unlock Bypass Program command can be issued to program addresses within the bank, and the Unlock Bypass Reset command to return the bank to Read mode. In Unlock Bypass mode the memory can be read as if in Read mode.

When V_{PP} is applied to the V_{PP}/Write Protect pin the memory automatically enters the Unlock Bypass mode and the Unlock Bypass Program command can be issued immediately. Care must be taken because applying a 12V V_{PP} voltage to the VPP/WP pin will temporarily unprotect any protected block.

Unlock Bypass Program Command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted, a Bus Read operation to the Bank where the command was issued outputs the Status Register. See the Program command for details on the behavior.

Unlock Bypass Reset Command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass Mode.

Chip Erase Command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 7. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

Block Erase Command

The Block Erase command can be used to erase a list of one or more blocks in a Bank. It sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. All blocks must belong to the same Bank; if a block belonging to the other Bank is given it will not be erased. The Block Erase operation starts the Program/Erase Controller after a time-out period of 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. After the sixth Bus Write operation a Bus Read operation within the same Bank will output the Status Register. See the Status Register section for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the 50µs time-out period. Typical block erase times are given in Table 7.

After the Erase operation has started all Bus Read operations to the Bank being erased will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Erase Suspend Command

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within the Erase Suspend Latency time of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

During Erase Suspend a Bus Read operation to the Extended Block will output the Extended Block data.

Erase Resume Command

The Erase Resume command must be used to restart the Program/Erase Controller after an Erase Suspend. The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

Enter Extended Block Command

The M29DW323D has an extra 64KByte block (Extended Block) that can only be accessed using the Enter Extended Block command. Three Bus write cycles are required to issue the Extended Block command. Once the command has been issued the device enters Extended Block mode where all Bus Read or Program operations to the Boot Block addresses access the Extended Block. The Extended Block (with the same address as the boot block) cannot be erased, and can be treated as one-time programmable (OTP) memory. In Extended Block mode the Boot Blocks are not accessible. In Extended Block mode dual operations are possible, with the Extended Block mapped in Bank A. When in Extended Block mode, Erase Commands in Bank A are not allowed.

To exit from the Extended Block mode the Exit Extended Block command must be issued.

The Extended Block can be protected, however once protected the protection cannot be undone.

Exit Extended Block Command

The Exit Extended Block command is used to exit from the Extended Block mode and return the device to Read mode. Four Bus Write operations are required to issue the command.

Block Protect and Chip Unprotect Commands

Groups of blocks can be protected against accidental Program or Erase. The Protection Groups are shown in APPENDIX A., Tables 23 and 24, Block Addresses. The whole chip can be unprotected to allow the data inside the blocks to be changed. Block Protect and Chip Unprotect operations are described in APPENDIX D.

Table 5. Commands, 16-bit mode, $\overline{BYTE}$ = V_{IH}

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	(BKA) 555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Double Word Program	3	555	50	PA0	PD0	PA1	PD1						
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	BKA	B0										
Erase Resume	1	BKA	30										
Read CFI Query	1	55	98										
Enter Extended Block	3	555	AA	2AA	55	555	88						
Exit Extended Block	4	555	AA	2AA	55	555	90	X	00				

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block, BKA Bank Address. All values in the table are in hexadecimal.

The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A20, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 6. Commands, 8-bit mode, $\overline{BYTE}$ = V_{IL}

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset	1	X	F0										
	3	AAA	AA	555	55	X	F0						
Auto Select	3	AAA	AA	555	55	(BKA) AAA	90						
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Quadruple Byte Program	5	AAA	55	PA0	PD0	PA1	PD1	PA2	PD2	PA3	PD3		
Unlock Bypass	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase	6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BA	30
Erase Suspend	1	BKA	B0										
Erase Resume	1	BKA	30										
Read CFI Query	1	AA	98										
Enter Extended Block	3	AAA	AA	555	55	AAA	88						
Exit Extended Block	4	AAA	AA	555	55	AAA	90	X	00				

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A20, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 7. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1, 2)	Max(2)	Unit
Chip Erase		40	200(3)	s
Block Erase (64 KBytes)		0.8	6(3)	s
Erase Suspend Latency Time			50(4)	µs
Program (Byte or Word)		10	200(4)	µs
Double Word Program (Byte or Word)		10	200(3)	µs
Chip Program (Byte by Byte)		40	200(3)	s
Chip Program (Word by Word)		20	100(3)	s
Chip Program (Quadruple Byte or Double Word)		10	100(3)	s
Program/Erase Cycles (per Block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,00 program/erase cycles.
4. Maximum value measured at worst case conditions for both temperature and V_{CC}.

STATUS REGISTER

The M29DW323D has a Status Register that provides information on the current or previous Program or Erase operations executed in each bank. The various bits convey information and errors on the operation. Bus Read operations from any address within the Bank, always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in Table 8., Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 7., Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 8., Toggle Flowchart, gives an example of how to use the Data Toggle Bit. Figures 14 and 15 describe Toggle Bit timing waveform.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Figures 14 and 15 describe Alternative Toggle Bit timing waveform.

Table 8. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	$\overline{RB}$
Program	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program During Erase Suspend	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program Error	Bank Address	$\overline{DQ7}$	Toggle	1	–	–	Hi-Z
Chip Erase	Any Address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	Hi-Z
	Non-Erasing Block	Data read as normal					Hi-Z
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle	Hi-Z
	Faulty Block Address	0	Toggle	1	1	Toggle	Hi-Z

Note: Unspecified data bits should be ignored.

Figure 7. Data Polling Flowchart

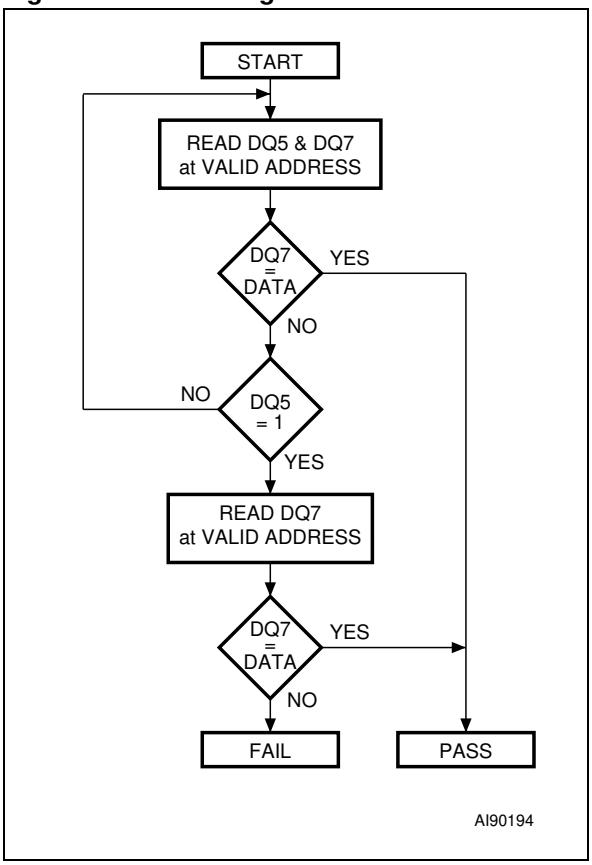
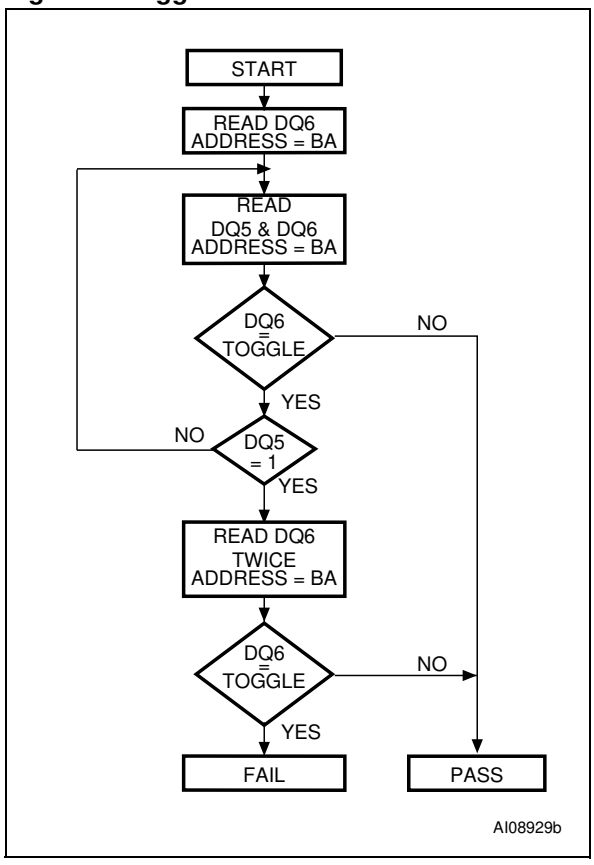


Figure 8. Toggle Flowchart



Note: BA = Address of Bank being Programmed or Erased.

DUAL OPERATIONS AND MULTIPLE BANK ARCHITECTURE

The Multiple Bank Architecture of the M29DW323DT and M29DW323DB gives greater flexibility for software developers to split the code and data spaces within the memory array. The Dual Operations feature simplifies the software management of the device by allowing code to be executed from one bank while the other bank is being programmed or erased.

The Dual Operations feature means that while programming or erasing in one bank, read operations are possible in the other bank with zero latency.

Only one bank at a time is allowed to be in program or erase mode.

If a read operation is required in a bank, which is programming or erasing, the program or erase operation can be suspended.

Also if the suspended operation was erase then a program command can be issued to another block, so the device can have one block in Erase Suspend mode, one programming and other banks in read mode.

By using a combination of these features, read operations are possible at any moment.

Table 9. and Table 10. show the dual operations possible in other banks and in the same bank. Note that only the commonly used commands are represented in these tables.

Table 9. Dual Operations Allowed In the Other Bank

Status of First Bank(1)	Commands allowed in the Other Bank(1)							
	Read Array	Read Status Register(6)	Read CFI Query	Auto Select	Program	Erase	Erase Suspend	Erase Resume
Idle	Yes	Yes(2)	Yes	Yes	Yes	Yes	Yes(2)	Yes(3)
Programming	Yes	No	No	No	–	–	No	No
Erasing	Yes	No	No	No	–	–	No	No
Erase Suspended	Yes	Yes	Yes	Yes	Yes	No	-	Yes

Note: 1. If one bank is involved in a program or erase operation, then the other bank is available for dual operations.
2. Only after an Erase operation in that bank.
3. Only after an Erase Suspend command in that bank.

Table 10. Dual Operations Allowed In Same Bank

Status of bank	Commands allowed in same bank							
	Read Array	Read Status Register(4)	Read CFI Query	Auto Select	Program	Erase	Erase Suspend	Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes(2)	Yes(3)
Programming	No	Yes	No	No	–	–	No	-
Erasing	No	Yes	No	No	–	No	Yes(5)	-
Erase Suspended	Yes(1)	Yes(5)	Yes	Yes	Yes(1)	No	-	Yes(4)

Note: 1. Not allowed in the Block or Word that is being erased or programmed.
2. Only after an Erase operation in that bank.
3. Only after an Erase Suspend command in that bank.
4. Read Status Register is not a command. The Status Register can be read during a block program or erase operation.
5. The Status Register can be read by addressing the block being erase suspended.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering		(1)	°C
V_{IO}	Input or Output Voltage (2,3)	–0.6	V_{CC} +0.6	V
V_{CC}	Supply Voltage	–0.6	4	V
V_{ID}	Identification Voltage	–0.6	13.5	V
V_{PP}(4)	Program Voltage	–0.6	13.5	V

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
3. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.
4. V_{PP} must not remain at 12V for more than a total of 80hrs.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 12., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 12. Operating and AC Measurement Conditions

Parameter	M29DW323D		Unit
	70ns		
	Min	Max	
V_{CC} Supply Voltage	2.7	3.6	V
Ambient Operating Temperature	–40	85	°C
Load Capacitance (C_L)	30		pF
Input Rise and Fall Times		10	ns
Input Pulse Voltages	0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		V

Figure 9. AC Measurement I/O Waveform

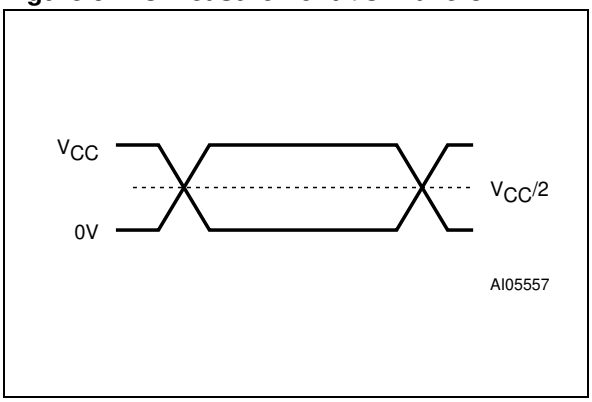


Figure 10. AC Measurement Load Circuit

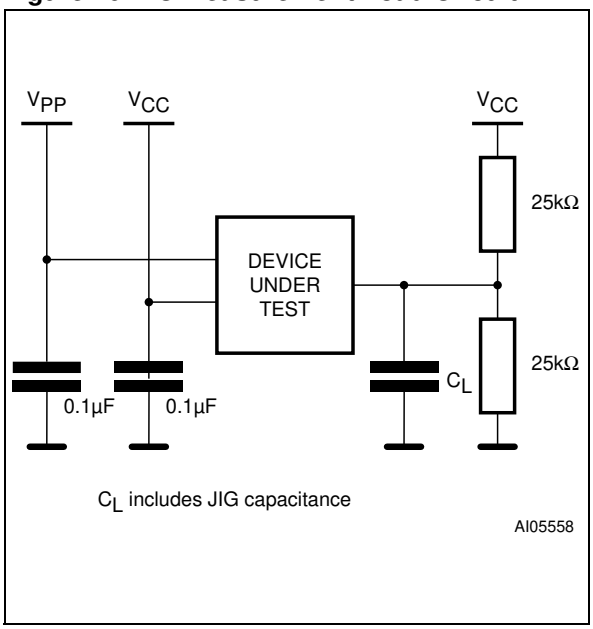


Table 13. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 14. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1} (2)	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz			10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$			100	µA
I_{CC3} (1,2)	Supply Current (Program/ Erase)	Program/Erase Controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}		20	mA
			$V_{PP}/\overline{WP} = V_{PP}$		20	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			$0.7V_{CC}$	V_{CC} +0.3	V
V_{PP}	Voltage for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 2.7V ±10%		11.5	12.5	V
I_{PP}	Current for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 2.7V ±10%			15	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA		V_{CC} –0.4		V
V_{ID}	Identification Voltage			11.5	12.5	V
V_{LKO}	Program/Erase Lockout Supply Voltage			1.8	2.3	V

Note: 1. Sampled only, not 100% tested.
2. In Dual operations the Supply Current will be the sum of I_{CC1}(read) and I_{CC3} (program/erase).

Figure 11. Read Mode AC Waveforms

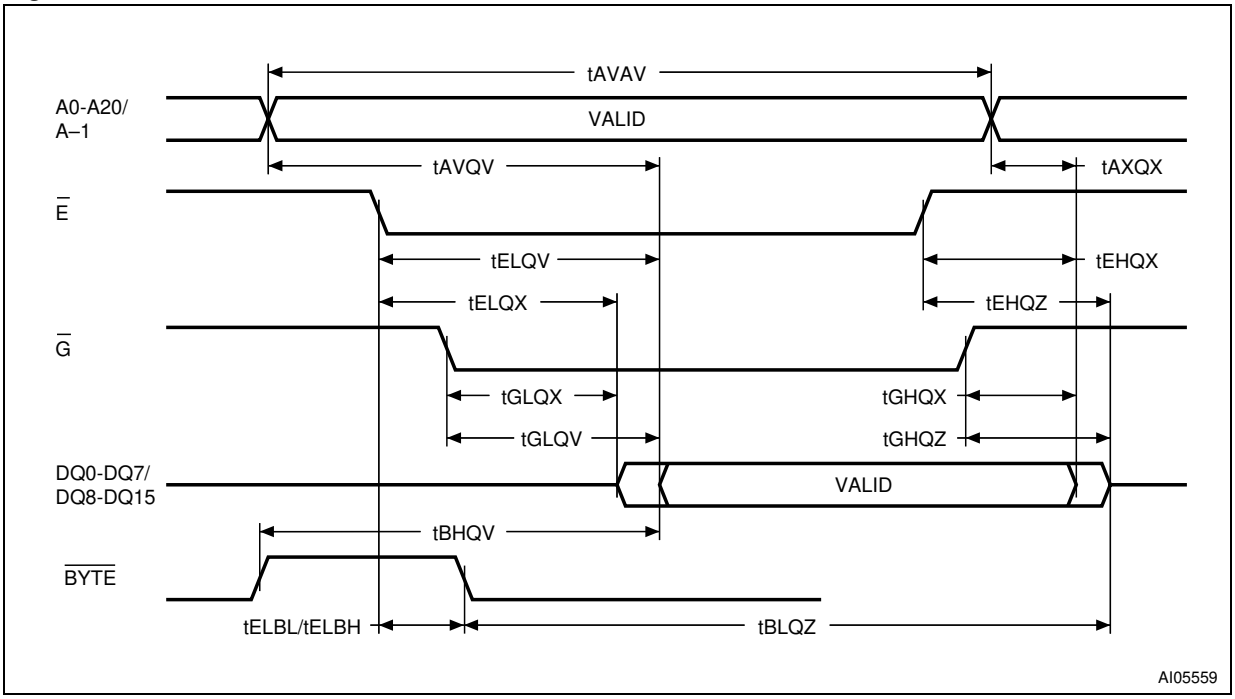


Table 15. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29DW323D	Unit
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	70	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	70	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	30	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	25	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	25	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	ns

Note: 1. Sampled only, not 100% tested.