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Micron Parallel NOR Flash Embedded Memory

Top/Bottom Boot Block 5V Supply

M29F200FT/B, M29F400FT/B, M29F800FT/B, M29F160FT/B

Features

- Supply voltage
  - V_{CC} = 5V
- Access time: 55ns
- Program/erase controller
  - Embedded byte/word program algorithms
- Erase suspend and resume modes
- Low power consumption
  - Standby and automatic standby
- 100,000 PROGRAM/ERASE cycles per block
- Electronic signature
  - Manufacturer code: 0x01h
- Top device codes
  - M29F200FT: 0x2251
  - M29F400FT: 0x2223
  - M29F800FT: 0x22D6
  - M29F160FT: 0x22D2
- Bottom device codes
  - M29F200FB: 0x2257
  - M29F400FB: 0x22AB
  - M29F800FB: 0x2258
  - M29F160FB: 0x22D8
- RoHS-compliant packages
  - TSOP48
  - SO44 (16Mb not available for this package)
- Automotive device grade 3
  - Temperature: –40 to +125°C
- Automotive device grade 6
  - Temperature: –40 to +85°C
- Automotive grade certified (AEC-Q100)

Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details
Device Type	M29F = 5V
Density	200 = 2Mb
	400 = 4Mb
	800 = 8Mb
	160 = 16Mb (not available in SO 44 package)
Technology	F = 110nm
Configuration	T = Top boot
	B = Bottom boot
Speed	55 = 55ns device speed in conjunction with temperature range = 3, which denotes Auto Grade –40 to 125 °C parts
	5A = 55ns access time (Auto Grade) only in conjunction with the Grade 6 option
Package	M = SO 44
	N = TSOP 48 12mm x 20mm AL 42
Temperature Range	6 = –40°C to +85°C
	3 = –40°C to +125°C
Shipping Options	blank = standard packing (Tray)
	E = RoHS-compliant package, standard packing (tray)
	T = Tape and reel packing (24mm)
	F = RoHS-compliant package, tape and reel packing (24mm)
Fab Location	2 = Fab 13 (Singapore)

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General Description

This description applies specifically to the M29F 16Mb (2 Meg x 8 or 1 Meg x 16) nonvolatile memory device, but also applies to lower densities. The device enables READ, ERASE, and PROGRAM operations using a single, low-voltage (4.5–5.5V) supply. On power-up, the device defaults to read mode and can be read in the same way as a ROM or EPROM.

The device is divided into blocks that can be erased independently, preserving valid data while old data is erased. Each block can be protected independently to prevent accidental PROGRAM or ERASE operations from modifying the memory. PROGRAM and ERASE commands are written to the command interface. An on-chip program/erase controller simplifies the process of programming or erasing the device by managing the operations required to update the memory contents.

The end of a PROGRAM or ERASE operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks are asymmetrically arranged. The first or last 64KB have been divided into four additional blocks. The 16KB boot block can be used for small initialization code to start the microprocessor. The two 8KB parameter blocks can be used for parameter storage. The remaining 32KB is a small main block where the application may be stored.

CE#, OE#, and WE# control the bus operation of the memory. They enable simple connection to most microprocessors, often without additional logic. Devices are offered in 48-pin TSOP (12mm x 20mm) and 44-pin small-outline packages. The device is supplied with all the bits erased (set to 1).

Figure 1: Logic Diagram

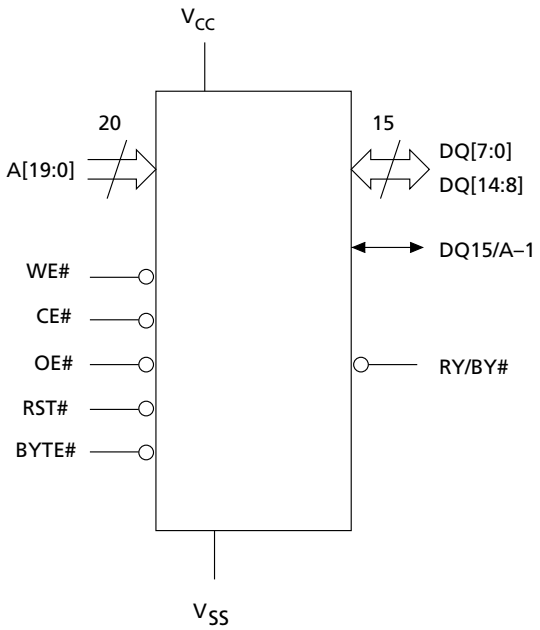


Figure 2: Block Addresses, M29F160 (x8)

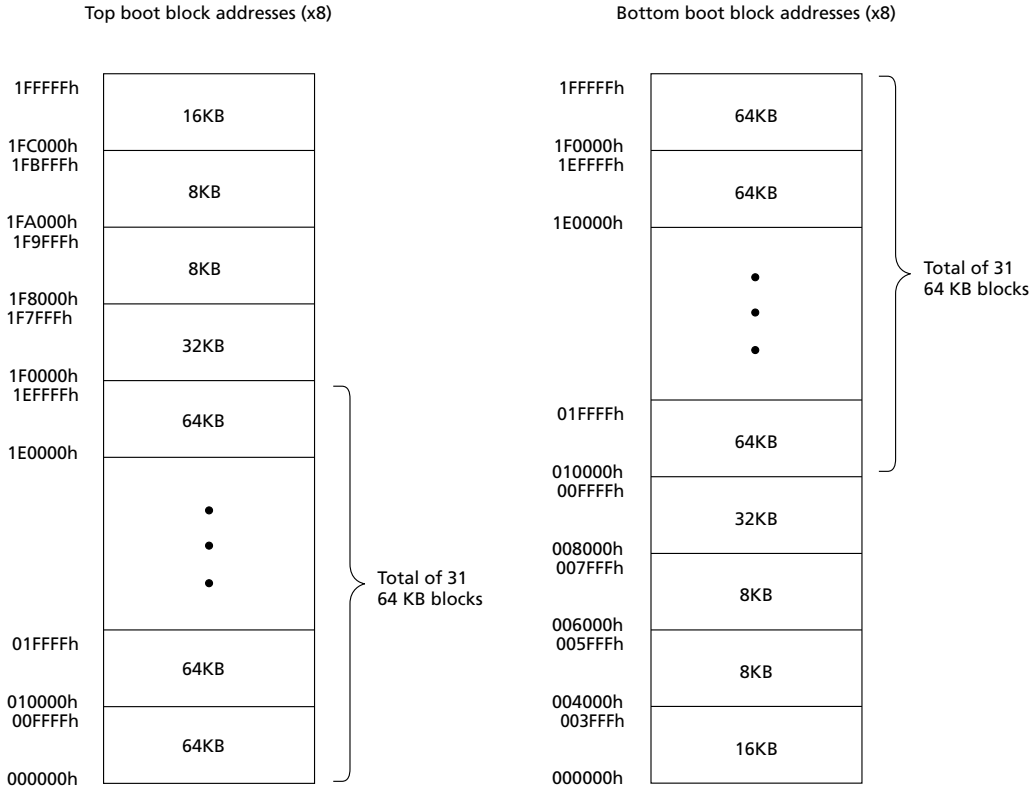


Figure 3: Block Addresses, M29F160 (x16)

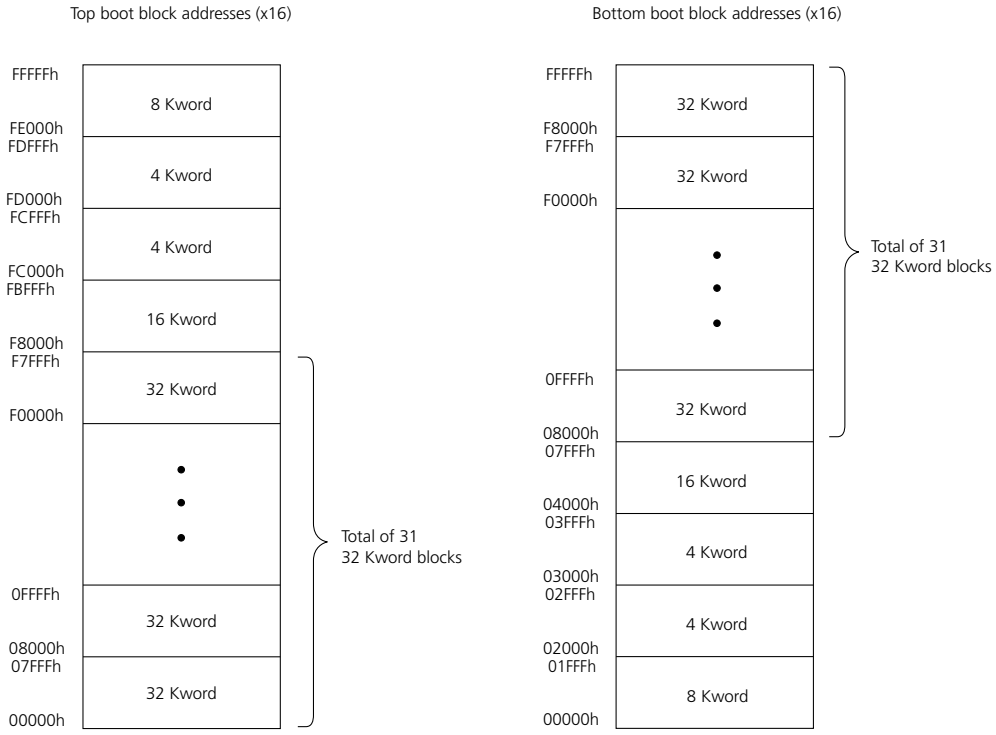


Figure 4: Block Addresses, M29F800 (x8)

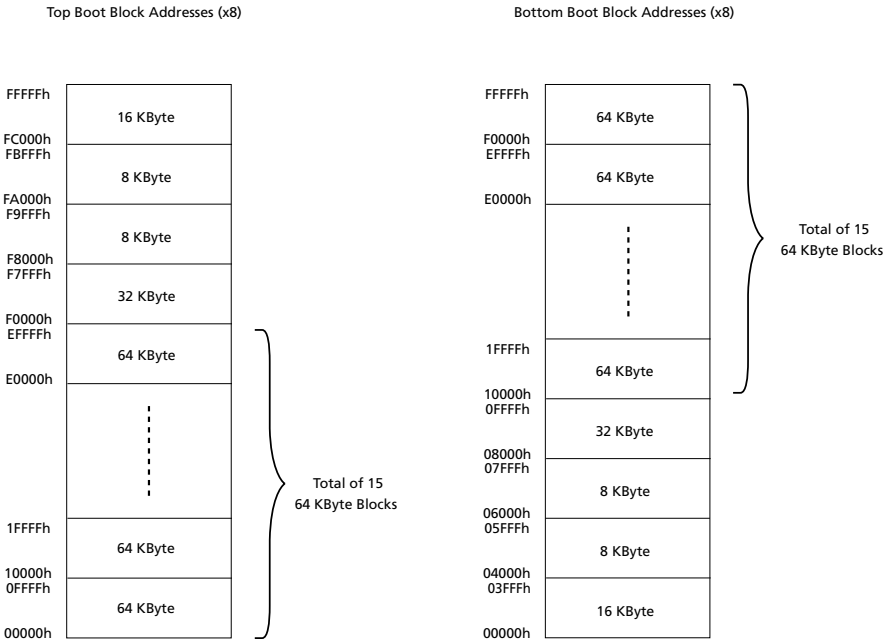


Figure 5: Block Addresses, M29F800 (x16)

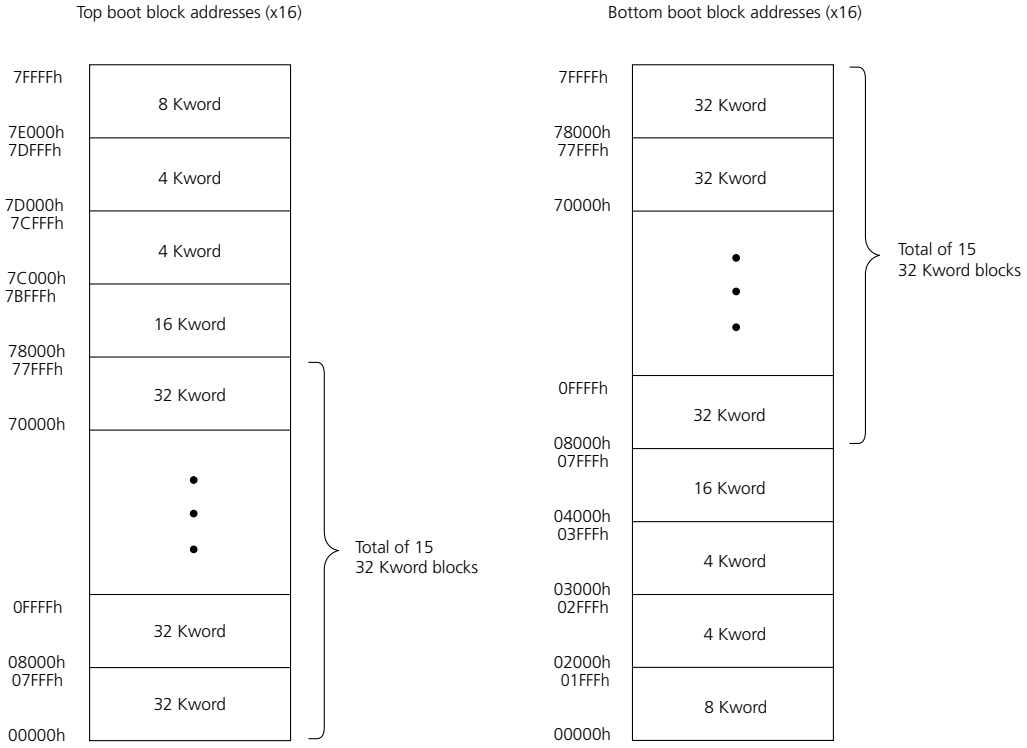


Figure 6: Block Addresses, M29F400 (x8)

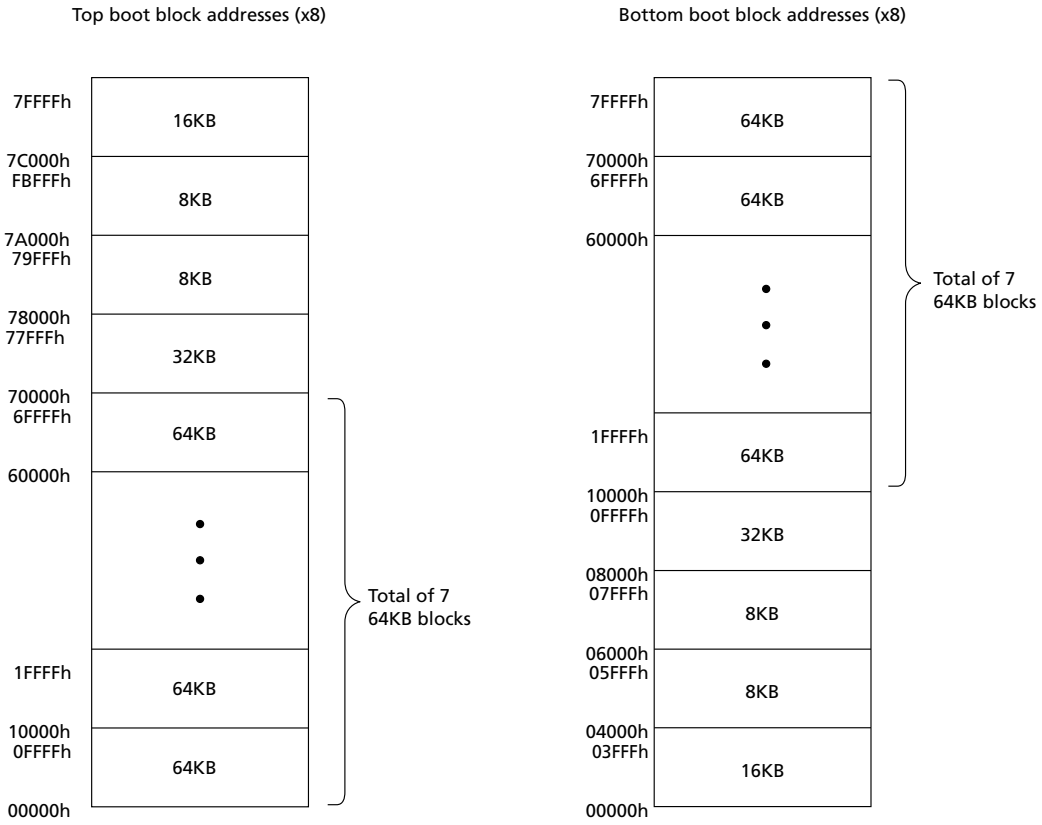


Figure 7: Block Addresses, M29F400 (x16)

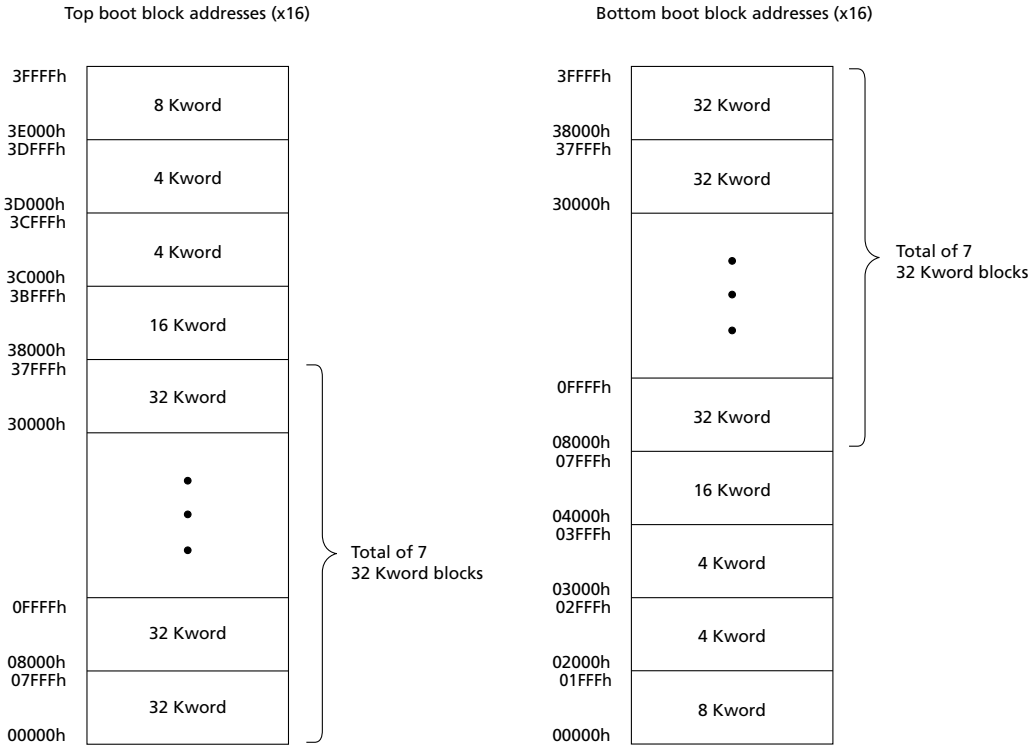


Figure 8: Block Addresses, M29F200 (x8)

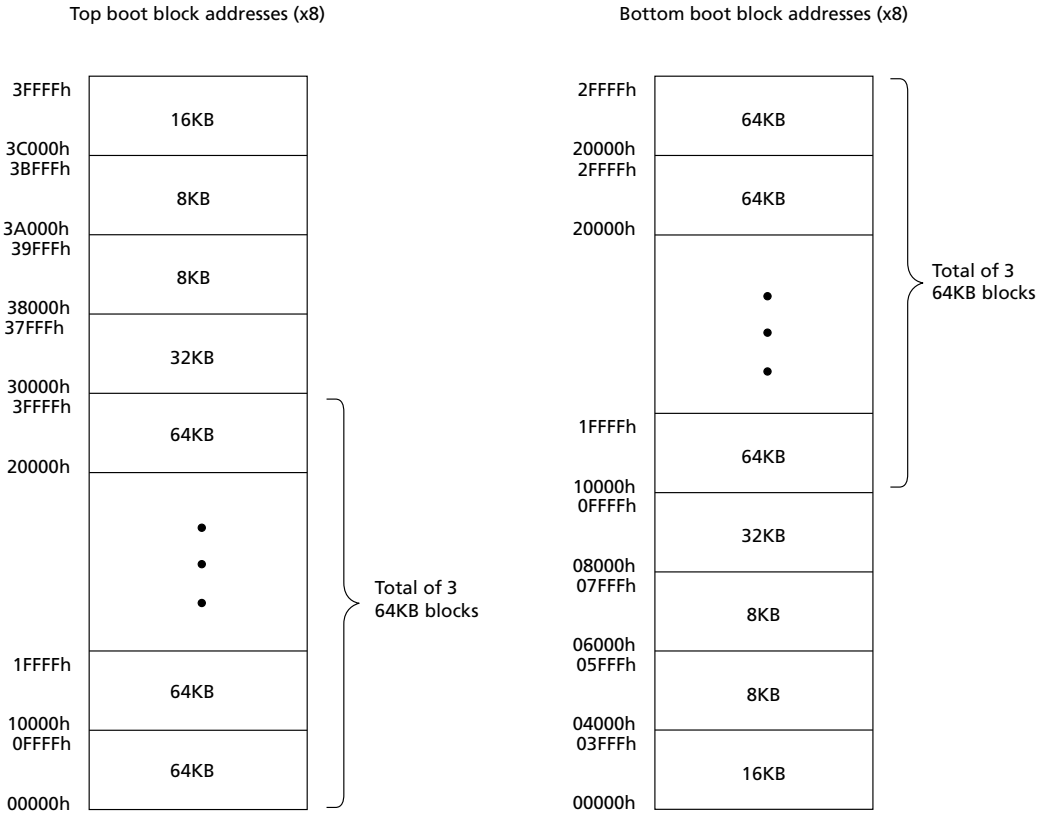
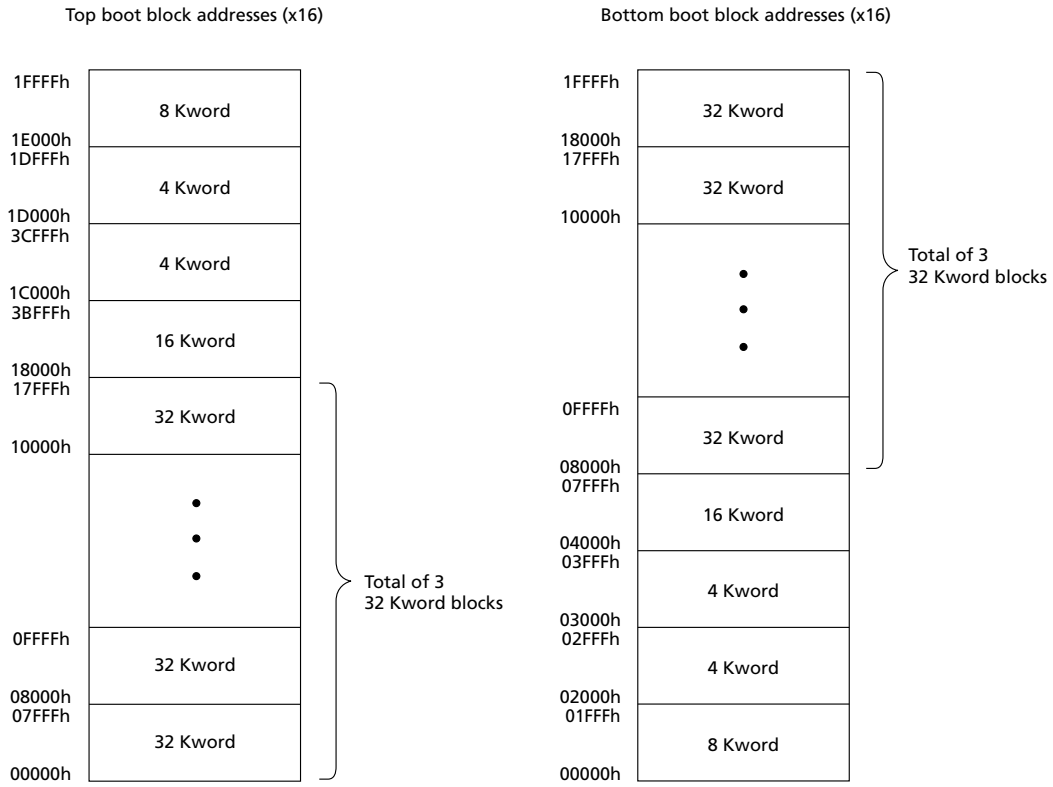


Figure 9: Block Addresses, M29F200 (x16)



Signal Assignments

TSOP Pin Assignments

Figure 10: M29F160F

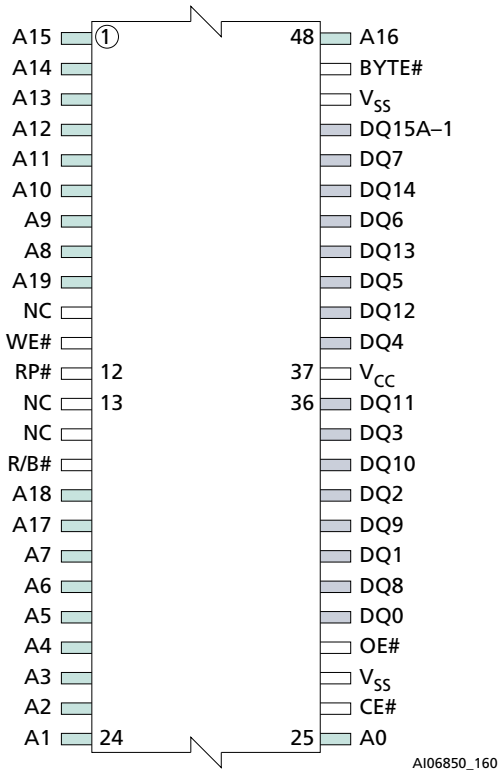


Figure 11: M29F800F

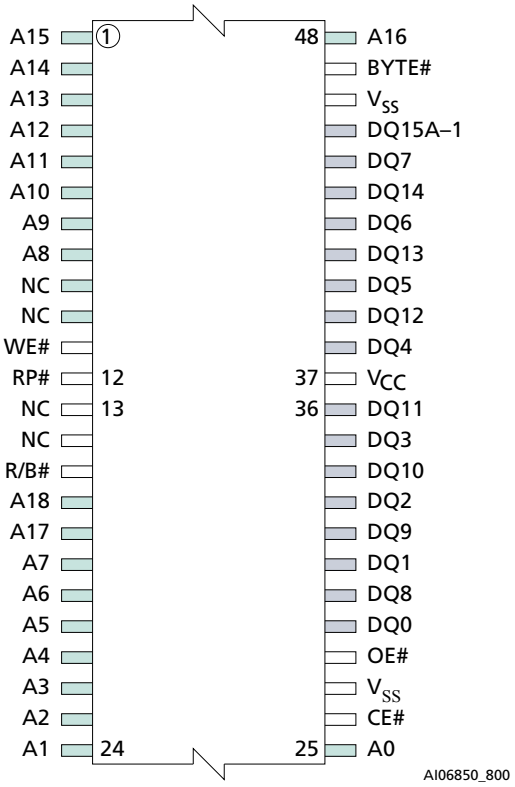


Figure 12: M29F400F

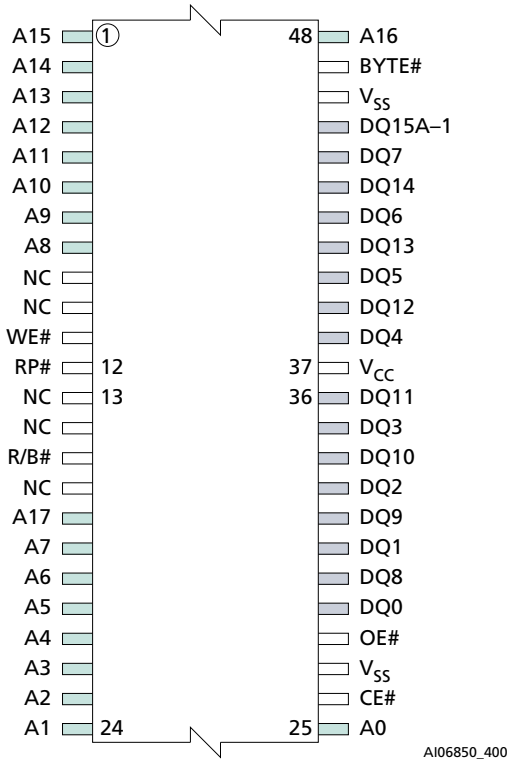
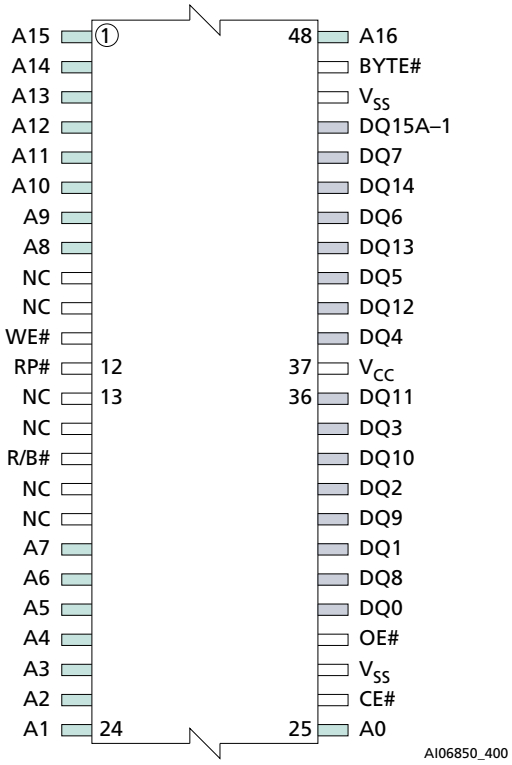


Figure 13: M29F200F



Small-Outline Pin Assignments

Figure 14: M29F800

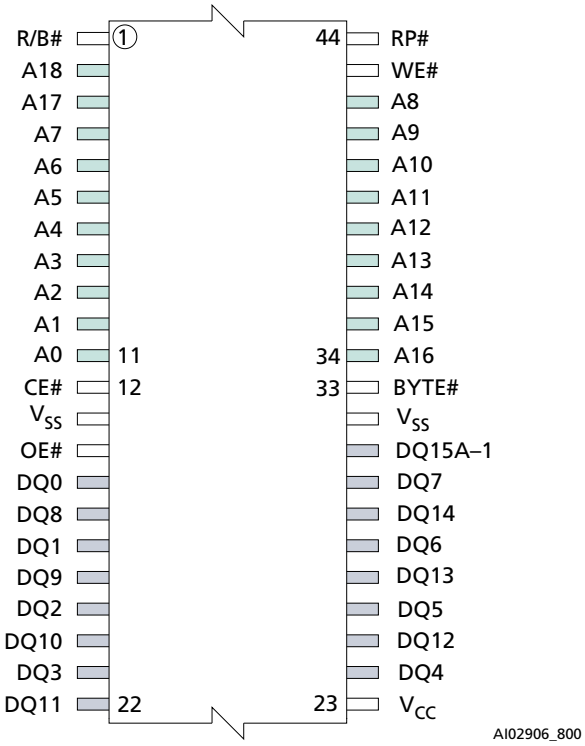


Figure 15: M29F400

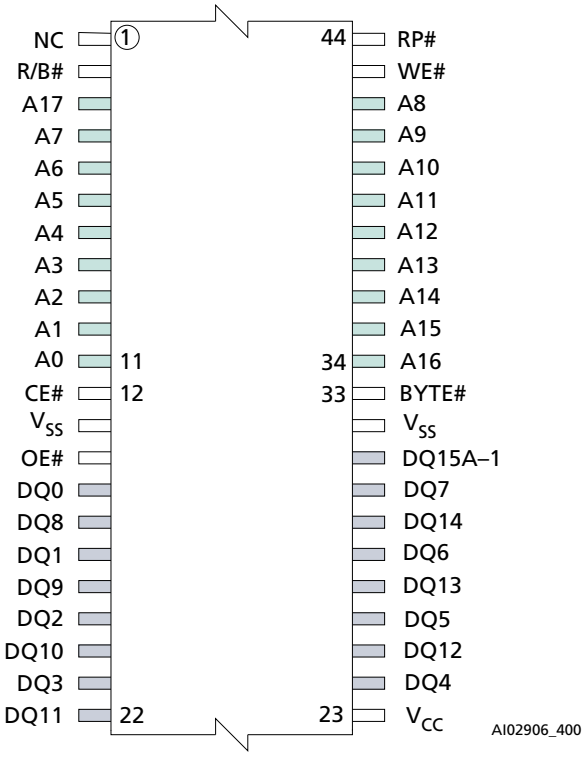
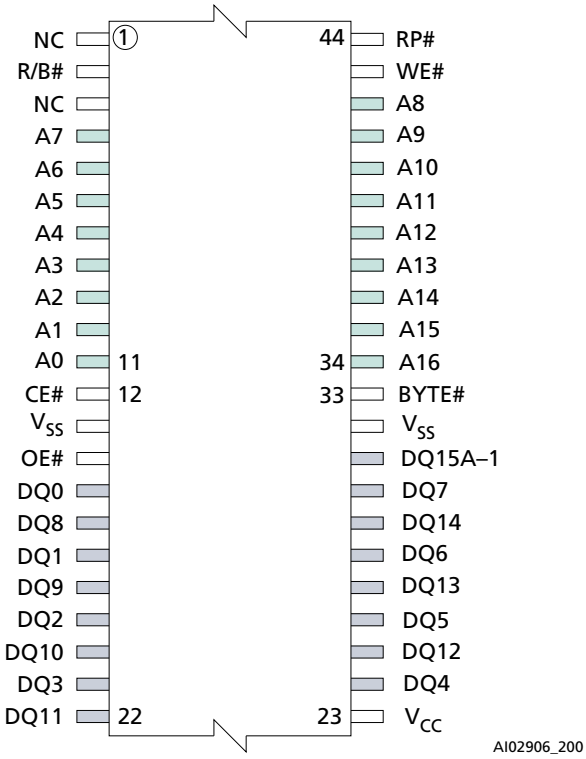


Figure 16: M29F200



Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 2: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, all other pins are ignored.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). Holding RST# at V_{ID} will temporarily unprotect the protected blocks. PROGRAM and ERASE operations on all blocks will then be possible. The transition from V_{IH} to V_{ID} must be slower than ^{t}PHPHH.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the program/erase controller.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details). The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy.

Table 2: Signal Descriptions (Continued)

Name	Type	Description
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when $V_{CC} < V_{LKO}$. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).
V_{SS}	Supply	**Ground:** Reference for all voltage measurements. All V_{SS} pins must be connected to the system ground.
NC	–	**Not connected:** Not connected internally.

Bus Operations

Table 3: Bus Operations

Notes 1 through 2 apply to entire table

Operation	CE#	OE#	WE#	8-Bit Mode			16-Bit Mode	
				A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	Command address	High-Z	Data input	Command address	Data input
OUTPUT DISABLE	X	H	H	X	High-Z	High-Z	X	High-Z
STANDBY	H	X	X	X	High-Z	High-Z	X	High-Z

Notes: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Read

Bus READ operations read from the memory cells or specific registers in the command interface. A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Standby

When CE# is HIGH, the device enters standby, and data I/Os are High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.2V. (See DC Characteristics.) During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic Standby

If CMOS levels (V_{CC} ±0.2V) are used to drive the bus, and the bus is inactive for 150ns or more, the device enters automatic standby, and the internal supply current is reduced to that of the standby supply current, I_{CC2}. The data I/Os will output data if a READ operation is in progress.

Command Interface

All WRITE operations are interpreted by the command interface. Commands consist of one or more sequential WRITE operations. Failure to observe a valid sequence will result in the memory returning to read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode.

READ/RESET Command

The READ/RESET command returns the device to read mode, where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the status register. Either one or three WRITE operations can be used to issue the READ/RESET command.

The READ/RESET command can be issued, between WRITE cycles, before the start of a PROGRAM or ERASE operation, to return the device to read mode. Once the PROGRAM or ERASE operation has started, the READ/RESET command is no longer accepted. The READ/RESET command will not abort an ERASE operation when issued while in erase suspend.

AUTO SELECT Command

The AUTO SELECT command is used to read the electronic signature, including the manufacturer code, the device code and the block protection status. Three consecutive WRITE operations are required to issue the AUTO SELECT command. Once the command is issued, the memory remains in auto select mode until a READ/RESET command is issued. READ CFI QUERY and READ/RESET commands are accepted in auto Select mode, while all other commands are ignored.

Note: These operations are intended for use by programming equipment and are not typically used in applications. They require V_{ID} to be applied to some of the pins.

From the auto select mode the manufacturer code can be read using a READ operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The manufacturer code for Micron is 0001h.

The device code can be read using a READ operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The block protection status of each block can be read using a READ operation with A0 = V_{IL}, A1 = V_{IH}, and A12-A19 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output. See Block Protection Operations for information on the block protection status; the Programmer Technique Block Protection table includes block protection bus READ information.