Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

UM0269
User manual

M29W128F Flash memory
VHDL Model v1.0

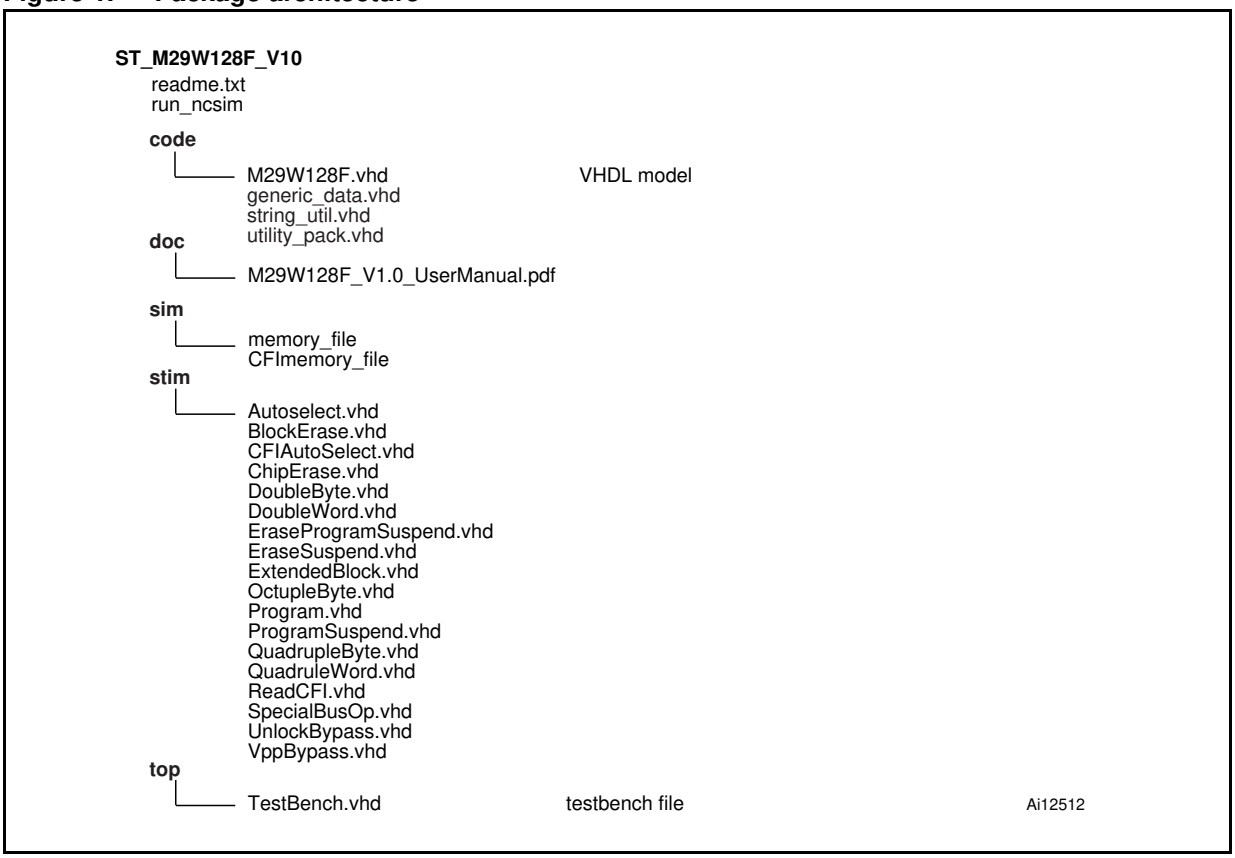
This user manual describes the VHDL behavioral model for M29W128FH and M29W128FL Flash memory devices. The M29W128FH and M29W128FL memories will be referred to as M29W128F throughout the document unless otherwise specified.

Organization of the VHDL Model Delivery package

The VHDL Model Delivery Package,*ST_M29W128F_V10.zip,* is organized into a main directory, named *M29W128F_V10, containing* five subdirectories with their related files (see *Figure 1: Package architecture*):

1. **code** subdirectory: it contains the code source files
2. **doc** subdirectory: it contains the model documentation (application note)
3. **sim** subdirectory: it contains the simulation initialization files
4. **stim** subdirectory: it contains the stimuli files used for simulation
5. **top** subdirectory: it contains the testbench file used for simulation

Figure 1. Package architecture



1. See the readme.txt file for the complete list of files contained in each folder.

Contents

1 Device description

The M29W128F is 128-Mbit (16Mb x8 or 8Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. At Power-up, the memory defaults to its Read mode.

The M29W128F is divided into 256 thirty-two KWord (sixty-four KByte) uniform blocks.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The Chip Enable, Output Enable and Write Enable signals control the bus operations of the memory. They enable simple connection to most microprocessors, often without additional logic.

The device supports Asynchronous Random Read and Page Read from all blocks of the memory array.

The M29W128F has one extra 256 Byte block (Extended Block) that can be accessed using a dedicated command. The Extended Block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently, so it is possible to preserve valid data while old data is erased.

The device features two different levels of hardware block protection to avoid unwanted program or erase (modify) operations.

- The VPP/WP pin provides a hardware protection of the highest block on the M29W128FH and the lowest block on the M29W128FL.
- The RP pin temporarily unprotects all the blocks previously protected using a High Voltage Block Protection technique (see *Appendix D of datasheet: High Voltage Block Protection*).

2 VHDL behavioural model

The M29W128F VHDL behavioural model v1.0 is contained in the *m29w128f.vhd* file of the **code** subdirectory. It includes a set of libraries that implement all the device functions listed in the device datasheet. See *Section 2.1* for the description of the libraries.

Note: Please check the ST web site or contact your local ST Sales office for the most recent version of the device datasheet.

Please refer to readme.txt file in the main package directory for reference datasheet used during model development and validation.

This model was validated using a Cadence NC-SIM 5.4 simulator. The use of this model with other simulators is not guaranteed.

2.1 Model libraries

The M29W128F VHDL model libraries are described in the following sections.

The **code**/*m29w128f.vhd* VHDL file and libraries code files must be compiled in the same order as described below and specified in the *run_ncsim* file.

2.1.1 *string_util.vhd*

This library contains the utilities used for string management.

2.1.2 generic_data.vhd

This library contains generic constants.

2.1.3 utility_pack.vhd

This library contains generic procedures.

2.2 VHDL Testbench and Stimuli files

The **top** subdirectory of the VHDL Model Delivery Package contains a testbench file, *TestBench.vhd*.

Stimuli files in VHDL format are available in the **stim** subdirectory. The stimuli files cover many operational conditions of the device, and in particular, the Command User Interface (CUI) commands.

The testbench and the stimuli files are written using the standard VHDL version.

3 Simulation guidelines

3.1 Launching a simulation

run_ncsim is an example of script used to launch the Cadence NC-SIM simulation. It is located in the main directory. This file compiles and elaborates the VHDL model file and the stimuli files contained into the **stim** directory.

3.2 Simulation timings

To reduce the simulation time, certain program and erase times are reduced in the VHDL simulation model (see *Table 1*).

These values can be configured by setting the variables listed in *Table 1* in the *timing_data.vhd* library file.

Table 1. Simulation times

Timing	Real time	Simulation time	Unit
Block Erase	0.8	$8*10^{-6}$	s
Chip Erase	80	$10*10^{-6}$	s
Word Program	10	1	µs
Program Suspend Latency	5	0.5	µs
Erase Suspend Latency	50	5	µs

3.3 *memory_file* file format

To facilitate testing of the memory array behaviour and model functions, the memory array must be loaded with specific data at power-up.

The format of the *memory_file*, located in the **sim** subdirectory, must be as follows:

```
hex_first_address/hex_data
```

For example:

```
07FFFF/7FFF
```

The user must write the file name into the entity file (this file name path cannot be empty):

```
generic(memoryfile: string := path/filename)
```

If the user does not provide the initialization file, all the memory bits are loaded with ‘1’, therefore the whole array is erased.

Similarly, the *CFImemory_file* file is used to load the model CFI area of the M29W128F. All these files are located in the **sim** subdirectory.

4 VHDL types used in model ports

The port section of M29W128F VHDL model defines the name and the related type for each signal of the device, as shown in *Table 2*.

Table 2. Model ports

Port	Type	Description
A0-A22	Standard Logic (22 down to 0)	Address Inputs
DQ0-DQ14	Standard Logic (14 down to 0)	Data Input /Output
DQ15A-1	Standard Logic	Data Input /Output
BYTE	Standard Logic	Byte/Word Organization Select
E_N	Standard Logic	Chip Enable
G_N	Standard Logic	Output Enable
W_N	Standard Logic	Write Enable
RP_N	Standard Logic	Reset /Block Temporary Unprotect
Vpp/WP_N	Real	Vpp/Write Protect
RB	Standard Logic	Ready/Busy Output
Vss	Real	Ground
Vcc	Real	Supply Voltage

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
7-Jul-2006	0.1	Initial release.
19-Jul-2006	1	Second release.
6-Oct-2006	2	Modified Datasheet reference information in *Section 2: VHDL behavioural model on page 4*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com