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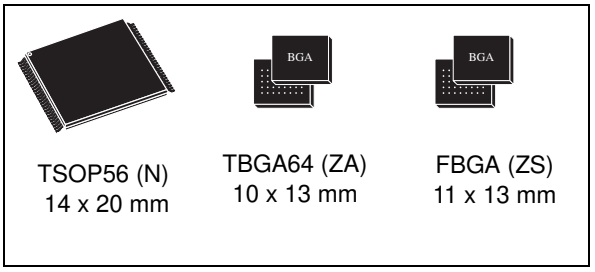
M29W128GH
M29W128GL

128-Mbit (16 Mbit x8 or 8 Mbit x16, page, uniform block) 3 V supply flash memory

Features

- Supply voltage
  - V_{CC} = 2.7 to 3.6 V for program, erase, read
  - V_{CCQ} = 1.65 to 3.6 V for I/O buffers
  - V_{PPH} = 12 V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8 words or 16 bytes
  - Page access: 25, 30 ns
  - Random access: 60 (only available upon customer request) or 70, 80 ns
- Fast program commands
  - 32 words (64-byte write buffer)
- Enhanced buffered program commands
  - 256 words
- Programming time
  - 16 µs per byte/word typical
  - Chip program time: 5 s with V_{PPH} and 8 s without V_{PPH}
- Memory organization
  - M29128GH/L: 128 main blocks, 128 Kbytes/64 Kwords each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/ erase suspend and resume
  - Read from any block during program suspend
  - Read and program another block during erase suspend



TSOP56 (N) 14 x 20 mm

TBGA64 (ZA) 10 x 13 mm

FBGA (ZS) 11 x 13 mm

- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer/Enhanced Buffer Program commands
  - Faster production/batch programming
  - Faster block and chip erase
- $V_{PP}/\overline{WP}$ pin for fast program and write: protects first or last block regardless of block protection settings
- Software protection:
  - Volatile protection
  - Non-volatile protection
  - Password protection
- Common flash interface
  - 64-bit security code
- 128-word extended memory block
  - Extra block used as security block or to store additional information
- Low power consumption
  - Standby and automatic standby
- Minimum 100,000 program/erase cycles per block
- RoHS compliant packages
- Automotive device grade: Temperature -40 °C to 125 °C (Automotive grade certified)

Table 1. Device summary

Root part number	Device code
M29W128GH: uniform, last block protected by $V_{PP}/\overline{WP}$	227Eh + 2221h + 2201h
M29W128GL: uniform, first block protected by $V_{PP}/\overline{WP}$	227Eh + 2221h + 2200h

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1 Description

The M29W128GH and M29W128GL are 128-Mbit (8 Mbit x16 or 16 Mbit x8) non-volatile flash memories that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. On power-up the memory defaults to its read mode.

The memory array is divided into 64-Kword/128-Kbyte uniform blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The M29W128GH and M29W128GL support asynchronous random read and page read from all blocks of the memory array. The devices also feature a write to buffer program capability that improves the programming throughput by programming in one shot a buffer of 32 words/64 bytes. The enhanced buffered program feature is also available to speed up the programming throughput, allowing to program 256 words in one shot (only in x16 mode). The $V_{PP}/\overline{WP}$ signal can be used to enable faster programming of the device.

The M29W128GH and M29W128GL have an extra block, the extended block, of 128 words in x16 mode or of 256 bytes in x8 mode that can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is not reversible, once protected the protection cannot be undone.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection:
  - The $V_{PP}/\overline{WP}$ provides a hardware protection of the highest and lowest block on the M29W128GH, M29W128GL, respectively.
- Software protection:
  - Volatile protection
  - Non-volatile protection
  - Password protection

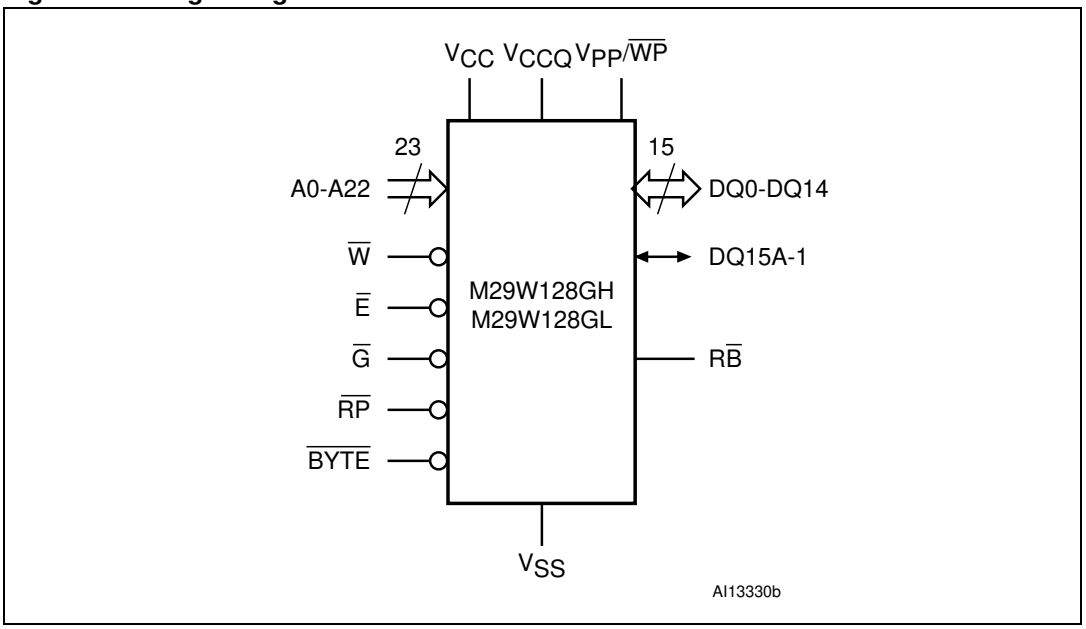
The M29W128GH and M29W128GL are offered in TSOP56 (14 x 20 mm), and TBGA64 (10 x 13 mm, 1 mm pitch), packages. The memories are delivered with all the bits erased (set to ‘1’).

Table 2. Signal names

Name	Description	Direction
A0-A22	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or address input	I/O
$\overline{E}$	Chip enable	Input
$\overline{G}$	Output enable	Input
$\overline{W}$	Write enable	Input
$\overline{RP}$	Reset	Input
$R\overline{B}$	Ready/busy output	Output
$\overline{BYTE}$	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
$V_{PP}/\overline{WP}$(1)	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

1. $V_{PP}/\overline{WP}$ may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

Figure 1. Logic diagram



1. Also see *Appendix A* and *Table 35* for a full listing of the block addresses.

Figure 2. TSOP connections

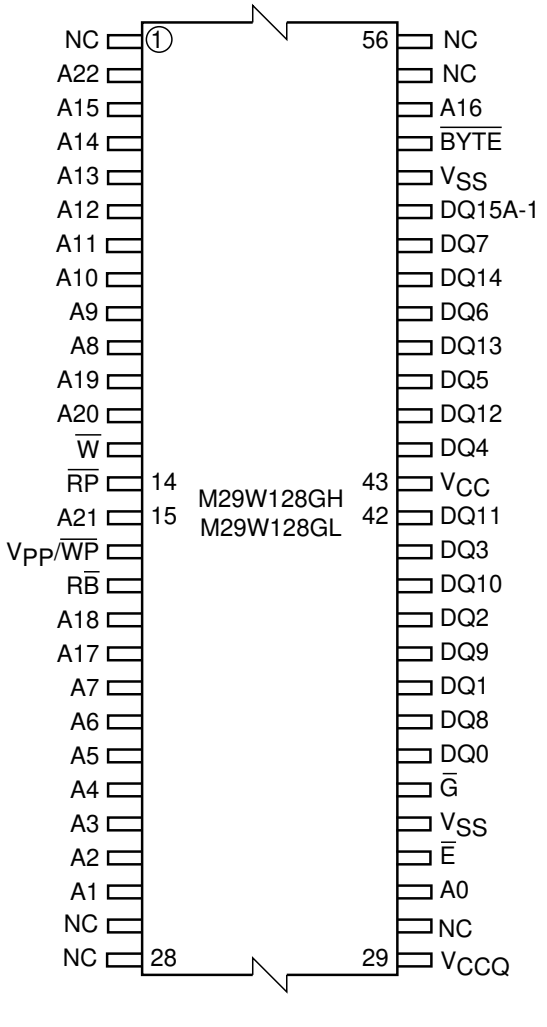
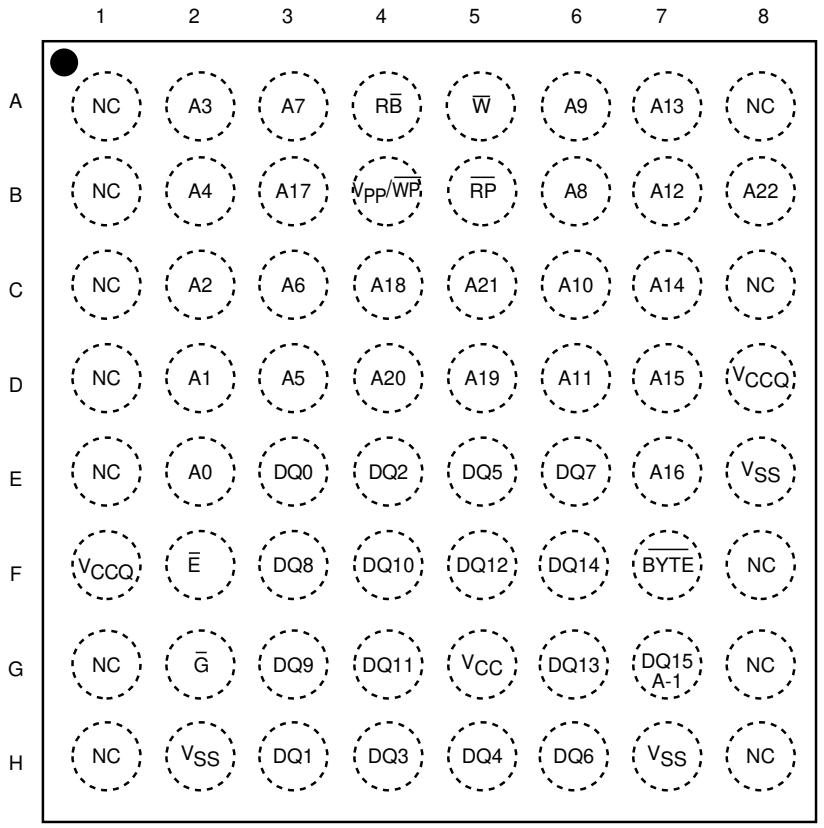
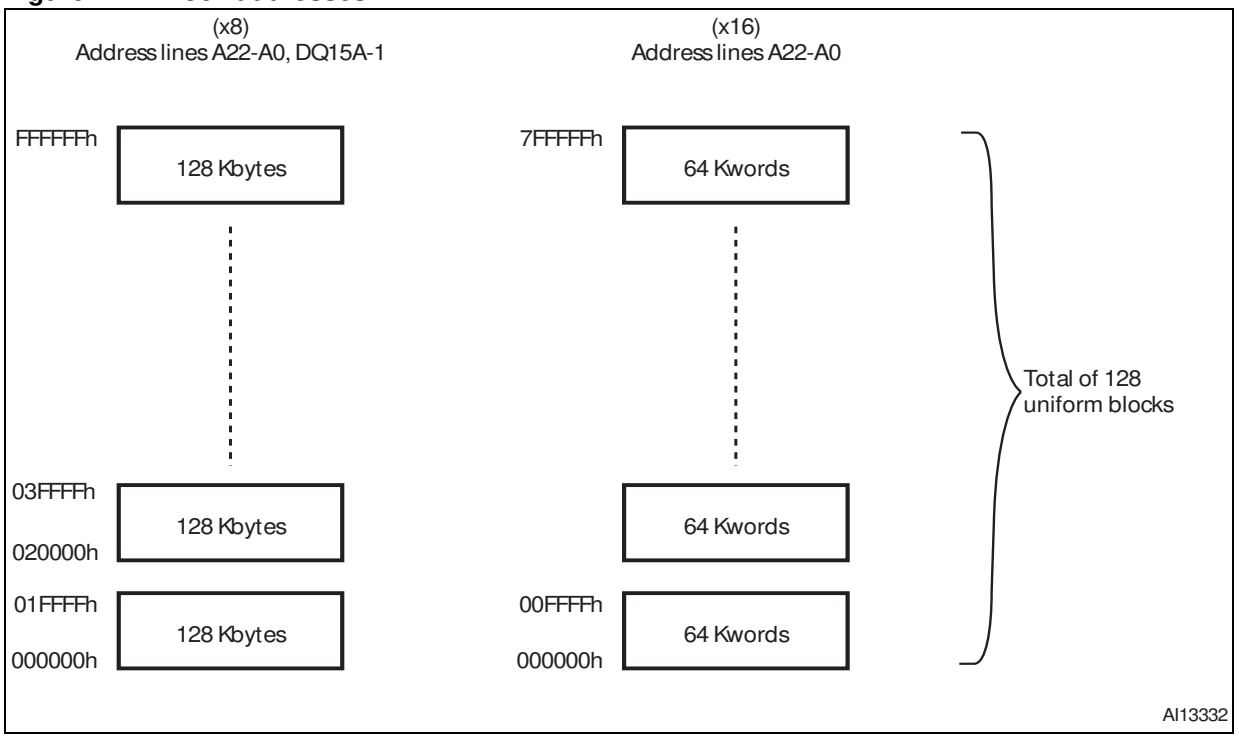


Figure 3. TBGA and FBGA connections (top view through package)



AI11527c

Figure 4. Block addresses



2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 2: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A22)

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The data I/O outputs the data stored at the selected address during a bus read operation. During bus write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The data I/O outputs the data stored at the selected address during a bus read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During bus write operations the command register does not use these bits. When reading the status register these bits should be ignored.

2.4 Data inputs/outputs or address inputs (DQ15A–1)

When the device is in x 16 bus mode, this pin behaves as a data input/output pin (as DQ8-DQ14). When the device operates in x 8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the data input/output to include this pin when the device operates in x 16 bus mode and references to the address inputs to include this pin when the device operates in x 8 bus mode except when stated explicitly otherwise.

2.5 Chip enable ($\overline{E}$)

The chip enable pin, $\overline{E}$, activates the memory, allowing bus read and bus write operations to be performed. When chip enable is High, V_{IH}, all other pins are ignored.

2.6 Output enable ($\overline{G}$)

The output enable pin, $\overline{G}$, controls the bus read operation of the memory.

2.7 Write enable ($\overline{W}$)

The write enable pin, $\overline{W}$, controls the bus write operation of the memory's command interface.

2.8 V_{PP}/write protect ($V_{PP}/\overline{WP}$)

The V_{PP}/write protect pin provides two functions. The V_{PPH} function allows the memory to use an external high voltage power supply to reduce the time required for program operations. This is achieved by bypassing the unlock cycles.

The write protect function provides a hardware method of protecting the highest or lowest block (see *Section 1: Description*). When V_{PP}/write protect is Low, V_{IL}, the highest or lowest block is protected. Program and erase operations on this block are ignored while V_{PP}/write protect is Low.

When V_{PP}/write protect is High, V_{IH}, the memory reverts to the previous protection status of the highest or lowest block. Program and erase operations can now modify the data in this block unless the block is protected using block protection.

When V_{PP}/write protect is raised to V_{PPH} the memory automatically enters the unlock bypass mode (see *Section 6.2.6*).

When V_{PP}/write protect is raised to V_{PPH}, the execution time of the command is lower (see *Table 17: Program, erase times and program, erase endurance cycles*).

When V_{PP}/write protect returns to V_{IH} or V_{IL} normal operation resumes. During unlock bypass program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 24: Accelerated program timing waveforms*).

Never raise V_{PP}/write protect to V_{PPH} from any mode except read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/write protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 25: DC characteristics*).

The V_{PP}/write protect pin may be left floating or unconnected because it features an internal pull-up.

Refer to *Table 3* for a summary of $V_{PP}/\overline{WP}$ functions.

Table 3. $V_{PP}/\overline{WP}$ functions

$V_{PP}/\overline{WP}$	Function
V_{IL}	Highest block protected on M29W128GH. Lowest block protected on M29W128GL.
V_{IH}	Highest and lowest block unprotected unless a software protection is activated (see *Section 4: Hardware protection*).
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming.

2.9 Reset ($\overline{RP}$)

The reset pin can be used to apply a hardware reset to the memory.

A hardware reset is achieved by holding reset Low, V_{IL}, for at least t_{PLPX}. After reset goes High, V_{IH}, the memory will be ready for bus read and bus write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/busy output (RB)*, *Table 29: Reset AC characteristics*, *Figure 22* and *Figure 23* for more details.

2.10 Ready/busy output ($\overline{RB}$)

The ready/busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations ready/busy is Low, V_{OL} (see *Table 20: Status register bits*). Ready/busy is high-impedance during read mode, auto select mode and erase suspend mode.

After a hardware reset, bus read and bus write operations cannot begin until ready/busy becomes high-impedance. See *Table 29: Reset AC characteristics*, *Figure 22* and *Figure 23*.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/word organization select ($\overline{BYTE}$)

It is used to switch between the x8 and x16 bus modes of the memory. When byte/word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (read, program and erase).

The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus write operations from accidentally damaging the data during power-up, power-down and power surges. If the program/erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 25: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins both of which must be connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are bus read (random and page modes), bus write, output disable, standby and automatic standby.

See *Table 4: Bus operations, 8-bit mode* and *Table 5: Bus operations, 16-bit mode* for a summary. Typical glitches of less than 5 ns on chip enable, write enable, and reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus read

Bus read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in page mode where data is internally read and stored in a page buffer. The page has a size of 8 words (or 16 bytes) and each word in the page is addressed by the address inputs A2-A0 in x 16 mode and A2-A0 plus DQ15A–1 in byte mode.

A valid bus read operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to chip enable and output enable and keeping write enable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 13: Random read AC waveforms (8-bit mode)*, *Figure 16: Page read AC waveforms (16-bit mode)*, and *Table 26: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus write

Bus write operations write to the command interface. A valid bus write operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of chip enable or write enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of chip enable or write enable, whichever occurs first. Output enable must remain High, V_{IH}, during the whole bus write operation. See *Figure 17*, and *Figure 18*, Write AC waveforms, and *Table 27* and *Table 28*, Write AC characteristics, for details of the timing requirements.

3.3 Output disable

The data inputs/outputs are in the high impedance state when output enable is High, V_{IH}.

3.4 Standby

Driving chip enable High in read mode, causes the memory to enter standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the supply current to the standby supply current, I_{CC2}, chip enable should be held within $V_{CC} \pm 0.3$ V. For the standby current level see *Table 25: DC characteristics*.

During program or erase operations the memory will continue to use the program/erase supply current, I_{CC3}, for program or erase operations until the operation completes.

3.5 Reset

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the standby level, independently from the chip enable, output enable or write enable inputs.

3.6 Automatic standby

Automatic standby allows the memory to achieve low power consumption during read mode.

After a read operation, if CMOS levels (V_{CC} ± 0.3 V) are used to drive the bus and the bus is inactive for t_{AVQV} + 30 ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, I_{CC2} (see *Table 25: DC characteristics*). The data inputs/outputs will still output data if a bus read operation is in progress.

The power supplier of data bus, V_{CCQ}, can have a null consumption (depending on load circuits connected with data bus) when the memory enters automatic standby.

3.7 Auto select mode

The auto select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the extended memory block, and apply/remove block protection. For example, this mode can be used by a programming equipment to automatically match a device and the application code to be programmed.

There are two methods to enter auto select mode:

- programmer method:

  Additional bus operations are used. They require V_{ID} to be applied to address pin A9. Refer to *Table 6*, *Table 7*, *Table 8*, and *Table 9* for a description of the bus operations required to read the electronic signature using the programmer method
- in-system method:

  The auto select mode is entered by issuing the Auto Select command (see *Section 6.1.2*). It is not necessary to apply V_{ID} to A9.

At power-up, the device is in read mode, and can then be put in auto select mode by using one of the methods described above.

The device cannot enter auto select mode when a program or erase operation is ongoing ($\overline{RB}$ Low). However, auto select mode can be entered if the erase operation has been suspended by issuing an Erase Suspend command (see *Section 6.1.6*).

The auto select mode is exited by performing a reset. The device is returned to read mode, except if the auto select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the erase or program suspend mode.

3.7.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 6: Read electronic signature - auto select mode -*

programmer method (8-bit mode) and *Table 7: Read electronic signature - auto select mode - programmer method (16-bit mode)*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6.1.2: Auto Select command*).

3.7.2 Verify extended memory block protection indicator

The extended memory block is either factory locked or customer lockable.

The protection status of the extended memory block (factory locked or customer lockable) can be accessed by reading the extended memory block protection indicator. It can be read in auto select mode using either the programmer (see *Table 8* and *Table 9*) or the in-system method (see *Table 10* and *Table 11*).

The protection status of the extended memory block is then output on bit DQ7 of the data input/outputs (see *Table 4* and *Table 5*, Bus operations in 8-bit and 16-bit mode).

3.7.3 Verify block protection status

The protection status of a block can be directly accessed by performing a read operation with control signals and addresses set as shown in *Table 8* and *Table 9*.

If the block is protected, then 01h (in x 8 mode) is output on data input/outputs DQ0-DQ7, otherwise 00h is output.

3.7.4 Hardware block protect

The $V_{PP}/\overline{WP}$ pin can be used to protect the highest or lowest block. When $V_{PP}/\overline{WP}$ is at V_{IL} the highest (M29W128GH) or lowest block (M29W128GL) is protected and remains protected regardless of the block protection status or the reset pin state.

Table 4. Bus operations, 8-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address Inputs	Data inputs/outputs	
						A22-A0, DQ15A-1	DQ14-DQ8	DQ7-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If $\overline{WP}$ is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Bus operations, 16-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs	Data inputs/outputs
						A22-A0	DQ15A-1, DQ14-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If $\overline{WP}$ is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 6. Read electronic signature - auto select mode - programmer method (8-bit mode)

Read cycle(1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs										Data inputs/outputs	
				A22-A10	A9	A8-A7	A6	A5-A4	A3	A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	20h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh (both devices)
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	21h (both devices)
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	01h (M29W128GH) 00h (M29W128GL)

1. X = V_{IL} or V_{IH}.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 7. Read electronic signature - auto select mode - programmer method (16-bit mode)

Read cycle(1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
				A22-A10	A9	A8-A7	A6	A5-A4	A3	A2	A1	A0	DQ15A-1, DQ14-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh (both devices)
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	2221h (both devices)
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h (M29W128GH) 2200h (M29W128GL)

1. X = V_{IL} or V_{IH}.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 8. Block protection - auto select mode - programmer method (8-bit mode)

Operation[1]		$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs	
					A22-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Verify extended memory block protection indicator (bit DQ7)	M29W128GL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	X	X	89h (factory locked) 09h (customer lockable)
	M29W128GH															99h (factory locked) 19h (customer lockable)
Verify block protection status					BAd								V_{IL}			01h (protected) 00h (unprotected)

1. X = V_{IL} or V_{IH}. BAd any address in the block.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 9. Block protection - auto select mode - programmer method (16-bit mode)

Operation[1]		$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
					A22-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1, DQ14-DQ0
Verify extended memory block indicator (bit DQ7)	M29W128GL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	0089h (factory locked) 0009h (customer lockable)
	M29W128GH													0099h (factory locked) 0019h (customer lockable)
Verify block protection status					BAd								V_{IL}	0001h (protected) 0000h (unprotected)

1. X = V_{IL} or V_{IH}. BAd any address in the block.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

4 Hardware protection

The M29W128GH and M29W128GL feature a $V_{PP}/\overline{WP}$ pin that protects the highest or lowest block. Refer to *Section 2: Signal descriptions* for a detailed description of the signal.

5 Software protection

The M29W128GH and M29W128GL have three different software protection modes:

- Volatile protection
- Non-volatile protection
- Password protection

On first use all parts default to operate in non-volatile protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable non-volatile protection mode lock bit, or the password protection mode lock bit of the lock register (see *Section 7.1: Lock register*). Programming the non-volatile protection mode lock bit or the password protection mode lock bit, to '0' will permanently activate the non-volatile or the password protection mode, respectively. These two bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The non-volatile and password protection modes both provide non-volatile protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 6* and *Table 7*) or by issuing an Auto Select command (see *Table 19: Block protection status*).

For the lowest and highest blocks, an even higher level of block protection can be achieved by locking the blocks using the non-volatile protection and then by holding the $V_{PP}/\overline{WP}$ pin Low.

5.1 Volatile protection mode

The volatile protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile protection bits, NVPBs, cleared (erased to '1') (see *Section 5.2: Non-volatile protection mode* and *Section 6.3.5: Non-volatile protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to '0') or cleared (erased to '1'), thus placing each block in the protected or unprotected state respectively. The VPBs can be set (programmed to '0') or cleared (erased to '1') as often as needed.

When the parts are first shipped, or after a power-up or hardware reset, the VPBs can be set or cleared depending upon the ordering option chosen:

- If the option to clear the VPBs after power-up is selected, then the blocks can be programmed or erased depending on the NVPBs state (see *Table 19: Block protection status*)
- If the option to set the VPBs after power-up is selected, the blocks default to be protected.

Refer to *Section 6.3.7* for a description of the volatile protection mode command set.

5.2 Non-volatile protection mode

5.2.1 Non-volatile protection bits

A non-volatile protection bit (NVPB) is assigned to each block.

When a NVPB is set to '0', the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits are set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be cleared all at the same time by issuing a Clear all Non-volatile Protection bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB lock bit (see *Section 5.2.2: Non-volatile protection bit lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to '1'), a few more steps are required:

1. First, the NVPB lock bit must be cleared by either putting the device through a power cycle, or hardware reset
2. The NVPBs can then be changed to reflect the desired settings
3. The NVPB lock bit must be set once again to lock the NVPBs. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding $V_{PP}/\overline{WP}$ Low, V_{IL}.

2 The NVPBs and VPBs have the same function when $V_{PP}/\overline{WP}$ pin is High, V_{IH}, as they do when $V_{PP}/\overline{WP}$ pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 19: Block protection status* and *Figure 5: Software protection scheme* for details on the block protection mechanism, and to *Section 6.3.5* for a description of the non-volatile protection mode command set.

5.2.2 Non-volatile protection bit lock bit

The non-volatile protection bit lock bit (NVPB lock bit) is a global volatile bit for all blocks.

When set (programmed to '0'), it prevents changing the state of the NVPBs. When cleared (programmed to '1'), the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB lock bit per device.

Refer to *Section 6.3.6* for a description of the NVPB lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB lock bit must be set (programmed to '0') only after all NVPBs are configured to the desired settings.

5.3 Password protection mode

The password protection mode provides an even higher level of security than the non-volatile protection mode by requiring a 64-bit password for unlocking the device NVPB lock bit.

In addition to this password requirement, the NVPB lock bit is set '0' after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB lock bit, allowing for block NVPBs to be modified.

If the password provided is not correct, the NVPL lock bit remains locked and the state of the NVPBs cannot be modified.

To place the device in password protection mode, the following steps are required:

1. Prior to entering the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password protection mode command set on page 42*). Password verification is only allowed during the password programming operation
2. The password protection mode is then activated by programming the password protection mode lock bit to '0'. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 19: Block protection status* and *Figure 5: Software protection scheme* for details on the block protection scheme.

Refer to *Section 6.3.4* for a description of the password protection mode command set.

Note: There is no means to verify the password after it is set. If the password is lost after setting the password mode lock bit, there is no way to clear the NVPB lock bit.