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Parallel NOR Flash Embedded Memory

M29W256GH, M29W256GL

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
  - V_{PPH} = 12V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8 words or 16 bytes
  - Page access: 25ns, 30ns
  - Random access: 60ns[1], 70ns, 80ns
- Fast program commands: 32-word (64-byte) write buffer
- Enhanced buffered program commands: 256-word
- Program time
  - 16µs per byte/word (TYP)
  - Chip program time: 10s with V_{PPH} and 16s without V_{PPH}
- Memory organization
  - Uniform blocks: 256 main blocks, 128KB, or 64-Kwords each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume capability
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, write to buffer and program
  - Fast buffered/batch programming
  - Fast block/chip erase
- V_{PP}/WP# pin protection
  - Protects first or last block regardless of block -protection settings
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - 128-word (256-byte) memory block for permanent, secure identification
  - Programmed or locked at the factory or by the customer
- Common Flash interface
  - 64-bit security code
- Low power consumption: Standby and automatic mode
- JESD47H-compliant
  - 100,000 minimum PROGRAM/ERASE cycles per block
  - Data retention: 20 years (TYP)
- 65nm single-level cell (SLC) process technology
- Fortified BGA, TBGA, and TSOP packages
- "Green" packages available
  - RoHS-compliant
  - Halogen-free
- Automotive device grade (6) temperature: –40°C to +85°C (automotive grade-certified)
- Automotive device grade (3) temperature: –40°C to +125°C (automotive grade-certified)

Note: 1. The 60ns device is available upon customer request.

Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details	Notes
Device type	M29W	
Operating voltage	W = V_{CC} = 2.7 to 3.6V	
Device function	256GH = 256Mb (x8/x16) page, uniform block Flash memory, highest block protected by V_{PP}/WP#	
	256GL = 256Mb (x8/x16) page, uniform block Flash memory, lowest block protected by V_{PP}/WP#	
Speed	70 = 70ns	1
	60 = 60ns	1, 2
	7A = 70ns	1, 3
Package	N = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant	
	ZA = 64-ball TBGA, 10mm x 13mm, lead-free, halogen-free, RoHS-compliant	
	ZS = 64-ball fortified BGA, 11mm x 13mm	
Temperature range	1 = 0 to 70°C	
	6 = –40°C to +85°C	
	3 = –40°C to +125°C	
Shipping options	E = RoHS-compliant package, standard packing	
	F = RoHS-compliant package, tape and reel packing	

Notes:
1. 80ns if V_{CCQ} = 1.65V to V_{CC}.
2. The 60ns device is available upon customer request.
3. Automotive-qualified, available only with option 6. Qualified and characterized according to AEC Q100 and Q003 or equivalent; advanced screening according to AEC Q001 and Q002 or equivalent.

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General Description

The M29W is an asynchronous, uniform block, parallel NOR Flash memory device manufactured on 65nm single-level cell (SLC) technology. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

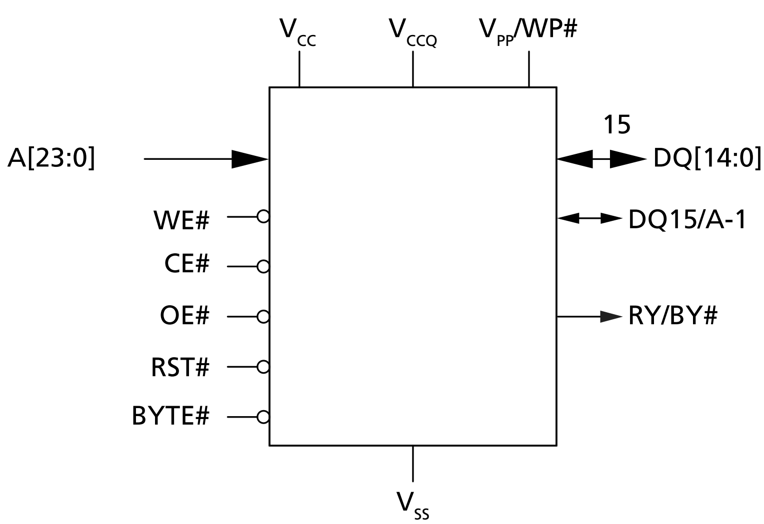
The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected, and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The M29W supports asynchronous random read and page read from all blocks of the array. It features a write to buffer program capability that improves throughput by programming a buffer of 32 words in one command sequence. Also, in x16 mode, the enhanced buffered program capability improves throughput by programming 256 words in one command sequence. The device V_{PP}/WP# signal enables faster programming.

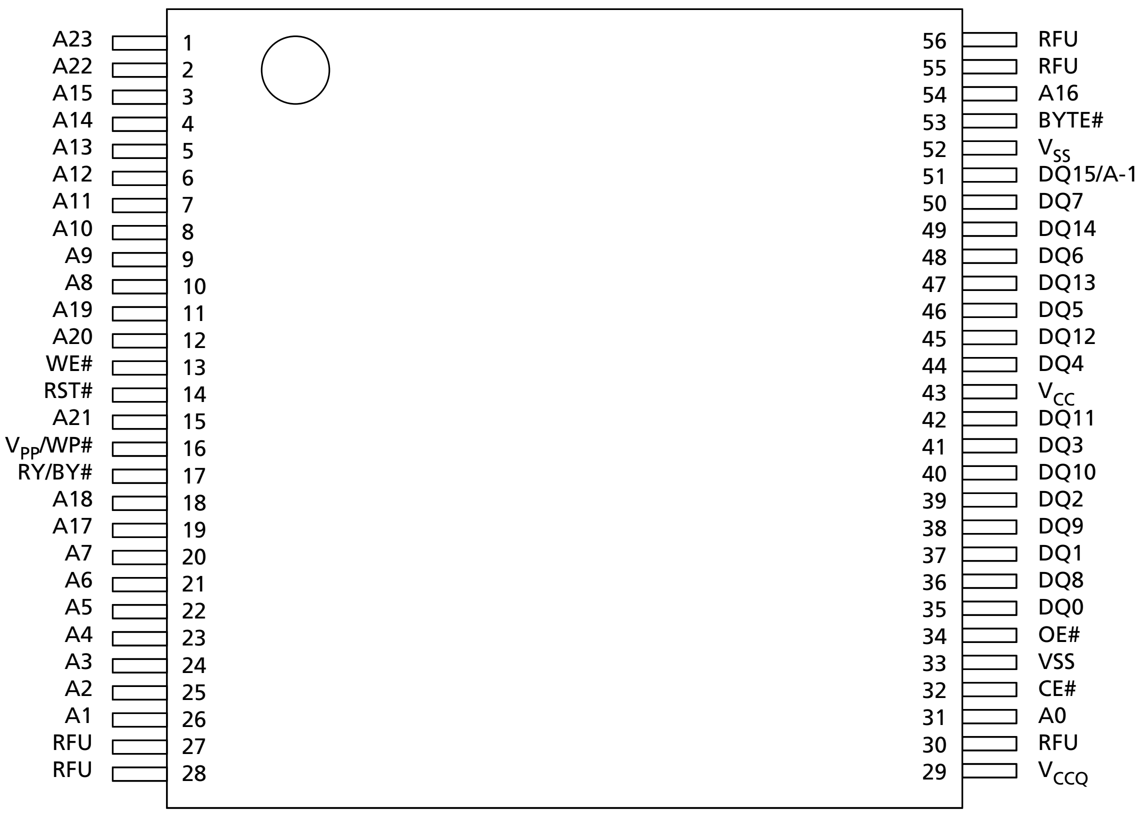
The device contains a 128-word (x16) and 256-byte (x8) extended memory block. The user can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Figure 1: Logic Diagram



Signal Assignments

Figure 2: 56-Pin TSOP (Top View)



Notes:
1. A23 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 3: 64-Ball Fortified BGA and 64-Ball TBGA

Top view – ball side down

	1	2	3	4	5	6	7	8
A	RFU	A3	A7	RY/BY#	WE#	A9	A13	RFU
B	RFU	A4	A17	V_{PP}/WP#	RST#	A8	A12	A22
C	RFU	A2	A6	A18	A21	A10	A14	A23
D	RFU	A1	A5	A20	A19	A11	A15	V_{CCQ}
E	RFU	A0	D0	D2	D5	D7	A16	V_{SS}
F	V_{CCQ}	CE#	D8	D10	D12	D14	BYTE#	RFU
G	RFU	OE#	D9	D11	V_{CC}	D13	D15/A-1	RFU
H	RFU	V_{SS}	D1	D3	D4	D6	V_{SS}	RFU

Bottom view – ball side up

8	7	6	5	4	3	2	1	
RFU	A13	A9	WE#	RY/BY#	A7	A3	RFU	A
A22	A12	A8	RST#	V_{PP}/WP#	A17	A4	RFU	B
A23	A14	A10	A21	A18	A6	A2	RFU	C
V_{CCQ}	A15	A11	A19	A20	A5	A1	RFU	D
V_{SS}	A16	D7	D5	D2	D0	A0	RFU	E
RFU	BYTE#	D14	D12	D10	D8	CE#	V_{CCQ}	F
RFU	D15/A-1	D13	V_{CC}	D11	D9	OE#	RFU	G
RFU	V_{SS}	D6	D4	D3	D1	V_{SS}	RFU	H

Notes:
1. A[23] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 2: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby, and data outputs are at High-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/write protect:** Provides WRITE PROTECT function and V_{PPH} function. These functions protect the lowest or highest block and enable the device to enter unlock bypass mode, respectively. (Refer to Hardware Protection and Bypass Operations for details.)
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). (See RESET AC Specifications for more details.)
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).
RY/BY#	Output	**Ready/busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z. (See RESET AC Specifications for more details.) The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10,000Ω or higher resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

Table 2: Signal Descriptions (Continued)

Name	Type	Description
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when $V_{CC} \leq V_{LKO}$. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts, and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations. (See DC Characteristics.)
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map – 256Mb Density

Table 3: 256Mb, Blocks[255:0]

Block	Block Size	Address Range (x8)		Block Size	Address Range (x16)	
		Start	End		Start	End
255	128KB	1FE 0000h	1FF FFFFh	64KW	0FF 0000h	0FF FFFFh
⋮		⋮	⋮		⋮	⋮
127		0FE 0000h	0FF FFFFh		07F 0000h	07F FFFFh
⋮		⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh		03F 0000h	03F FFFFh
⋮		⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh		000 0000h	000 FFFFh

Bus Operations

Table 4: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode: A[MAX:0], DQ15/A-1	8-Bit Mode: DQ[14:8]	8-Bit Mode: DQ[7:0]	16-Bit Mode: A[MAX:0]	16-Bit Mode: DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	H	X[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	X	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

The page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page read mode.

A valid READ operation requires setting the appropriate address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. Data I/O signals output the value.

Write

Bus WRITE operations write to the command interface. A valid WRITE operation requires setting the appropriate address on the address inputs. These are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. Values on data I/O signals are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire operation.

Standby and Automatic Standby

When the device is in read mode, driving CE# HIGH places the device in standby mode and drives data I/Os to High-Z. Supply current is reduced to standby (I_{CC2}) by holding CE# within V_{CC} ±0.3V.

During PROGRAM or ERASE operations, the device continues to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic standby enables low power consumption during read mode. When CMOS levels (V_{CC} ± 0.3 V) drive the bus, and following a READ operation and a period of inactivity specified in DC Characteristics, the memory enters automatic standby as internal supply current is reduced to I_{CC2}. Data I/O signals still output data if a READ operation is in progress. Depending on load circuits connected with data bus, V_{CCQ} can have a null consumption when the memory enters automatic standby.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode, the device is deselected, and outputs are High-Z. The device is in reset mode when RST# is LOW. Power consumption is reduced to standby level independently from CE#, OE#, or WE# inputs.

Registers

Status Register

Table 5: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM or ERASE operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.

6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

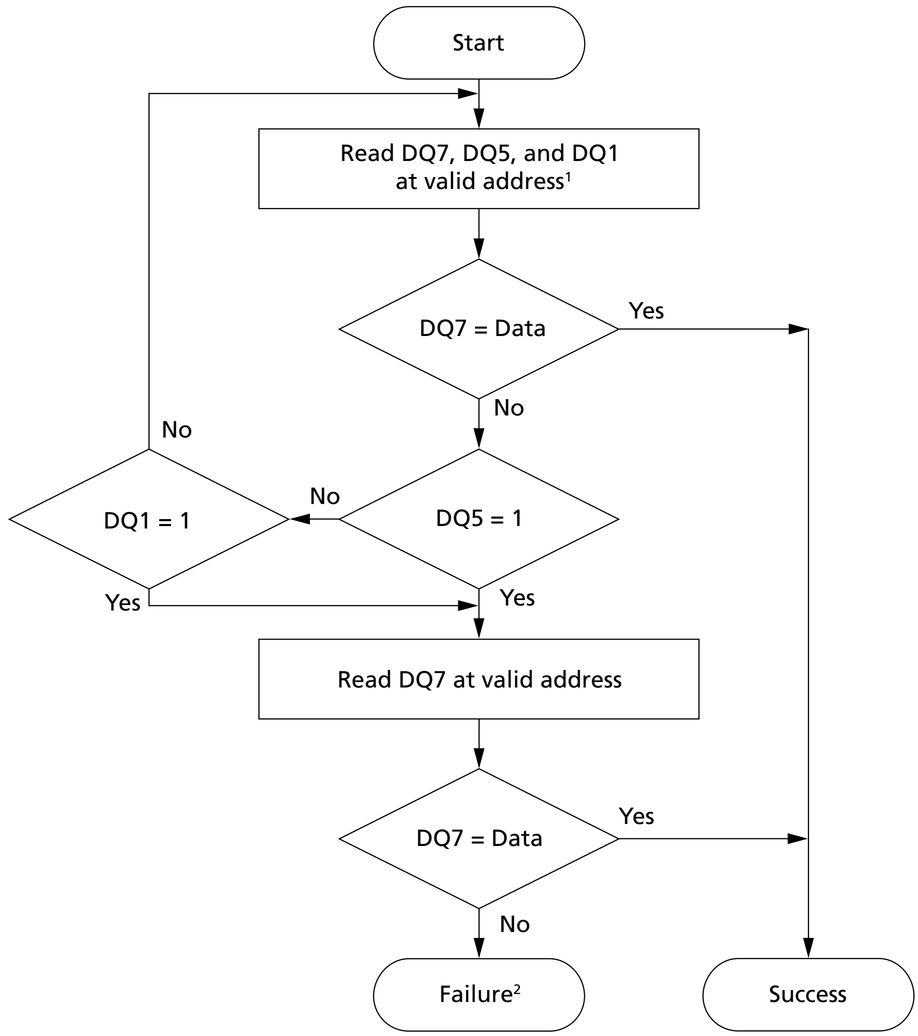
Table 6: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	No toggle	0	0	2
PROGRAM during ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	–	0	
ENHANCED BUFFERED PROGRAM	Any address	–	Toggle	0	–	–	–	0	
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	0	2
PROGRAM error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
ERASE SUSPEND	Erasing block	1	No toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode					–	High-Z	
BLOCK ERASE error	Good block address	0	Toggle	1	1	No toggle	–	High-Z	
	Faulty block address	0	Toggle	1	1	Toggle	–	High-Z	

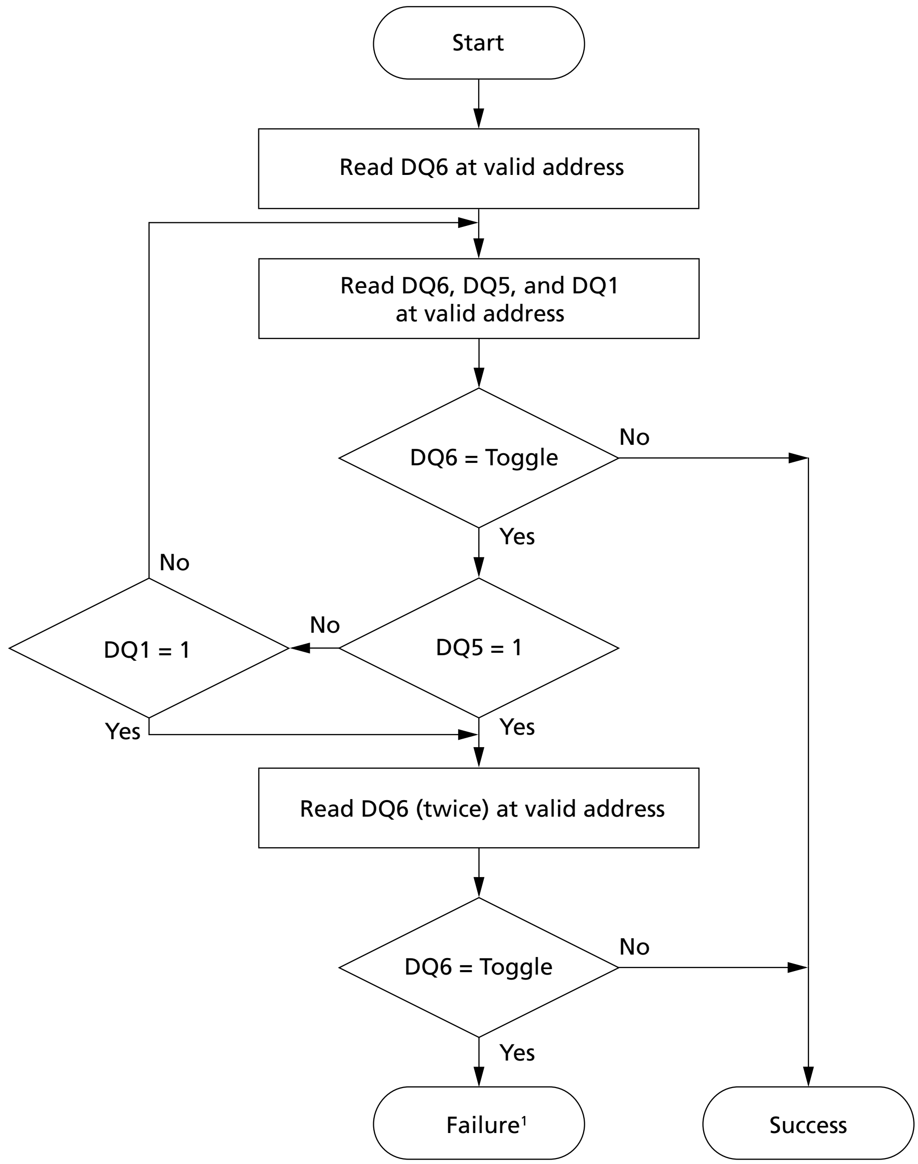
Notes:
1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

Figure 4: Data Polling Flowchart



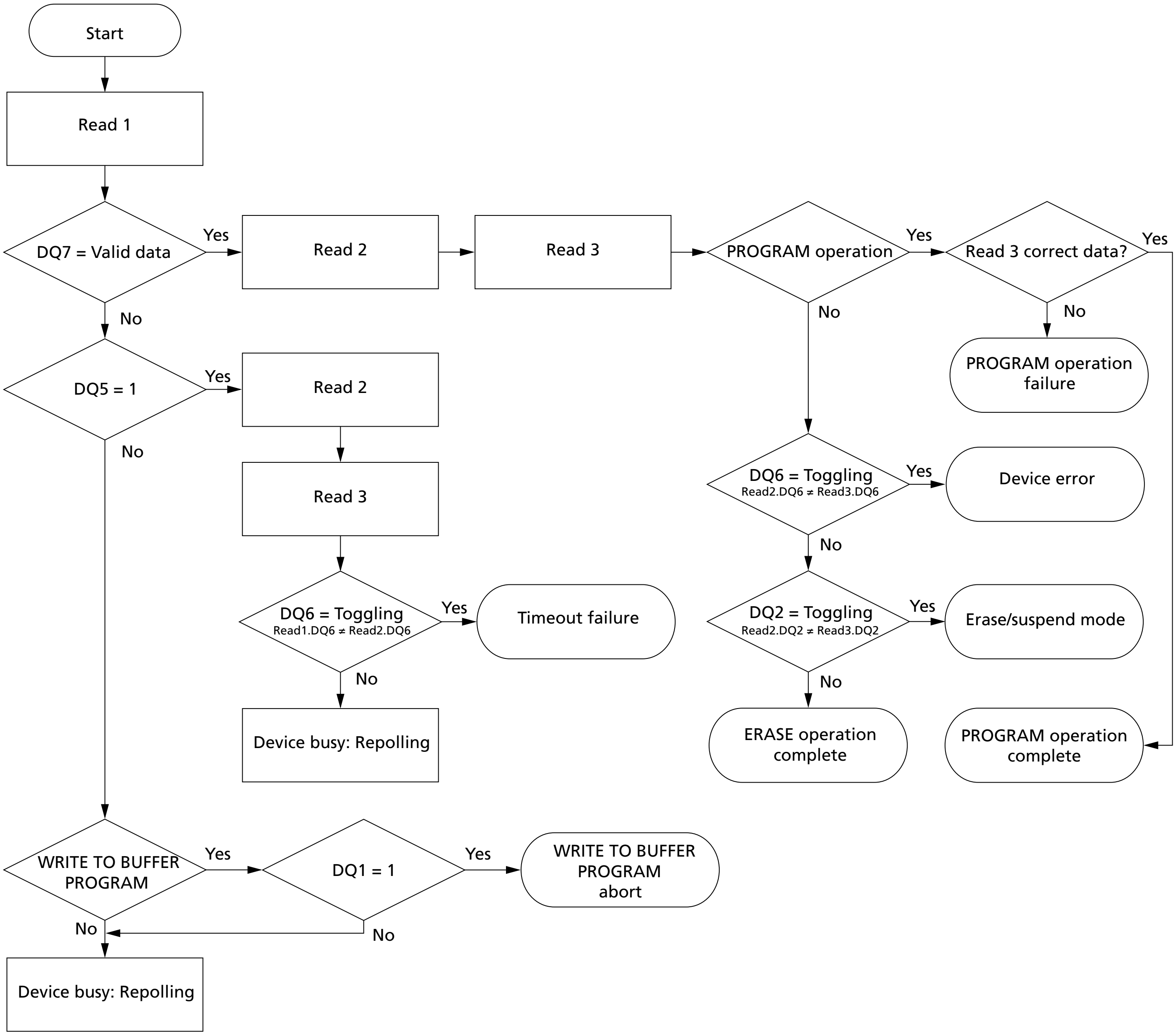
Notes:
1. Valid address is the address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 5: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 6: Status Register Polling Flowchart



Lock Register

Table 7: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

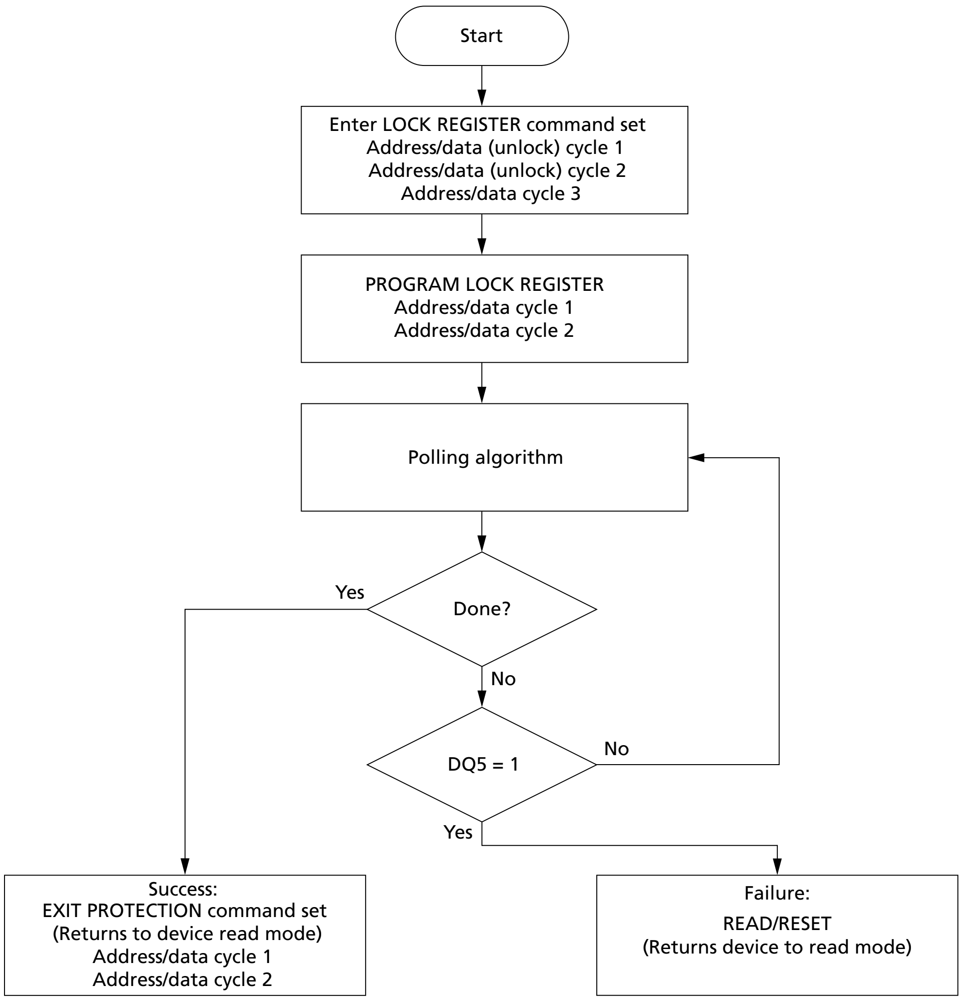
Table 8: Block Protection Status

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
1	1	1	00h	Block unprotected; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.
1	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit changeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
0	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.
0	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit unchangeable.

Notes:
1. Nonvolatile protection bit lock bit: when cleared to 1, all nonvolatile protection bits are unlocked; when set to 0, all nonvolatile protection bits are locked.

2. Block nonvolatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
3. Block volatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.

Figure 7: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address/data cycle details.

Standard Command Definitions – Address/Data Cycles

Table 9: Standard Command Definitions – Address/Data Cycles, 8-Bit and 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x8	X	F0											
		AAA	AA	555	55	X	F0							
	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x8	AA	98											
	x16	55												
AUTO SELECT (90h)	x8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2, 3, 4
	x16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	x8	AAA	AA	555	55	AAA	20							
	x16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	x8	X	90	X	00									
	x16													
PROGRAM Operations														
PROGRAM (A0h)	x8	AAA	AA	555	55	AAA	A0	PA	PD					
	x16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	x8	X	A0	PA	PD									5
	x16													
WRITE TO BUFFER PROGRAM (25h)	x8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			6, 7, 8
	x16	555		2AA										
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x8	BAd	25	BAd	N	PA	PD							5
	x16													
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											
	x16													
BUFFERED PROGRAM ABORT and RESET (F0h)	x8	AAA	AA	555	55	AAA	F0							
	x16	555		2AA		555								
ENTER ENHANCED BUFFERED PROGRAM (38h)	x8	NA												
	x16	555	AA	2AA	55	555	38							
ENHANCED BUFFERED PROGRAM (33h)	x8	NA												9
	x16	BAd	33	BAd (00)	Data	BAd (01)	Data							

Table 9: Standard Command Definitions – Address/Data Cycles, 8-Bit and 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
EXIT ENHANCED BUFFERED PROGRAM (90h)	x8	NA												
	x16	X	90	X	00									
ENHANCED BUFFERED PROGRAM ABORT (F0h)	x8	NA												
	x16	555	AA	2AA	55	555	F0							
PROGRAM SUSPEND (B0h)	x8	X	B0											
	x16													
PROGRAM RESUME (30h)	x8	X	30											
	x16													
ERASE Operations														
CHIP ERASE (80/10h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	x16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	x8	X	80	X	10									5
	x16													
BLOCK ERASE (80/30h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	10
	x16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	x8	X	80	BAd	30									5
	x16													
ERASE SUSPEND (B0h)	x8	X	B0											
	x16													
ERASE RESUME (30h)	x8	X	30											
	x16													

Notes:
1. A = Address; D = Data; X = "Don't Care"; BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. These cells represent READ cycles (versus WRITE cycles for the others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM third and fourth cycles.
7. WRITE TO BUFFER PROGRAM operation: maximum cycles = 68 (x8) and 36 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 66 (x8) and 34

(x16). WRITE TO BUFFER PROGRAM operation: N + 1 = bytes to be programmed; maximum buffer size = 64 bytes (x8) and 32 words (x16).

8. For x8, A[MAX:5] address pins should remain unchanged while A[4:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:5] address pins should remain unchanged while A[4:0] pins are used to select a word within the N + 1 word page.
9. The following is content for address/data cycles 256 through 258: BAd (FE) - Data; BAd (FF) - Data; BAd (00) - 29.
10. BLOCK ERASE address cycles can extend beyond six address/data cycles, depending on the number of blocks to erase.

READ Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is valid only when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area. A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

AUTO SELECT Operations

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command or by applying V_{ID} to A9. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information, as shown in the Electronic Signature table.
- Block protection, which includes the block protection status and extended memory block protection indicator, as shown in the Block Protection table.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set, as shown in the Read Electronic Signature table or the Block Protection table, respectively.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

To enter auto select mode by appling V_{ID} to A9, see the Read Electronic Signature table and the Block Protection table.

Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 10: Read Electronic Signature

Note 1 applies to entire table

Signal	READ Cycle				Notes
	Manufacturer Code	Device Code 1	Device Code 2	Device Code 3	
CE#	L	L	L	L	
OE#	L	L	L	L	
WE#	H	H	H	H	
Address Input, 8-Bit and 16-Bit					
A[MAX:10]	X	X	X	X	
A9	V_{ID}	V_{ID}	V_{ID}	V_{ID}	2
A8	X	X	X	X	
A[7:5]	L	L	L	L	
A4	X	X	X	X	
A[3:1]	L	L	H	H	

Table 10: Read Electronic Signature (Continued)

Note 1 applies to entire table

Signal	READ Cycle				Notes
	Manufacturer Code	Device Code 1	Device Code 2	Device Code 3	
A0	L	H	L	H	
Address Input, 8-Bit Only					
DQ[15]/A-1	X	X	X	X	
Data I/O, 8-Bit Only					
DQ[14:8]	X	X	X	X	
DQ[7:0]	20h	7Eh	22h	01h	
Data I/O, 16-Bit Only					
DQ[15]/A-1, and DQ[14:0]	0020h	227Eh	2222h	2201h	

Notes:
1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. When using the AUTO SELECT command to enter auto select mode, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.