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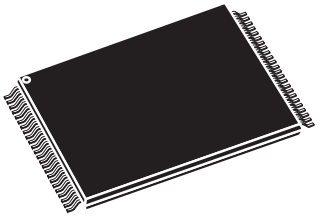
M29W320ET
M29W320EB

32 Mbit (4Mbx8 or 2Mbx16, Uniform Parameter Blocks, Boot Block) 3V supply Flash memory

Features

- Supply voltage
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
  - V_{PP} =12V for Fast Program (optional)
- Access times: 70, 90ns
- Programming time
  - 10µs per byte/word typical
  - Double word/ Quadruple byte Program
- Memory Blocks
  - Memory Array: 63 Main Blocks
  - 8 Parameter Blocks (Top or Bottom Location)
- Erase Suspend and Resume modes
  - Read and Program another Block during Erase Suspend
- Unlock Bypass Program command
  - Faster Production/Batch Programming
- $V_{PP}/\overline{WP}$ pin for fast Program and Write Protect
- Temporary Block Unprotection mode
- Common Flash Interface
  - 64 bit Security code
- Extended memory Block
  - Extra block used as security block or to store additional information
- Low power consumption
  - Standby and Automatic Standby
- 100,000 Program/Erase cycles per block
- Electronic signature
  - Manufacturer code: 0020h
  - Top Device code M29W320ET: 2256h
  - Bottom Device code M29W320EB: 2257h
- RoHS® packages available



TSOP48 (N)
12 x 20 mm

TFBGA48 (ZE)
6 x 8 mm

FBGA64 (ZS)
11 x 13 mm

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1 Description

The M29W320E is a 32 Mbit (4Mb x8 or 2Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode.

The device features an asymmetrical block architecture. The M29W320E has an array of 8 parameter and 63 main blocks. M29W320ET locates the Parameter Blocks at the top of the memory address space while the M29W320EB locates the Parameter Blocks starting from the bottom.

M29W320E has an extra 32 Kword (x16 mode) or 64 Kbyte (x8 mode) block, the Extended Block, that can be accessed using a dedicated command. The Extended Block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently so it is possible to preserve valid data while old data is erased. The blocks can be protected to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12x20mm), and TFBGA48 (6x8mm, 0.8mm pitch) packages. In order to meet environmental requirements, Numonyx offers the M29W320E in RoHS packages, which are are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

The memory is supplied with all the bits erased (set to ’1’).

Figure 1. Logic diagram

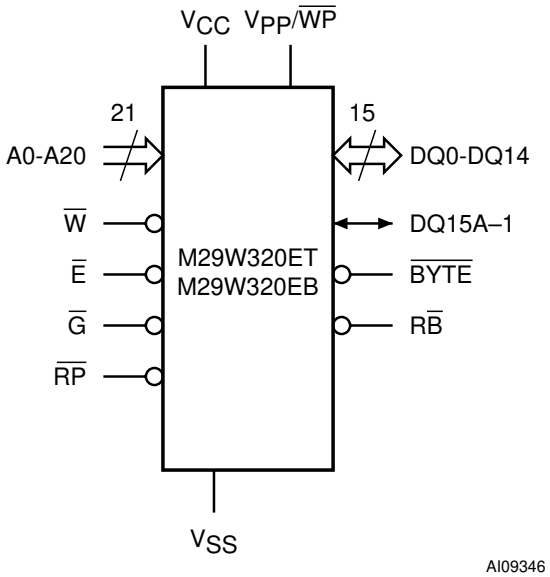


Table 1. Signal names

A0-A20	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/word Organization Select
V_{CC}	Supply voltage
$V_{PP}/\overline{WP}$	V_{PP}/Write Protect
V_{SS}	Ground
NC	Not Connected Internally

Figure 2. TSOP connections

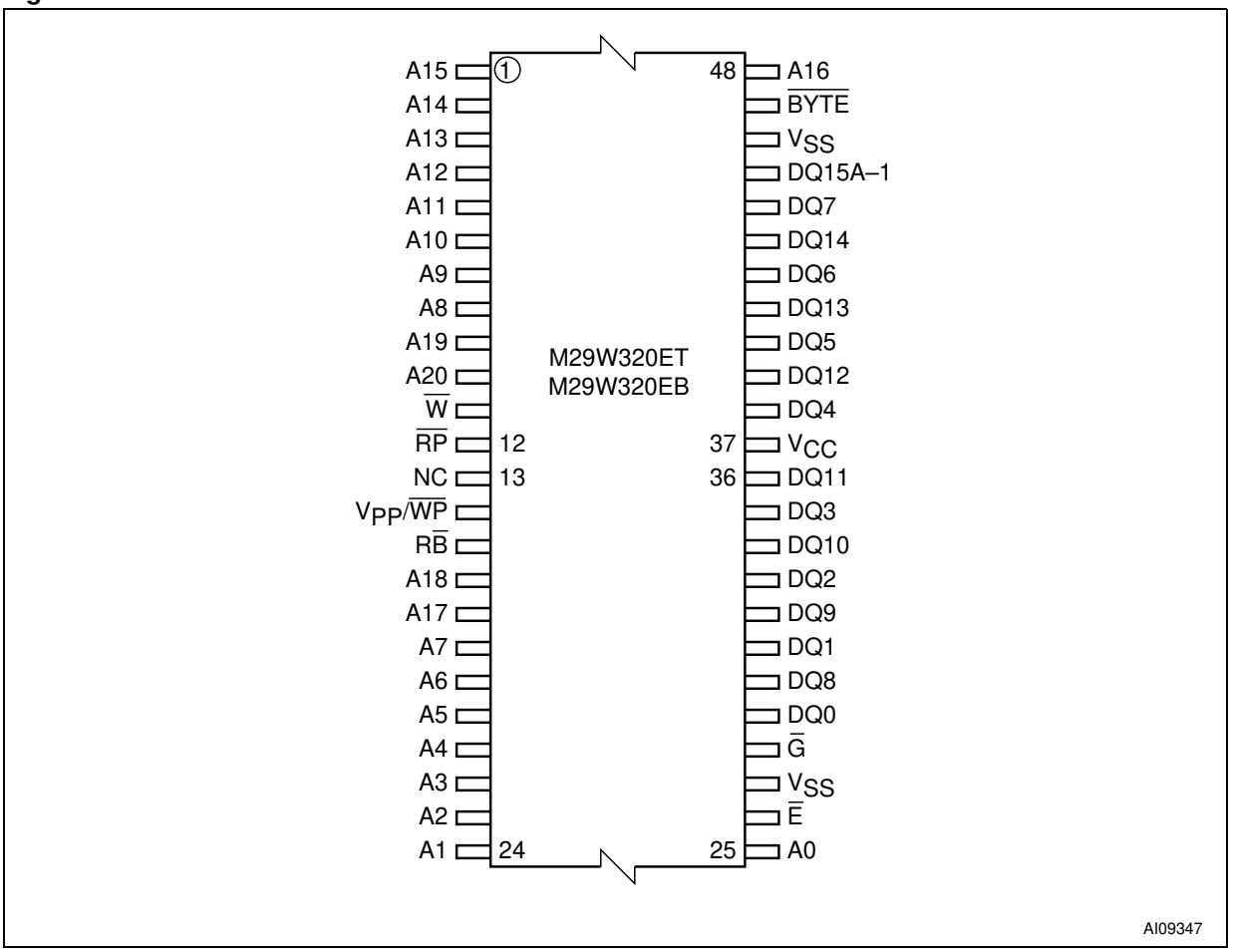


Figure 3. TFBGA48 connections (top view through package)

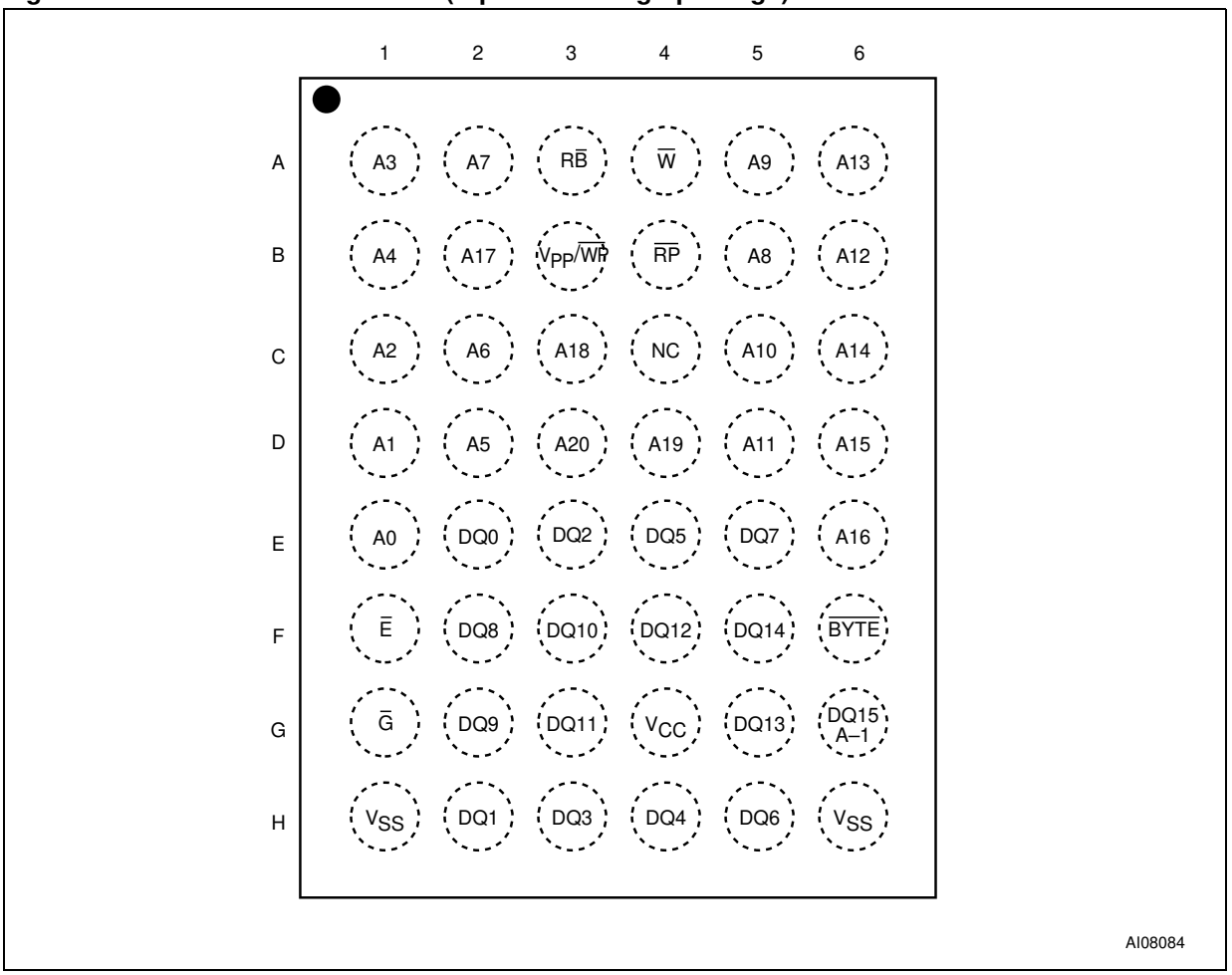


Figure 4. FBGA64 connections (top view through package)

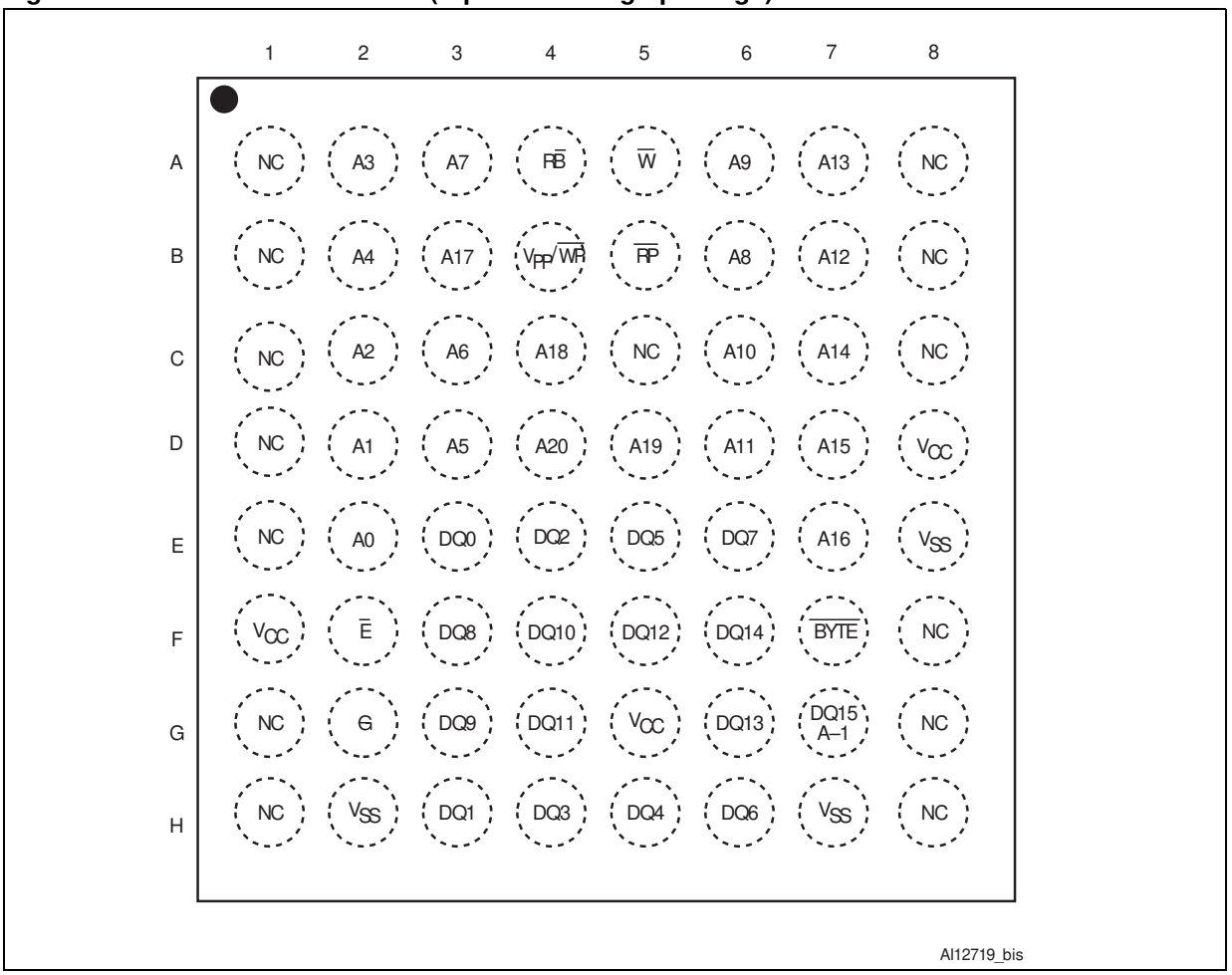
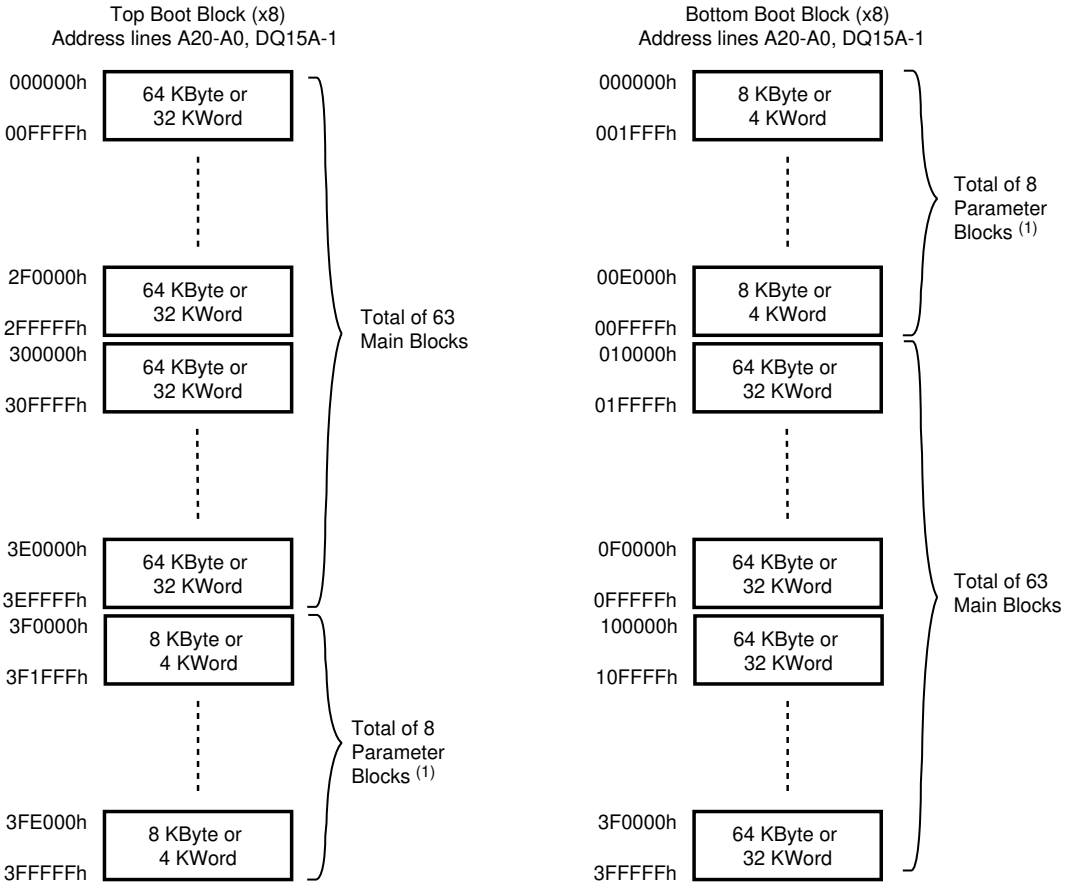
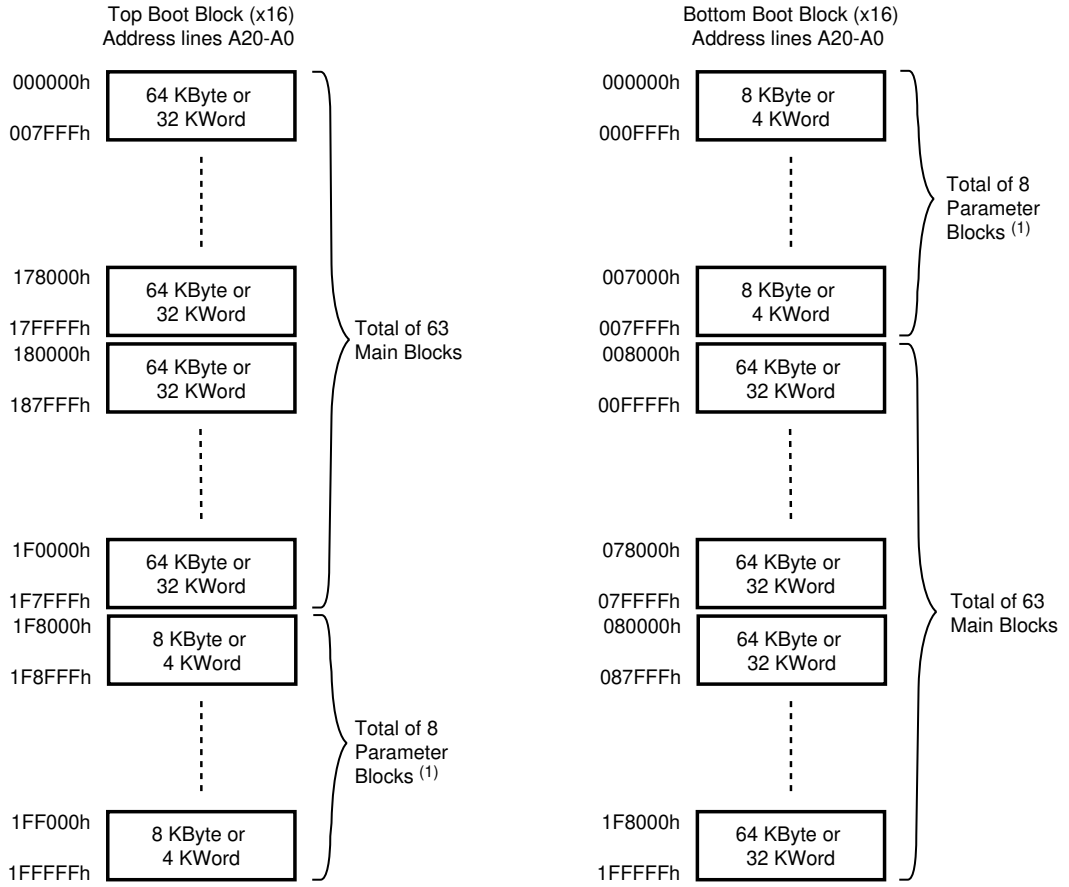


Figure 5. Block Addresses (x8)



1. See also *Appendix A: Block Addresses*, *Table 21* and *Table 22* for a full listing of the Block Addresses.

Figure 6. Block Addresses (x16)



Note 1. Used as Extended Block Addresses in Extended Block mode.

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1. See also *Appendix A: Block Addresses*, *Table 21* and *Table 22* for a full listing of the Block Addresses.

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A20)

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command interface of the Program/Erase Controller.

2.2 Data Inputs/Outputs (DQ0-DQ7)

The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command interface of the Program/Erase Controller.

2.3 Data Inputs/Outputs (DQ8-DQ14)

The Data I/O outputs the data stored at the selected address during a Bus Read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status register these bits should be ignored.

2.4 Data Input/Output or Address Input (DQ15A–1)

When $\overline{BYTE}$ is High, V_{IH}, this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When $\overline{BYTE}$ is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the addressed word, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when $\overline{BYTE}$ is High and references to the Address Inputs to include this pin when $\overline{BYTE}$ is Low except when stated explicitly otherwise.

2.5 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

2.7 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command interface.

2.8 V_{PP}/Write Protect ($V_{PP}/\overline{WP}$)

The V_{PP}/Write Protect pin provides two functions. The V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for Program operations. This is achieved by bypassing the unlock cycles and/or using the Double word or Quadruple byte Program commands.

The Write Protect function provides a hardware method of protecting the two outermost boot blocks. When V_{PP}/Write Protect is Low, V_{IL}, the memory protects the two outermost boot blocks; Program and Erase operations in these blocks are ignored while V_{PP}/Write Protect is Low, even when $\overline{RP}$ is at V_{ID}.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the two outermost boot blocks. Program and Erase operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

When V_{PP}/Write Protect is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the Command interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}, see *Figure 17*

Never raise V_{PP}/Write Protect to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

The V_{PP}/Write Protect pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

2.9 Reset/Block Temporary Unprotect ($\overline{RP}$)

The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if $V_{PP}/\overline{WP}$ is at V_{IL}, then the two outermost boot blocks will remain protected even if RP is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, *Table 16* and *Figure 16: Reset/Block Temporary Unprotect ac waveforms*, for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

2.10 Ready/Busy Output ($\overline{RB}$)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 16* and *Figure 16: Reset/Block Temporary Unprotect ac waveforms*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/word Organization Select ($\overline{BYTE}$)

The byte/word Organization Select pin is used to switch between the x8 and x16 Bus modes of the memory. When byte/word Organization Select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} Supply voltage

V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command interface is disabled when the V_{CC} Supply voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase operations, I_{CC3}.

2.13 V_{SS} Ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins which must be both connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby.

See *Table 2* and *Table 3*, Bus operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the Command interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see *Figure 11: Read mode ac waveforms*, and *Table 12: Read ac characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the Command interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 12* and *Figure 13*, Write ac waveforms, and *Table 13* and *Table 14*, Write ac characteristics, for details of the timing requirements.

3.3 Output Disable

The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply current to the Standby Supply current, I_{CC2}, Chip Enable should be held within V_{CC} ± 0.2V. For the Standby current level see *Table 11: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply current, I_{CC3}, for Program or Erase operations until the operation completes.

3.5 Automatic Standby

If CMOS levels (V_{CC} ± 0.2V) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply current is reduced to the Standby Supply current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

3.6 Special bus operations

Additional bus operations can be performed to read the Electronic signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.6.1 Electronic signature

The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in *Table 2* and *Table 3*, Bus operations.

3.6.2 Block Protect and Chip Unprotect

Groups of blocks can be protected against accidental Program or Erase. The Protection groups are shown in *Appendix A: Block Addresses*, *Table 21* and *Table 22*, Block Addresses. The whole chip can be unprotected to allow the data inside the blocks to be changed.

The V_{PP}/Write Protect pin can be used to protect the two outermost boot blocks. When V_{PP}/Write Protect is at V_{IL} the two outermost boot blocks are protected and remain protected regardless of the Block Protection Status or the Reset/Block Temporary Unprotect pin status.

Block Protect and Chip Unprotect operations are described in *Appendix D: Block Protection*.

Table 2. Bus operations, $\overline{BYTE}$ = V_{IL} (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs DQ15A–1, A0-A20	Data Inputs/Outputs	
					DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Hi-Z	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Hi-Z	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z
Read Manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	20h
Read Device code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	56h (M29W320ET) 57h (M29W320EB)
Extended memory Block Verify code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	81h (factory locked) 01h (factory unlocked)

1. X = V_{IL} or V_{IH}.

Table 3. Bus operations, $\overline{BYTE}$ = V_{IH} (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A20	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	0020h
Read Device code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	2256h (M29W320ET) 2257h (M29W320EB)
Extended memory Block Verify code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	81h (factory locked) 01h (factory unlocked)

1. X = V_{IL} or V_{IH}.

4 Command interface

All Bus Write operations to the memory are interpreted by the Command interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode. See either *Table 4*, or *Table 5*, depending on the configuration that is being used, for a summary of the commands.

4.1 Read/Reset command

The Read/Reset command returns the memory to its Read mode. It also resets the errors in the Status register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the time-out of a Block erase operation then the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

4.2 Auto Select command

The Auto Select command is used to read the Manufacturer code, the Device code, the Block Protection Status and the Extended memory Block Verify code. Three consecutive Bus Write operations are required to issue the Auto Select command. The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

In Auto Select mode the Manufacturer code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Device code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH} and A12-A20 specifying the block address. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

4.3 Read CFI Query command

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) memory Area. This command is valid when the device is in the Read Array mode, or when the device is in Auto Select mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface memory Area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Auto Select mode.

See *Appendix B: Common Flash Interface (CFI)*, *Table 23*, *Table 24*, *Table 25*, *Table 26*, *Table 27* and *Table 28* for details on the information contained in the Common Flash Interface (CFI) memory area.

4.4 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. After programming has started, Bus Read operations output the Status register content. See *Section 5: Status register* for more details. Typical program times are given in *Table 6*

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations will continue to output the Status register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at ’0’ back to ’1’. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

4.5 Fast Program commands

There are two Fast Program commands available to improve the programming throughput, by writing several adjacent words or bytes in parallel. The Quadruple byte Program command is available for x8 operations, while the Double word Program command is available for x16 operations.

Fast Program commands should not be attempted when $V_{PP}/\overline{WP}$ is not at V_{PP}. Care must be taken because applying a 12V V_{PP} voltage to the VPP/$\overline{WP}$ pin will temporarily unprotect any protected block.

After programming has started, Bus Read operations output the Status register content.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations will continue to output the Status register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Fast Program commands cannot change a bit set at ’0’ back to ’1’. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

Typical Program times are given in *Table 6: Program, Erase times and Program, Erase Endurance cycles*

4.5.1 Quadruple byte Program command

The Quadruple byte Program command is used to write a page of four adjacent bytes in parallel. The four bytes must differ only for addresses A0, DQ15A-1. Five bus write cycles are necessary to issue the Quadruple byte Program command.

1. The first bus cycle sets up the Quadruple byte Program command.
2. The second bus cycle latches the Address and the Data of the first byte to be written.
3. The third bus cycle latches the Address and the Data of the second byte to be written.
4. The fourth bus cycle latches the Address and the Data of the third byte to be written.
5. The fifth bus cycle latches the Address and the Data of the fourth byte to be written and starts the Program/Erase Controller.

4.5.2 Double word Program command

The Double word Program command is used to write a page of two adjacent words in parallel. The two words must differ only for the address A0.

Three bus write cycles are necessary to issue the Double word Program command.

1. The first bus cycle sets up the Double word Program command.
2. The second bus cycle latches the Address and the Data of the first word to be written.
3. The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

4.6 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory enters Unlock Bypass mode. The Unlock Bypass Program command can then be issued to program addresses or the Unlock Bypass Reset command can be issued to return to Read mode. In Unlock Bypass mode the memory can be read as if in Read mode.

When V_{PP} is applied to the V_{PP}/Write Protect pin the memory automatically enters the Unlock Bypass mode and the Unlock Bypass Program command can be issued immediately. Care must be taken because applying a 12V V_{PP} voltage to the VPP/$\overline{WP}$ pin will temporarily unprotect any protected block.

4.7 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted, a Bus Read operation outputs the Status register. See the Program command for details on the behavior.

4.8 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass mode.

4.9 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 6*. All Bus Read operations during the Chip Erase operation will output the Status register on the Data Inputs/Outputs. See the section on the Status register for more details.

After the Chip Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the

Status register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

4.10 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller after a time-out period of 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. After the sixth Bus Write operation a Bus Read operation will output the Status register. See the Status register section for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the 50µs time-out period. Typical block erase times are given in *Table 6*.

After the Erase operation has started all Bus Read operations will output the Status register on the Data Inputs/Outputs. See the section on the Status register for more details.

After the Block Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations will continue to output the Status register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

4.11 Erase Suspend command

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within the Erase Suspend Latency time of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.