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Parallel NOR Flash Embedded Memory

M29W640FT, M29W640FB

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{PP} = 12V for fast program (optional)
- Asynchronous random/page read
  - Page width: 4 words
  - Page access: 25ns
  - Random access: 60ns, 70ns
- Program time
  - 10µs per byte/word TYP
  - 4 words/8 bytes program
- Memory organization
  - 135 memory blocks
  - 1 boot block and 7 parameter blocks, 8KB each (top or bottom)
  - 127 main blocks, 64KB each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- UNLOCK BYPASS PROGRAM command
  - Faster production/batch programming
- V_{PP}/WP# pin for fast program and write protect
- Temporary block unprotection mode
- Common Flash interface
  - 64-bit security code
- Extended memory block
  - Extra block used as security block or to store additional information
- Low power consumption
  - Standby and automatic standby
- 100,000 PROGRAM/ERASE cycles per block
- Electronic signature
  - Manufacturer code: 0020h
  - Device code M29W640FT: 22EDh
  - Device code M29W640FB: 22FDh
- RoHS-compliant packages
  - 48-pin TSOP (N) 12mm x 20mm
  - 48-ball TFBGA (ZA) 6mm x 8mm

Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or speed, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details
Device Type	M29 = Parallel Flash memory
Operating Voltage	W = V_{CC} = 2.7 to 3.6V
Device Function	640F = 64Mb (x8/x16) boot block
Array Matrix	T = Top boot
	B = Bottom boot
Speed	60 = 60ns
	70 = 70ns
Package	N = 48-pin TSOP: 12mm x 20mm
	ZA = 48-ball TFBGA, 6mm x 8mm, 0.80mm pitch
Temperature Range	6 = –40°C to 85°C
Shipping Options	E = RoHS-compliant package, standard packing
	F = RoHS-compliant package, tape and reel packing

Contents

List of Figures

List of Tables

General Description

The M29W640F is a 64Mb (8Mb x8 or 4Mb x16) nonvolatile memory that can be read, erased, and reprogrammed. These operations can be performed using a single low voltage (2.7–3.6V) supply. On power-up, the memory defaults to read mode.

The memory is divided into blocks that can be erased independently so that valid data can be preserved while old data is erased. Blocks can be protected in units of 256KB (typically, groups of four 64KB blocks), to prevent accidental PROGRAM or ERASE commands from modifying the memory. PROGRAM and ERASE commands are written to the command interface. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The device features an asymmetrical blocked architecture. The device has an array of 135 blocks: 8 parameters blocks of 8KB each (or 4 K words each) and 127 main blocks of 64KB each (or 32K words each)

M29W640FT contains the parameter blocks at the top of the memory address space. The M29W640FB contains the parameter blocks starting from the bottom.

The M29W640F has an extra block, the extended block, of 128 words in x16 mode, or of 256 bytes in x8 mode, that can be accessed using a dedicated command. The extended block can be protected. It is useful for storing security information. However, the protection is not reversible. Once protected, the protection cannot be undone.

CE#, OE#, and WE# signals control the bus operation of the memory. They enable simple connection to most microprocessors, often without additional logic.

V_{PP}/WP enables faster programming of the device, enabling multiple word/byte programming. If this signal is held at V_{SS}, the boot block and its adjacent parameter block are protected from PROGRAM and ERASE operations.

The device supports asynchronous random read and page read from all blocks of the memory array.

In order to meet environmental requirements, Micron offers the M29W640FT and the M29W640FB in RoHS packages (lead-free). The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC-Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

The memory is delivered with all the bits erased (set to 1).

Figure 1: Logic Diagram

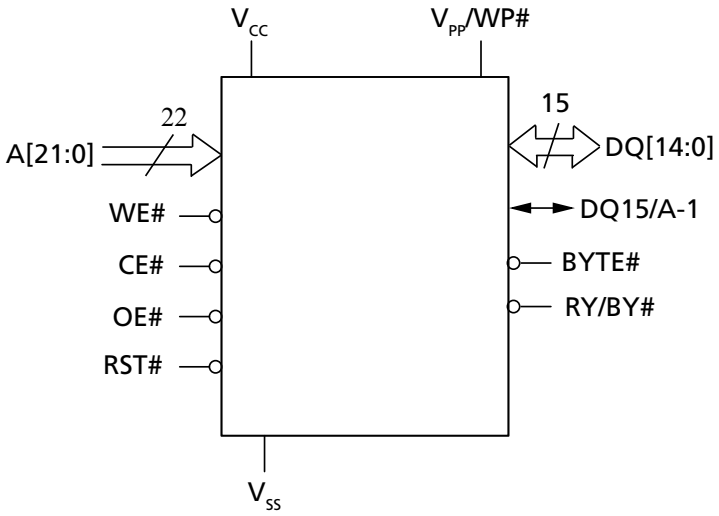
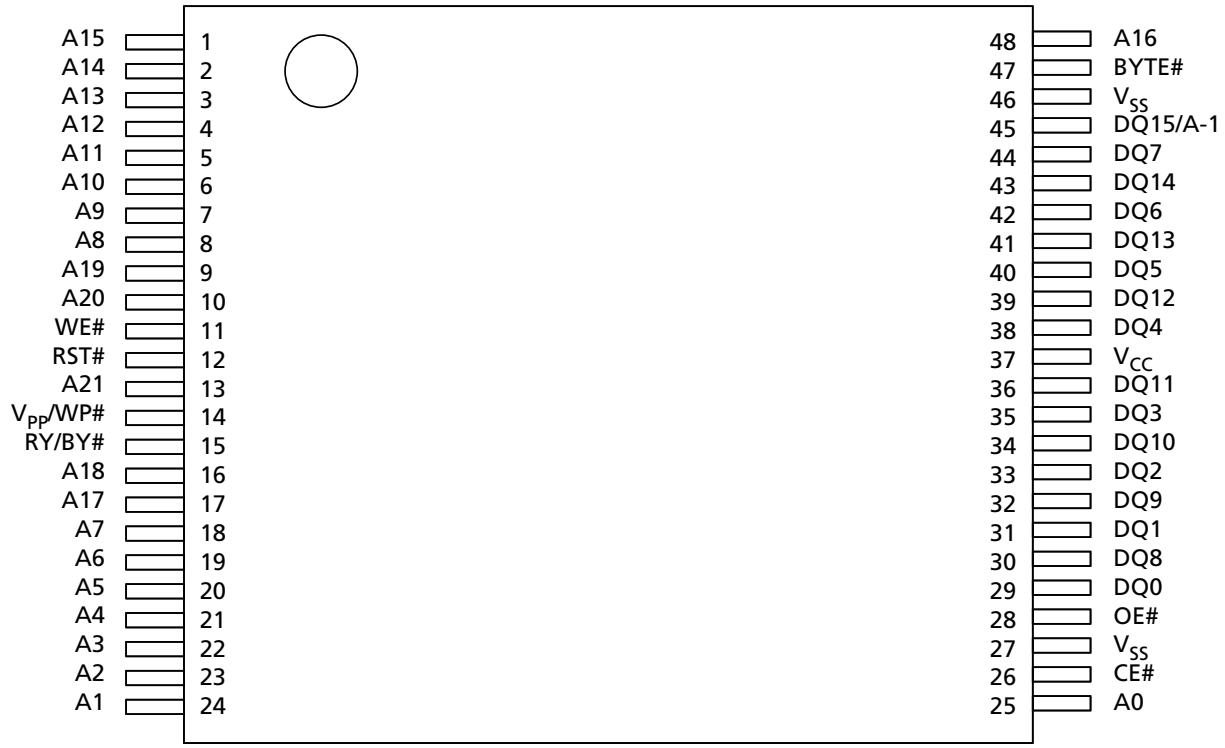


Table 2: Signal Names

Name	Type	Description
A[21:0]	Input	Address inputs
CE#	Input	Chip enable
OE#	Input	Output enable
WE#	Input	Write enable
RST#	Input	Reset/block temporary unprotect
RY/BY#	Input	Ready/busy
BYTE#	Input	Byte/word organization select
DQ[7:0]	I/O	Data input/outputs
DQ[14:8]	I/O	Data input/outputs
DQ15A-1 (or DQ15)	I/O	Data input/output or address input (or data I/O)
V_{CC}	Supply voltage	Supply voltage
V_{PP}/WP#	Supply voltage	Supply voltage for FAST PROGRAM (optional) or WRITE PROTECT operations
V_{SS}	–	Ground
NC	–	Not connected internally

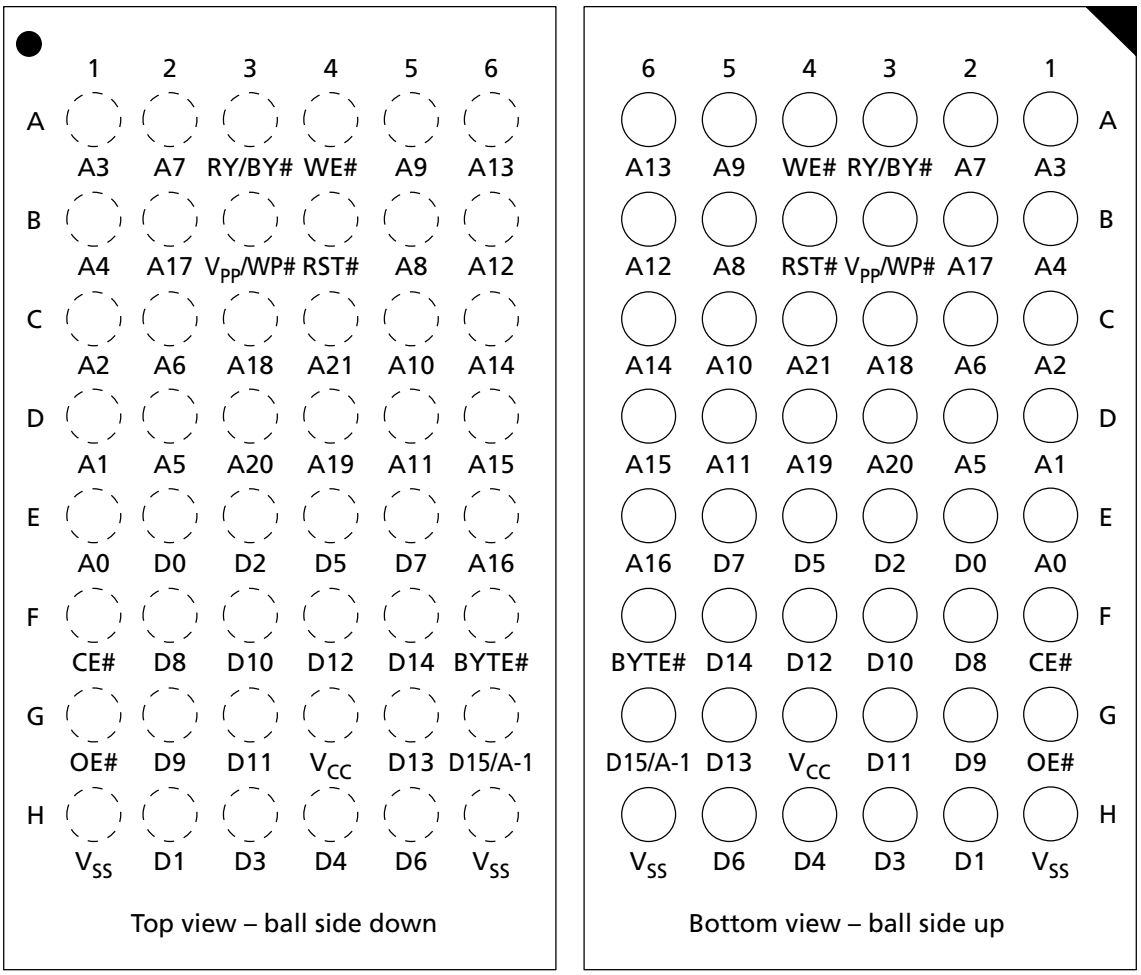
Signal Assignments

Figure 2: 48-Pin TSOP Pinout



Note: 1. RFU = reserved for future use.

Figure 3: 48-Ball TFBGA Ballout



Note: 1. RFU = reserved for future use.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 3: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Select the cells in the memory array to access during bus READ operations. During bus WRITE operations they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the memory, allowing bus READ and bus WRTE operations to be performed. When CE# is HIGH, all other pins are ignored.
OE#	Input	**Output enable:** Controls the bus READ operation of the memory.
WE#	Input	**Write enable:** Controls the bus write operation of the memory's command interface.
V_{PP}/WP#	Input	**V_{PP}/WP#:** Provides two functions: V_{PP} enables the memory to use an external high-voltage power supply to reduce the time required for UNLOCK BYPASS PROGRAM operations. WP# performs hardware protection by protection the last block at the end of the addressable area (M29W640GH) or the first block at the beginning of the addressable area (M29W640GL). It protects the last two blocks at the end of the addressable area (M29W640GT) and the first two boot blocks at the beginning of the addressable area (M29W640GB). V_{PP}/WP# may be left floating or unconnected (see DC Characteristics). When V_{PP}/WP# is LOW, the last or first block in the M29W640GH and M29W640GL, respectively, and the last or first two blocks in the M29W640GT and M29W640GB, respectively, are protected. PROGRAM and ERASE operations in this block are ignored while V_{PP}/WP# is LOW, even when RST# is at V_{ID}. When V_{PP}/WP# is HIGH, V_{IH}, the device reverts to the previous protection status of the outermost blocks. PROGRAM and ERASE operations can now modify the data in the outermost blocks unless the block is protected using block protection. Applying 12V to V_{PP}/WP# will temporarily unprotect any block previously protected (including the outermost blocks) using a high-voltage block protection technique (in-system or programmer technique). (See Hardware Protection for details. When V_{PP}/WP# is raised to V_{PP}, the device automatically enters the unlock bypass mode. When V_{PP}/WP# returns to V_{IH} or V_{IL}, normal operation resumes. During UNLOCK BYPASS PROGRAM operations, the device draws I_{PP} from the pin to supply the programming circuits. (See UNLOCK BYPASS Command.) The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than ^{t}VHVPP (See the Accelerated Program Timing waveforms). Never raise V_{PP}/WP# to V_{PP} from any mode except read mode; otherwise, the device may be left in an indeterminate state. A 0.1µF capacitor should be connected between V_{PP}/WP# and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during an UNLOCK BYPASS PROGRAM operation, I_{PP}.

Table 3: Signal Descriptions (Continued)

Name	Type	Description
RST#	Input	**Reset/Block temporary unprotect:** Applies a hardware reset to the memory or temporarily unprotect all blocks that have been protected. Note that if V_{PP}/WP is at V_{IL}, then the last and the first block in the M29W640GH and M29W640GL, respectively, and the last two and first two blocks in the M29W640GT and M29W640GB, respectively, will remain protected, even if RST# is at V_{ID}. A hardware reset is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the memory will be ready for bus READ and bus WRITE operations after ^{t}PHEL or ^{t}RHEL, whichever occurs last. (See Reset Characteristics for more details.) Holding RST# at V_{ID} will temporarily unprotect the protected blocks in the memory. PROGRAM and ERASE operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than ^{t}PHPHH.
DQ15/A-1	I/O	**Data I/O or address input:** When HIGH, behaves as a data I/o pin (as DQ8–DQ14). When LOW, behaves as an address pin; DQ15A–1 LOW will select the LSB of the addressed word; DQ15A–1 HIGH will select the MSB. Throughout the text, consider references to the data I/O to include this pin when BYTE# is HIGH and references to the address inputs to include this pin when BYTE# is LOW, except when stated explicitly otherwise.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a bus READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During bus WRITE operations, the command register does not use these bits. When reading the status register these bits should be ignored.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a bus READ operation. During bus WRITE operations, they represent the commands sent to the command interface of the program/erase controller.
RY/BY#	Output	**Ready busy:** Open-drain output that identifies when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, bus READ and WRITE operations cannot begin until RY/BY# becomes High-Z. (See Reset Characteristics for more details.) The use of an open-drain output enables RY/BY# pins from several devices to be connected to a single pull-up resistor. A LOW will then indicate that one, or more, of the devices is busy.
BYTE#	Input	**BYTE#/Word organization select:** Switches between the x8 and x16 bus modes of the device. When LOW, the device is in x8 mode; when HIGH, it is in x16 mode.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for all operations (READ, PROGRAM, and ERASE). The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the memory contents being altered will be invalid. A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations, I_{CC3}.

Table 3: Signal Descriptions (Continued)

Name	Type	Description
V_{SS}	Supply	**Ground:** Reference for all voltage measurements. The device features two V_{SS} pins which must be both connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Table 4: Hardware Protection

V_{PP}/WP#	RST#	Function
V_{IL}	V_{IH}	Two outermost parameter blocks protected from PROGRAM or ERASE operations
	V_{ID}	All blocks unprotected temporarily except the two outermost blocks
V_{IH} or V_{ID}	V_{ID}	All blocks unprotected temporarily
V_{PPH}	V_{IH} or V_{ID}	All blocks unprotected temporarily

Memory Organization

Memory Configuration

The main memory array is divided into 64KB blocks.

The blocks in the memory are asymmetrically arranged. The first or last 64KB of memory has been divided into eight 8KB parameter blocks.

x8 Memory Map – 64Mb Density

Table 5: x8 Top Boot – Blocks [134:0]

Block	Block Size	Address Range		Notes
		Start	End	
134	8KB	007F E000	007F FFFF	1
133	8KB	007F C000	007F DFFF	
132	8KB	007F A000	007F BFFF	
131	8KB	007F 8000	007F 9FFF	
130	8KB	007F 6000	007F 7FFF	
129	8KB	007F 4000	007F 5FFF	
128	8KB	007F 2000	007F 3FFF	
127	8KB	007F 0000	007F 1FFF	
126	64KB	007E 0000	007E FFFF	
⋮	⋮	⋮	⋮	
2	64KB	0002 0000	0002 FFFF	
1	64KB	0001 0000	0001 FFFF	
0	64KB	0000 0000	0000 FFFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

Table 6: x8 Bottom Boot – Blocks [134:0]

Block	Block Size	Address Range		Notes
		Start	End	
134	64KB	007F 0000	007F FFFF	
133	64KB	007E 0000	007E FFFF	
132	64KB	007D 0000	007D FFFF	
⋮	⋮	⋮	⋮	
8	64KB	0001 0000	0001 FFFF	

Table 6: x8 Bottom Boot – Blocks [134:0] (Continued)

Block	Block Size	Address Range		Notes
		Start	End	
7	8KB	0000 E000	0000 FFFF	1
6	8KB	0000 C000	0000 DFFF	
5	8KB	0000 A000	0000 BFFF	
4	8KB	0000 8000	0000 9FFF	
3	8KB	0000 6000	0000 7FFF	
2	8KB	0000 4000	0000 5FFF	
1	8KB	0000 2000	0000 3FFF	
0	8KB	0000 0000	0000 1FFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

x16 Memory Map – 64Mb Density

Table 7: x16 Top Boot – Blocks [134:0]

Block	Block Size	Address Range		Notes
		Start	End	
134	8KW	003F F000	003F FFFF	1
133	8KW	003F E000	003F EFFF	
132	8KW	003F D000	003F DFFF	
131	8KW	003F C000	003F CFFF	
130	8KW	003F B000	003F BFFF	
129	8KW	003F A000	003F AFFF	
128	8KW	003F 9000	003F 9FFF	
127	8KW	003F 8000	003F 8FFF	
126	32KW	003F 0000	003F 7FFF	
⋮	⋮	⋮	⋮	
2	32KW	0001 0000	0001 7FFF	
1	32KW	0000 8000	0000 FFFF	
0	32KW	0000 0000	0000 7FFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

Table 8: x16 Bottom Boot – Blocks [134:0]

Block	Block Size	Address Range		Notes
		Start	End	
134	32KW	003F 8000	003F FFFF	
133	32KW	003F 0000	003F 7FFF	
132	32KW	003E 8000	003E FFFF	
⋮	⋮	⋮	⋮	
8	32KW	0000 8000	000F FFFF	
7	8KW	0000 7000	0007 7FFF	1
6	8KW	0000 6000	0006 6FFF	
5	8KW	0000 5000	0005 5FFF	
4	8KW	0000 4000	0004 4FFF	
3	8KW	0000 3000	0003 3FFF	
2	8KW	0000 2000	0002 2FFF	
1	8KW	0000 1000	0001 1FFF	
0	8KW	0000 0000	0000 7FFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

Bus Operations

Table 9: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	8-Bit Mode			16-Bit Mode	
				A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	X	H	H	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE# and WE# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# = LOW, the highest/lowest block remains protected, depending on the line item.
4. Data input is required when issuing a command sequence or performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. A valid READ operation requires setting the appropriate address on the address inputs, taking CE# and OE# LOW and holding WE# HIGH. Data I/O signals output the value.

Write

Bus WRITE operations write to the command interface. A valid WRITE operation requires setting the appropriate address on the address inputs. These are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. Values on data I/O signals are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire operation.

Standby and Automatic Standby

When the device is in read mode, driving CE# HIGH places the device in standby mode and drives data I/Os to High-Z. Supply current is reduced to standby (I_{CC2}), by holding CE# within V_{CC} ±0.2V.

During PROGRAM or ERASE operations, the device continues to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic standby enables low power consumption during read mode. When CMOS levels (V_{CC} ± 0.2 V) drive the bus, and following a READ operation and a period of inactivity specified in DC Characteristics, the memory enters automatic standby as internal supply current is reduced to I_{CC2}. Data I/O signals still output data if a READ operation is in progress.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Status Register

Bus READ operations from any address always read the status register during PROGRAM and ERASE operations. It is also read during ERASE SUSPEND operations when an address within a block being erased is accessed. The bits in the status register are summarized in the Status Register Bits table.

Data Polling Bit (DQ7)

The data polling bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an ERASE SUSPEND operation. The data polling bit is output on DQ7 when the status register is read.

During PROGRAM operations, the data polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the PROGRAM operation, the memory returns to read mode, and bus READ operations from the address just programmed output DQ7, not its complement.

During ERASE operations, the data polling bit outputs 0, the complement of the erased state of DQ7. After successful completion of the ERASE operation, the memory returns to read mode.

In erase suspend mode, the data polling bit will output a 1 during a bus READ operation within a block being erased. The data polling bit will change from a 0 to a 1 when the program/erase controller has suspended the ERASE operation. The Data Polling Flowchart gives an example of how to use the data polling bit. A valid address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6)

The toggle bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an ERASE SUSPEND command. The toggle bit is output on DQ6 when the status register is read.

During PROGRAM and ERASE operations, the toggle bit changes from 0 to 1 to 0, etc., with successive bus READ operations at any address. After successful completion of the operation, the memory returns to read mode.

During erase suspend mode, the toggle bit will output when addressing a cell within a block being erased. The toggle bit will stop toggling when the program/erase controller has suspended the ERASE operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signaled, and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signaled, and DQ6 toggles for approximately 1µs. The Data Toggle Flowchart gives an example of how to use the data toggle bit.

Error Bit (DQ5)

The error bit can be used to identify errors detected by the program/erase controller. The error bit is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory. If the error bit is set, a READ/RESET command must be issued before other commands are issued. The error bit is output on DQ5 when the status register is read.

Note that the PROGRAM command cannot change a bit set to 0 back to 1, and attempting to do so will set DQ5 to 1. A bus READ operation to that address will show the bit is still 0. One of the ERASE commands must be used to set all the bits in a block or in the whole memory from 0 to 1.

Erase Timer Bit (DQ3)

The erase timer bit can be used to identify the start of program/erase controller operation during a BLOCK ERASE command. When the program/erase controller starts erasing, the erase timer bit is set to 1. Before the program/erase controller starts, the erase timer bit is set to 0, and additional blocks to be erased may be written to the command interface. The erase timer bit is output on DQ3 when the status register is read.

Alternative Toggle Bit (DQ2)

The alternative toggle bit can be used to monitor the program/erase controller during ERASE operations. It is output on DQ2 when the status register is read.

During CHIP ERASE and BLOCK ERASE operations, the toggle bit changes from 0 to 1 to 0, etc., with successive bus READ operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. After the operation completes, the memory returns to read mode.

During an ERASE SUSPEND operation, the alternative toggle bit changes from 0 to 1 to 0, etc., with successive bus READ operations from addresses within the blocks being erased. Bus READ operations to addresses within blocks not being erased will output the memory cell data as if in read mode.

After an ERASE operation that causes the error bit to be set, the alternative toggle bit can be used to identify which block or blocks have caused the error. The alternative toggle bit changes from 0 to 1 to 0, etc., with successive bus READ operations from addresses within blocks that have not erased correctly. The alternative toggle bit does not change if the addressed block has erased correctly.

Table 10: Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0
PROGRAM DURING ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	0
PROGRAM ERROR	Any address	DQ7#	Toggle	1	–	–	0
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	0
BLOCK ERASE BEFORE TIMEOUT	Erasing block	0	Toggle	0	0	Toggle	0
	Non-erasing block	0	Toggle	0	0	No Toggle	0
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	0
	Non-erasing block	0	Toggle	0	1	No Toggle	0
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	1
	Non-erasing block	Data read as normal					1

Table 10: Status Register Bits (Continued)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
ERASE ERROR	Good block address	0	Toggle	1	1	No Toggle	0
	Faulty block address	0	Toggle	1	1	Toggle	0

Note: 1. Unspecified data bits should be ignored.

Figure 4: Data Polling Flowchart

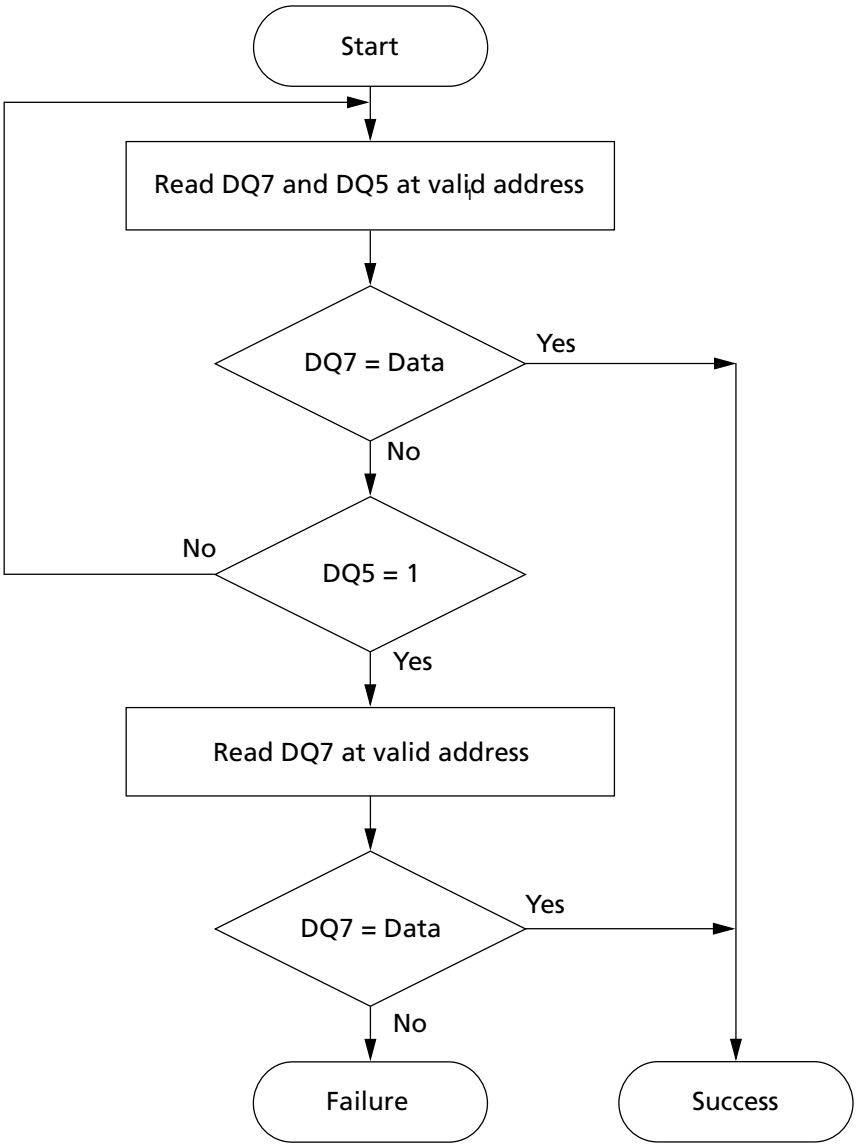
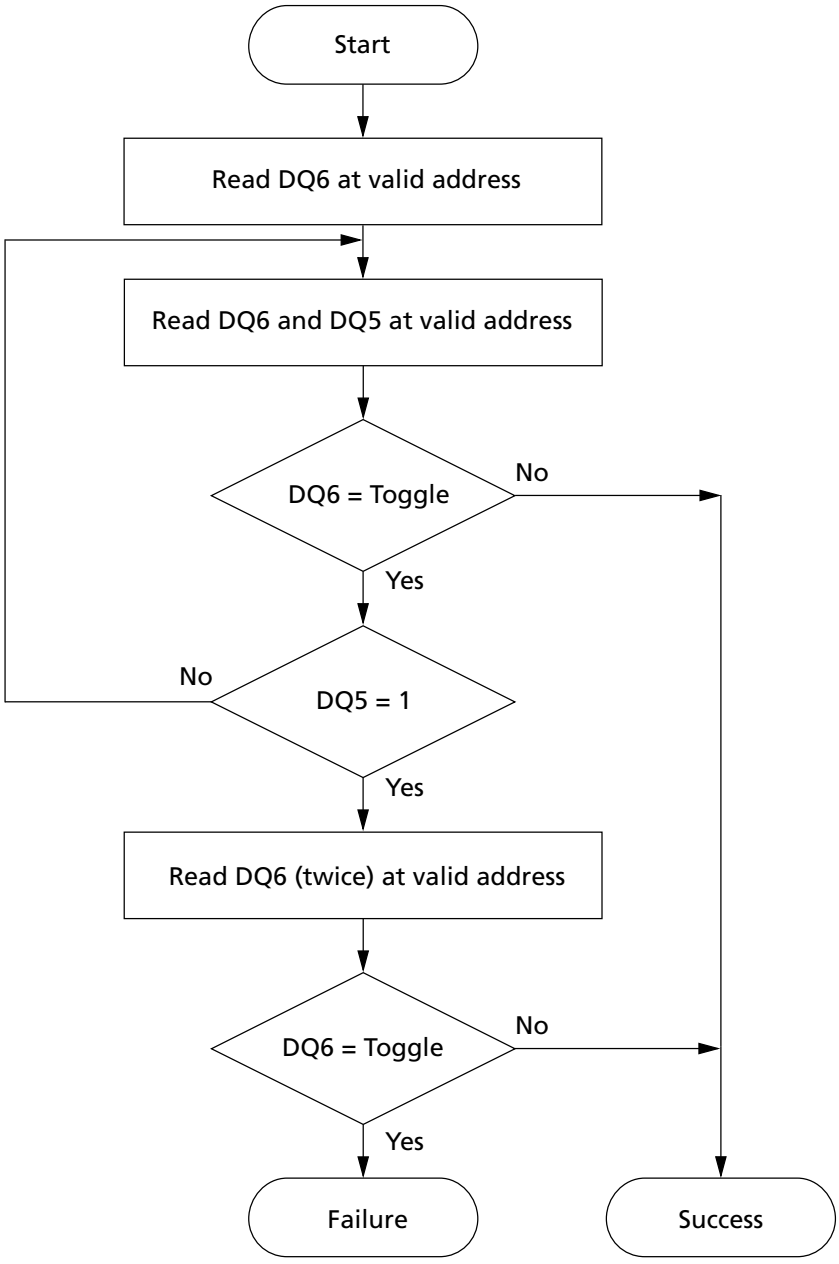


Figure 5: Data Toggle Flowchart



READ Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is valid only when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area. A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

AUTO SELECT Operations

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command or by applying V_{ID} to A9. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information.
- Block protection, which includes the block protection status and extended memory block protection indicator.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

To enter auto select mode by applying V_{ID} to A9 (see the following tables).

Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 11: Read Electronic Signature

Note 1 applies to entire table

Signal	READ Cycle						Notes
	Manufacturer Code	Device Code 1	Device Code 2		Device Code 3		
			GH/GL	GT/GB	GH/GT	GL/GB	
CE#	L	L	L	L	L	L	
OE#	L	L	L	L	L	L	
WE#	H	H	H	H	H	H	
Address Input, 8-Bit and 16-Bit							
A[MAX:10]	X	X	X	X	X	X	
A9	V_{ID}	V_{ID}	V_{ID}	V_{ID}	V_{ID}	V_{ID}	2
A8	X	X		X		X	
A[7:5]	L	L		L		L	
A4	X	X		X		X	
A[3:1]	L	L		H		H	
A0	L	H		L		H	
Address Input, 8-Bit Only							

Table 11: Read Electronic Signature (Continued)

Note 1 applies to entire table

Signal	READ Cycle						Notes
	Manufacturer Code	Device Code 1	Device Code 2		Device Code 3		
			GH/GL	GT/GB	GH/GT	GL/GB	
DQ[15]/A-1	X	X		X		X	
Data I/O, 8-Bit Only							
DQ[14:8]	X	X		X		X	
DQ[7:0]	20h	7Eh	0Ch	10h	01h	00h	
Data I/O, 16-Bit Only							
DQ[15]/A-1, and DQ[14:0]	0020h	227Eh	220Ch	2210h	2201h	2200h	

Notes: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. When using the AUTO SELECT command to enter auto select mode, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 12: Block Protection

Note 1 applies to entire table

Operation	CE#	OE#	WE#	Address Input										Data I/O
				A[MAX]	A15	A[14:13]	A12	A[11:10], A[8:7], A[5:4]	A9	A6	A[3:2]	A1	A0	DQ15/A-1, DQ[14:0]
BLOCK PROTECT (Group)	L	V_{ID}	LP	Block address				X	V_{ID}	X				X
CHIP UNPROTECT	V_{ID}	V_{ID}	LP	X	H	X	H	X	V_{ID}	X				X
VERIFY BLOCK PROTECTION	L	L	H	Block address				X	V_{ID}	L	L	H	L	Pass = xx01h Retry= xx00h
VERIFY BLOCK UNPROTECT	L	L	H	Block address				X	V_{ID}	H	L	H	L	Retry = xx01h Pass= xx00h

Note: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); LP = L pulse; X = HIGH or LOW.

Command Interface

All bus WRITE operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus WRITE operations. Failure to observe a valid sequence of bus WRITE operations will result in the memory returning to read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes, depending on whether the memory is in 16-bit or 8-bit mode. See the x8 and x16 command tables, depending on the configuration that is being used, for a summary of the commands.

READ/RESET Command

The READ/RESET command returns the memory to read mode. It also resets the errors in the status register. Either one or three bus WRITE operations can be used to issue the READ/RESET command.

The READ/RESET command can be issued, between bus WRITE cycles before the start of a PROGRAM or ERASE operation, to return the device to read mode. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, then the device will take up to 10µs to abort. During the abort period, no valid data can be read from the device. The READ/RESET command will not abort an ERASE operation when issued while in erase suspend.

AUTO SELECT Command

The AUTO SELECT command is used to read the manufacturer code, the device code, the block protection status, and the extended memory block verify code. Three consecutive bus WRITE operations are required to issue the AUTO SELECT command. After the AUTO SELECT command is issued, the memory remains in auto select mode until a READ/RESET command is issued. READ CFI QUERY and READ/RESET commands are accepted in auto select mode; all other commands are ignored.

In auto select mode, the manufacturer code and the device code can be read by using a bus READ operation with addresses and control signals set, as shown Bus Operations, except for A9 (which is "Don't Care").

The block protection status of each block can be read using a bus READ operation with addresses and control signals set, as shown in Bus Operations, except for A9 (which is "Don't Care"). If the addressed block is protected, then 01h is output on DQ0–DQ7; otherwise, 00h is output (in 8-bit mode).

The protection status of the extended memory block, or extended memory block verify code, can be read using a bus READ operation with addresses and control signals, except for A9 (which is "Don't Care"). If the extended block is "factory-locked." then 80h is output on DQ0–DQ7; otherwise, 00h is output (8-bit mode).

READ CFI QUERY Command

The READ CFI QUERY command is used to read data from the CFI. This command is valid when the device is in the read array mode, or when the device is in auto select mode.

One bus WRITE cycle is required to issue the READ CFI QUERY command. After the command is issued, subsequent bus READ operations read from the CFI.