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Parallel NOR Flash Embedded Memory

M29W640GH, M29W640GL
M29W640GT, M29W640GB

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{PP} = 12V for fast program (optional)
- Asynchronous random/page read
  - Page width: 4 words
  - Page access: 25ns
  - Random access: 60ns, 70ns, 90ns
- Fast program commands
  - 2-word/4-byte program (without V_{PP} = 12V)
  - 4-word/8-byte program (with V_{PP} = 12V)
  - 16-word/32-byte write buffer
- Programming time
  - 10µs per byte/word TYP
  - Chip program time: 10 s (4-word program)
  - Double word/quadruple byte program
- Memory organization
  - M29W640GH/L 128 main blocks, 64KB each
  - M29W640GT/B 127 main blocks, 64KB each and 8 boot blocks, 8KB each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Hardware block protection
  - V_{PP}/WP# pin for fast program and write protect
  - Temporary block unprotect mode
- Common Flash interface
  - 64-bit security code
- 128-word extended memory block
  - Extra block used as security block or to store additional information
- Low power consumption: Standby and automatic mode
- 100,000 PROGRAM/ERASE cycles per block
- Electronic signature
  - Manufacturer code: 0020h
- Device summary: part number and device code
  - M29W640GH: uniform, last block protected by V_{PP}/WP#
  - 227Eh + 220Ch + 2201h
  - M29W640GL: uniform, first block protected by V_{PP}/WP#
  - 227Eh + 220Ch + 2200h
  - M29W640GT: top boot block
  - 227Eh + 2210h + 2201h
  - M29W640GB: bottom boot block
  - 227Eh + 2210h + 2200h
- RoHS-compliant packages
  - 48-pin TSOP (N/NA) 12mm x 20mm
  - 56-pin TSOP (NB) 14mm x 20mm
  - 48-ball TFBGA (ZA) 6mm x 8mm
  - 64-ball FBGA (ZS) 11mm x 13mm
  - 64-ball TBGA (ZF) 10mm x 13mm
- Automotive certified parts available

Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or speed, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details
Device Type	M29 = Parallel Flash memory
Operating Voltage	W = 2.7 to 3.6V
Device Function	640G = 64Mb (x8/x16) boot block, uniform or boot block
Array Matrix	T = Top boot
	B = Bottom boot
	L = First block protected by V_{PP}/WP#
	H = Last block protected by V_{PP}/WP#
Speed	60 = 60ns (in conjunction with temperature range 6; denotes industrial grade –40°C to 85°C parts)
	6A = 60ns (in conjunction with temperature range 6; denotes automotive grade –40°C to 85°C parts)
	7A = 70ns (in conjunction with temperature range 6; denotes automotive grade –40°C to 85°C parts)
	70 = 70ns (in conjunction with temperature range 6; denotes industrial grade –40°C to 85°C parts; temperature range = 3 denotes automotive grade –40°C to 125°C parts)
	90 = 90ns (in conjunction with temperature range 6; denotes industrial grade –40°C to 85°C parts)
Package	N/NA = 48-pin TSOP, 12mm x 20mm
	NB = 56-pin TSOP, 14mm x 20mm (available upon request)
	ZA = 48-ball TFBGA, 6mm x 8mm, 0.8mm pitch
	ZS = 64-ball FBGA, 11mm x 13mm, 1mm pitch
	ZF = 64-ball TBGA, 10mm x 13mm, 1mm pitch (available upon request)
Temperature Range	6 = –40°C to 85°C
	3 = –40°C to 125°C (Automotive)
Shipping Options	E = RoHS-compliant package, standard packing
	F = RoHS-compliant package, tape and reel packing

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General Description

The M29W640G is a 64Mb (8Mb x8 or 4Mb x16) nonvolatile memory that can be read, erased, and reprogrammed. These operations can be performed using a single low voltage (2.7–3.6V) supply. Upon power-up, the device defaults to read mode.

The memory is divided into blocks that can be erased independently so that valid data can be preserved while old data is erased. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

The M29W640GH and M29W640GL memory array is organized into 128 uniform blocks of 64KB each (or 32Kwords each).

The M29W640GT and M29W640GB feature an asymmetric memory block, each having an array of 135 blocks divided into 8 parameter blocks of 8KB each (or 4 Kwords each), and 127 main blocks of 64KB each (or 32Kwords each). The M29W640GT has the parameter blocks at the top of the memory array whereas the M29W640GB locates the parameter blocks starting from the bottom.

Blocks are protected by groups to prevent accidental PROGRAM or ERASE commands from modifying the memory.

The M29W640G supports asynchronous random read and page read from all blocks of the array. Chip enable, output enable, and write enable signals control the bus operation. They enable simple connection to most microprocessors, often without additional logic.

The V_{PP}/WP# signal is used to enable faster programming of the device. Protection from PROGRAM/ERASE commands can be obtained by holding V_{PP}/WP# to V_{SS}:

- On the M29W640GH and M29W640GL, the last and first blocks are protected.
- On the M29W640GT and M29W640GB, the last two and first two boot blocks are protected.

The M29W640G devices feature a full set of fast program commands to improve programming throughput:

- 2-byte PROGRAM (it is not necessary to raise V_{PP}/WP# to 12V before issuing this command)
- 2 words/4-byte PROGRAM (it is not necessary to raise V_{PP}/WP# to 12V before issuing this command)
- 4 word/8-byte PROGRAM (V_{PP}/WP# must be raised to 12V before issuing this command)
- WRITE TO BUFFER and PROGRAM (enables program in one shot a buffer of 16 words/32 bytes)

The M29W640G has an extra block, the extended block, of 128 words in x16 mode or 256 bytes in x8 mode that can be accessed using a dedicated command. The extended block can be protected, and therefore, is useful for storing security information. However, protection is not reversible; once protected, the protection cannot be undone.

The memory is delivered with all bits erased (set to 1).

Figure 1: Logic Diagram

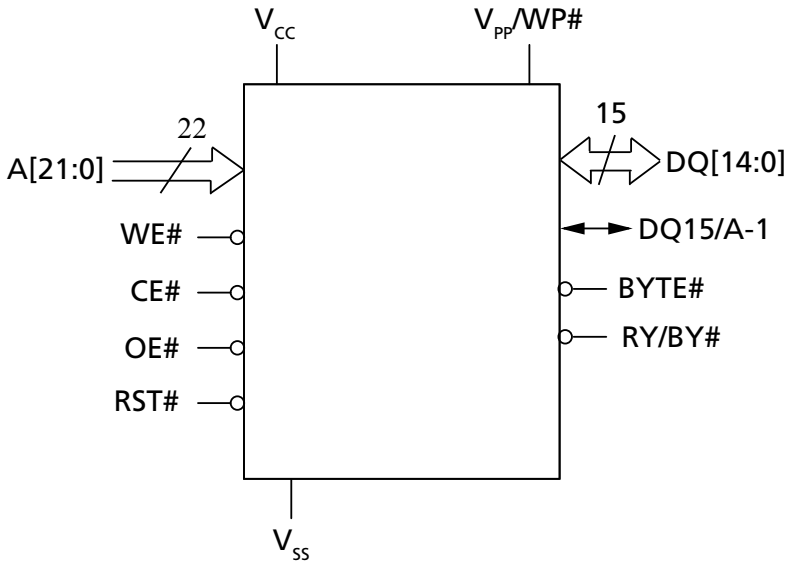


Table 2: Signal Names

Name	Description	Direction
A0-A21	Address inputs	Inputs
CE#	Chip enable	Input
OE#	Output enable	Input
WE#	Write enable	Input
RP#	Reset/Block temporary unprotect	Input
RY/BY#	Ready/Busy	Input
BYTE#	Byte/Word organization select	Input
DQ0–DQ7	Data input/outputs	I/O
DQ8–DQ14	Data input/outputs	I/O
DQ15A-1 (or DQ15)	Data input/output or address input (or data I/O)	I/O
V_{CC}	Supply voltage	Supply voltage
V_{PP}/WP#	Supply voltage for FAST PROGRAM (optional) or WRITE PROTECT command	Supply voltage
V_{SS}	Ground	–
NC	Not connected internally	–

Note: 1. V_{PP}/WP# may be left floating because it is internally connected to a pull-up resistor to enable PROGRAM/ERASE commands.

Table 3: Protection Granularity on the M29W640GH and M29W640GL

Block	KB/Kwords	Protection Block Group	(x8)	(x16)
0 to 3	4 x 64/32	Block level	000000h-03FFFFh[1]	000000h-01FFFFh[1]
4 to 7	4 x 64/32	Protection group	040000h-07FFFFh	020000h-03FFFFh
–	–	–	–	–
120 to 123	4 x 64/32	Protection group	780000h-7BFFFFh	3C0000h-3DFFFFh
124 to 127	4 x 64/32	Block level	7C0000h-7FFFFFh	3E0000h-3FFFFFh

Note: 1. Used as the extended block addresses in extended block mode.

Table 4: Protection Granularity on the M29W640GT

Block	KB/Kwords	Protection Block Group	(x8)	(x16)
0 to 3	4 x 64/32	Protection group	000000h-03FFFFh[1]	000000h-01FFFFh[1]
4 to 7	4 x 64/32	Protection group	040000h-07FFFFh	020000h-03FFFFh
–	–	–	–	–
120 to 123	4 x 64/32	Protection group	780000h-7BFFFFh	3C0000h-3DFFFFh
124 to 126	3 x 64/32	Protection group	7C0000h-7EFFFFh	3E0000h-3F7FFFh
127 to 134	8 x 8/4[2]	Block level	7F0000h-7FFFFFh	3F8000h-3FFFFFh

Notes: 1. Used as the extended block addresses in extended block mode.
2. Boot blocks.

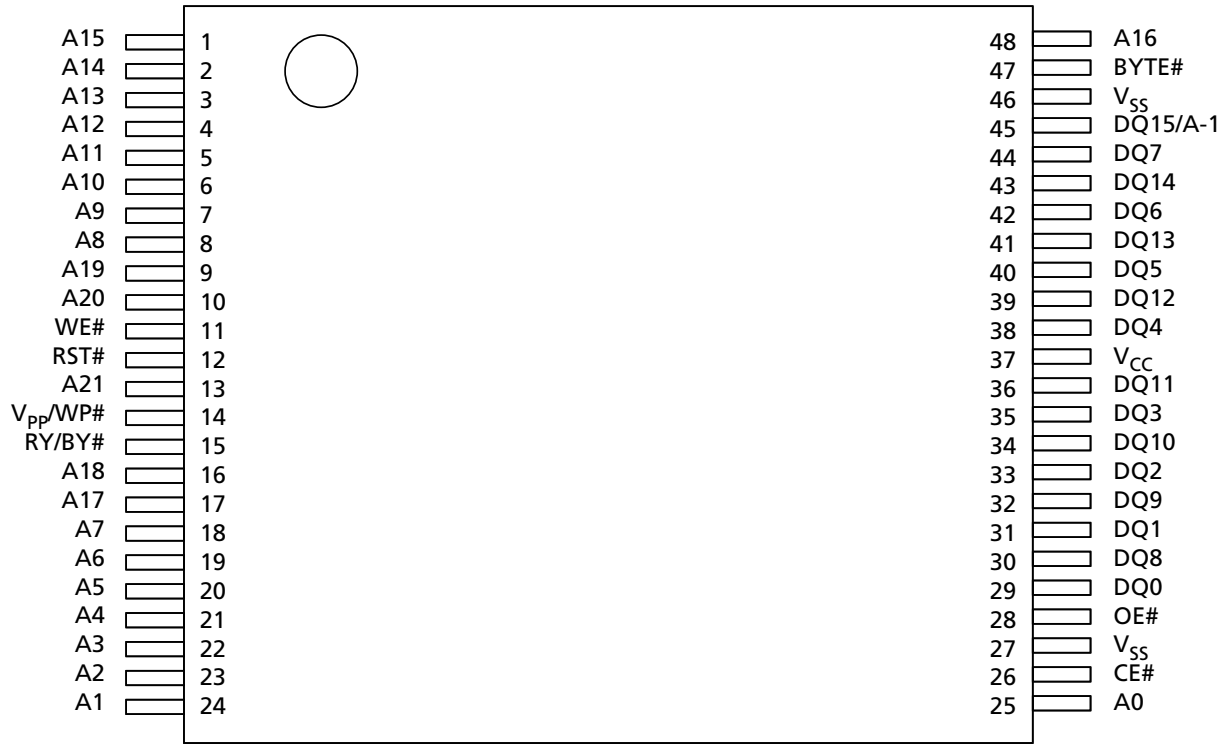
Table 5: Protection Granularity on the M29W640GB

Block	KB/Kwords	Protection Block Group	(x8)	(x16)
0 to 7	8x 8/4[1]	Block level	000000h-00FFFFh[2]	000000h-007FFFh[2]
8 to 10	3 x 64/32	Protection group	010000h-03FFFFh	008000h-01FFFFh
11 to 14	4 x 64/32	Protection group	040000h-07FFFFh	020000h-03FFFFh
–	–	–	–	–
127 to 130	4 x 64/32	Protection group	780000h-7BFFFFh	3C0000h-3DFFFFh
131 to 134	4 x 64/32	Protection group	7C0000h-7FFFFFh	3E0000h-3FFFFFh

Notes: 1. Boot blocks.
2. Used as the extended block addresses in extended block mode.

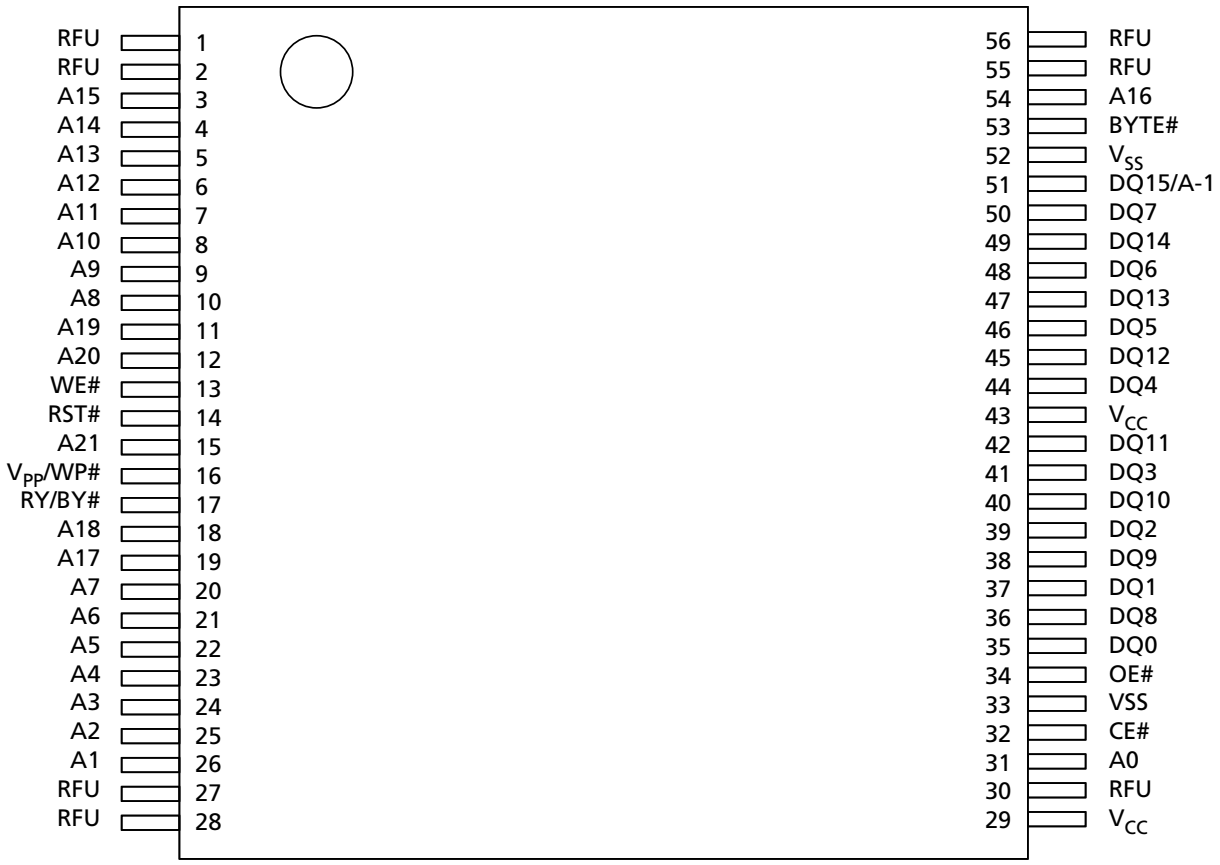
Signal Assignments

Figure 2: 48-Pin TSOP



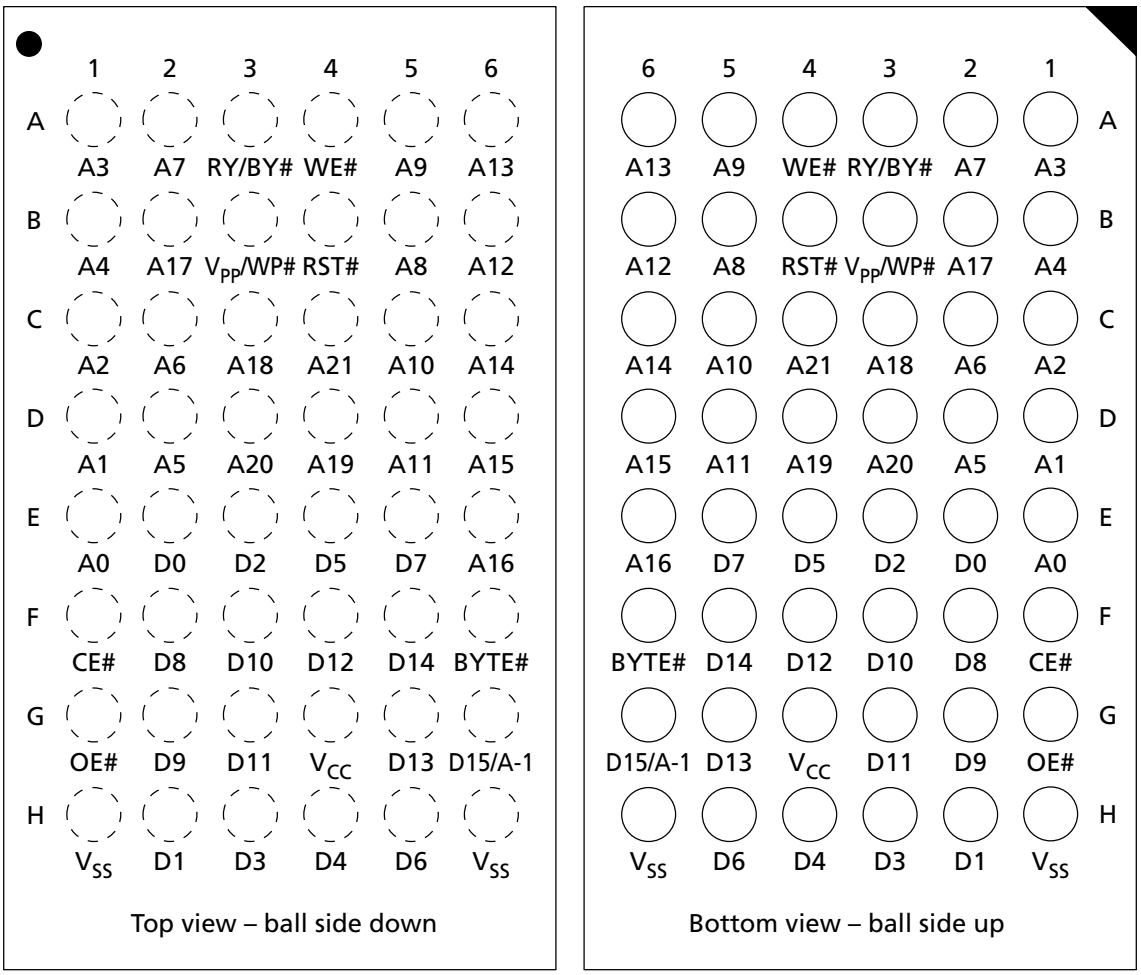
Note: 1. RFU = reserved for future use.

Figure 3: 56-Pin TSOP



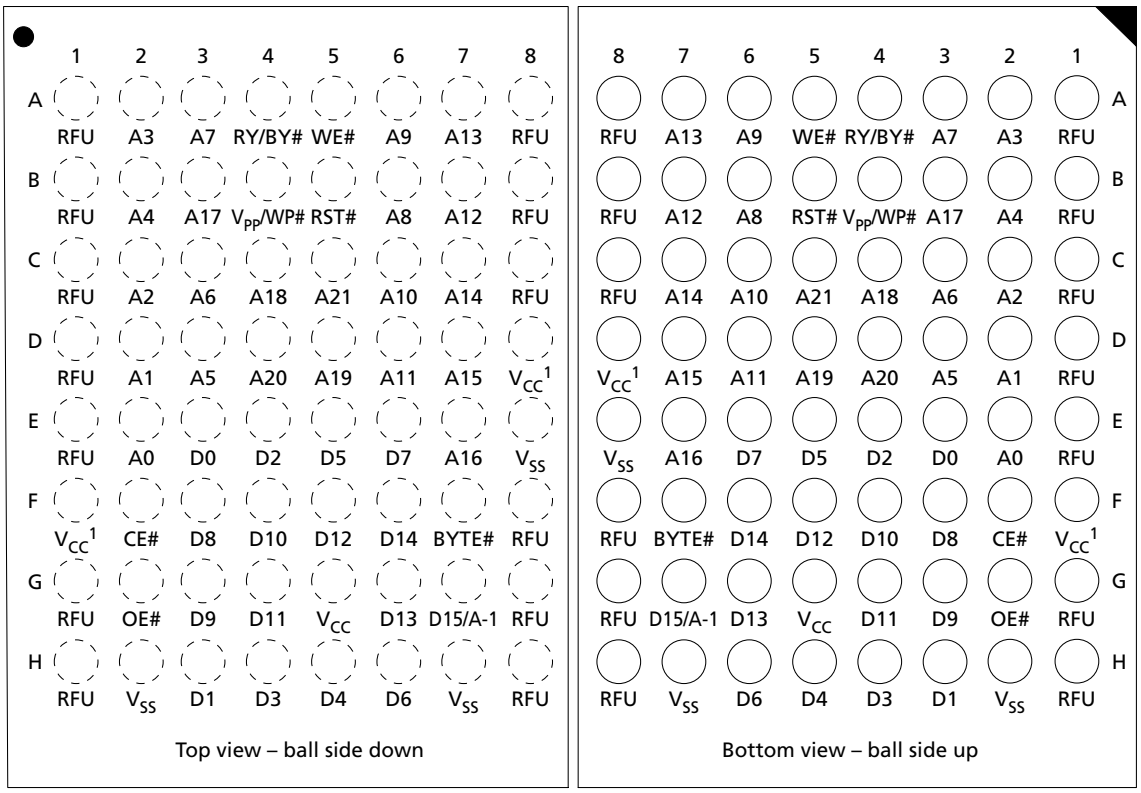
Note: 1. RFU = reserved for future use.

Figure 4: 48-Ball TFBGA



Note: 1. RFU = reserved for future use.

Figure 5: 64-Ball TFBGA



Notes: 1. RFU = reserved for future use.
2. Pads D8 and F1 are connected on the M29W640GT and M29W640GB devices.

Signal Descriptions

The following table is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 6: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Select the cells in the memory array to access during bus READ operations. During bus WRITE operations they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the memory, allowing bus READ and bus WRTE operations to be performed. When CE# is HIGH, all other pins are ignored.
OE#	Input	**Output enable:** Controls the bus READ operation of the memory.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the memory's command interface.
V_{PP}/WP#	Input	**V_{PP}/WP#:** Provides two functions: V_{PP} enables the memory to use an external high-voltage power supply to reduce the time required for UNLOCK BYPASS PROGRAM operations. WP# performs hardware protection by protection the last block at the end of the addressable area (M29W640GH) or the first block at the beginning of the addressable area (M29W640GL). It protects the last two blocks at the end of the addressable area (M29W640GT) and the first two boot blocks at the beginning of the addressable area (M29W640GB). V_{PP}/WP# may be left floating or unconnected (see DC Characteristics). When V_{PP}/WP# is LOW, the last or first block in the M29W640GH and M29W640GL, respectively, and the last or first two blocks in the M29W640GT and M29W640GB, respectively, are protected. PROGRAM and ERASE operations in this block are ignored while V_{PP}/WP# is LOW, even when RST# is at V_{ID}. When V_{PP}/WP# is HIGH, V_{IH}, the device reverts to the previous protection status of the outermost blocks. PROGRAM and ERASE operations can now modify the data in the outermost blocks unless the block is protected using block protection. Applying 12V to V_{PP}/WP# will temporarily unprotect any block previously protected (including the outermost blocks) using a high-voltage block protection technique (in-system or programmer technique). (See Hardware Protection for details. When V_{PP}/WP# is raised to V_{PP}, the device automatically enters the unlock bypass mode. When V_{PP}/WP# returns to V_{IH} or V_{IL}, normal operation resumes. During UNLOCK BYPASS PROGRAM operations, the device draws I_{PP} from the pin to supply the programming circuits. (See UNLOCK BYPASS Command.) The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than ^{t}VHVPP (See the Accelerated Program Timing waveforms). Never raise V_{PP}/WP# to V_{PP} from any mode except read mode; otherwise, the device may be left in an indeterminate state. A 0.1µF capacitor should be connected between V_{PP}/WP# and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during an UNLOCK BYPASS PROGRAM operation, I_{PP}.

Table 6: Signal Descriptions (Continued)

Name	Type	Description
DQ15/A-1	I/O	**Data I/O or address input:** When HIGH, behaves as a data I/O pin (as DQ8–DQ14). When LOW, behaves as an address pin; DQ15A–1 LOW will select the LSB of the addressed word; DQ15A–1 HIGH will select the MSB. Throughout the text, consider references to the data I/O to include this pin when BYTE# is HIGH and references to the address inputs to include this pin when BYTE# is LOW, except when stated explicitly otherwise.
RST#	Input	**Reset/Block temporary unprotect:** Applies a hardware reset to the memory or temporarily unprotect all blocks that have been protected. Note that if V_{PP}/WP is at V_{IL}, then the last and the first block in the M29W640GH and M29W640GL, respectively, and the last two and first two blocks in the M29W640GT and M29W640GB, respectively, will remain protected, even if RST# is at V_{ID}. A hardware reset is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the memory will be ready for bus READ and bus WRITE operations after ^{t}PHEL or ^{t}RHEL, whichever occurs last. (See Reset Characteristics for more details.) Holding RST# at V_{ID} will temporarily unprotect the protected blocks in the memory. PROGRAM and ERASE operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than ^{t}PHPHH.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a bus READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During bus WRITE operations, the command register does not use these bits. When reading the status register these bits should be ignored.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a bus READ operation. During bus WRITE operations, they represent the commands sent to the command interface of the program/erase controller.
RY/BY#	Output	**Ready busy:** Open-drain output that identifies when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, bus READ and WRITE operations cannot begin until RY/BY# becomes High-Z. (See Reset Characteristics for more details.) The use of an open-drain output enables RY/BY# pins from several devices to be connected to a single pull-up resistor. A LOW will then indicate that one, or more, of the devices is busy.
BYTE#	Input	**BYTE#/Word organization select:** Switches between the x8 and x16 bus modes of the device. When LOW, the device is in x8 mode; when HIGH, it is in x16 mode.

Table 6: Signal Descriptions (Continued)

Name	Type	Description
V_{CC}	Supply	**Supply voltage:** Provides the power supply for all operations (READ, PROGRAM, and ERASE). The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the memory contents being altered will be invalid. A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations, I_{CC3}.
V_{SS}	Supply	**Ground:** Reference for all voltage measurements. The device features two V_{SS} pins which must be both connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Table 7: Hardware Protection

V_{PP}/WP#	RST#		Function
V_{IL}	V_{IH}	M29W640GT and M29W640GB	Last 2 blocks at the end of the addressable area (M29W640GT) and first 2 blocks at the beginning of the addressable area (M29W640GB) protected from program/erase operations
		M29W640GH and M29W640GL	Last block at the end of the addressable area (M29W640GH) and first block at the beginning of the addressable area (M29W640GL) protected from program/erase operations
	V_{ID}	M29W640GT and M29W640GB	All blocks temporarily unprotected except the last 2 blocks at the end of the addressable area (M29W640GT) and first 2 blocks at the beginning of the addressable area (M29W640GB)
		M29W640GH and M29W640GL	All blocks temporarily unprotected except the last block at the end of the addressable area (M29W640GH) and first block at the beginning of the addressable area (M29W640GL)
V_{IH} or V_{ID}	V_{ID}		All blocks temporarily unprotected
V_{PP}	V_{IH} or V_{ID}		All blocks temporarily unprotected

Memory Organization

Memory Configuration

The memory array for M29W640GH and M29W640GL devices is organized into 128 uniform blocks of 64KB each for x8 and 32KW each for x16.

Uniform Block Memory Map, x16 – 64Mb Density

Table 8: x16 Uniform Blocks [127:0]

Block	Block Size	Address Range		Notes
		Start	End	
127	32KW	003F 8000	003F FFFF	
126	32KW	003F 0000	003F 7FFF	
125	32KW	003E 8000	003E FFFF	
124	32KW	003E 0000	003E 7FFF	
⋮	⋮	⋮	⋮	
3	32KW	0001 8000	0001 FFFF	1
2	32KW	0001 0000	0001 7FFF	
1	32KW	0000 8000	0000 FFFF	
0	32KW	0000 0000	0000 7FFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

Uniform Block Memory Map, x8 – 64Mb Density

Table 9: x8 Uniform Blocks [127:0]

Block	Block Size	Address Range		Notes
		Start	End	
127	64KB	007F 0000	007F FFFF	
126	64KB	007E 0000	007E FFFF	
125	64KB	007D 0000	007D FFFF	
124	64KB	007C 0000	007C FFFF	
⋮	⋮	⋮	⋮	
3	64KB	0003 0000	0003 FFFF	1
2	64KB	0002 0000	0002 FFFF	
1	64KB	0001 0000	0001 FFFF	
0	64KB	0000 0000	0000 FFFF	

Note: 1. Used as the extended block addresses when the device is in extended block mode.

Bus Operations

Table 10: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	8-Bit Mode			16-Bit Mode	
				A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	X	H	H	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE# and WE# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# = LOW, the highest/lowest block remains protected, depending on the line item.
4. Data input is required when issuing a command sequence or performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. A valid READ operation requires setting the appropriate address on the address inputs, taking CE# and OE# LOW and holding WE# HIGH. Data I/O signals output the value.

Write

Bus WRITE operations write to the command interface. A valid WRITE operation requires setting the appropriate address on the address inputs. These are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. Values on data I/O signals are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire operation.

Standby and Automatic Standby

When the device is in read mode, driving CE# HIGH places the device in standby mode and drives data I/Os to High-Z. Supply current is reduced to standby (I_{CC2}), by holding CE# within V_{CC} ±0.2V.

During PROGRAM or ERASE operations, the device continues to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic standby enables low power consumption during read mode. When CMOS levels (V_{CC} ± 0.2 V) drive the bus, and following a READ operation and a period of inactivity specified in DC Characteristics, the memory enters automatic standby as internal supply current is reduced to I_{CC2}. Data I/O signals still output data if a READ operation is in progress.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Status Register

Bus READ operations from any address, always read the status register during PROGRAM and ERASE operations. It is also read during erase suspend when an address within a block being erased is accessed.

Data Polling Bit (DQ7)

The data polling bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The data polling bit is output on DQ7 when the status register is read.

During PROGRAM operations, DQ7 outputs the complement of the bit being programmed to DQ7. After successful completion of the PROGRAM operation, the memory returns to read mode and bus READ operations from the address just programmed output DQ7, not its complement.

During ERASE operations DQ7 outputs 0, the complement of the erased state of DQ7. After successful completion of the ERASE operation the memory returns to read mode.

In erase suspend mode, DQ7 will output a 1 during a bus READ operation within a block being erased. DQ7 will change from a 0 to a 1 when the program/erase controller has suspended the ERASE operation. The Data Polling Flowchart gives an example of how to use DQ7. A valid address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6)

The toggle bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The toggle bit is output on DQ6 when the status register is read.

During PROGRAM and ERASE operations, DQ6 changes from 0 to 1 to 0, and so forth, with successive bus READ operations at any address. After successful completion of the operation, the memory returns to read mode.

During erase suspend mode, DQ6 will output when addressing a cell within a block being erased. DQ6 will stop toggling when the program/erase controller has suspended the ERASE operation.

The Data Toggle Flowchart gives an example of how to use DQ6 and the toggle and alternative toggle waveforms describe toggle bit timing.

Error Bit (DQ5)

The error bit can be used to identify errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory. If DQ5 is set, a READ/RESET command must be issued before other commands are issued. The error bit is output on DQ5 when the status register is read.

Note that the PROGRAM command cannot change a bit set to 0 back to 1 and attempting to do so will set DQ5 to 1. A bus READ operation to that address will show the bit remains 0. One of the ERASE commands must be used to set all the bits in a block or in the whole memory from 0 to 1.

Erase Timer Bit (DQ3)

The erase timer bit can be used to identify the start of program/erase controller operation during a BLOCK ERASE command. After the program/erase controller starts erasing, DQ3 is set to 1. Before the program/erase controller starts, DQ3 is set to 0 and additional blocks to be erased may be written to the command interface. The erase timer bit is output on DQ3 when the status register is read.

Alternative Toggle Bit (DQ2)

The alternative toggle bit can be used to monitor the program/erase controller during ERASE operations. It is output on DQ2 when the status register is read.

During CHIP ERASE and BLOCK ERASE operations, DQ2 changes from 0 to 1 to 0, and so forth, with successive bus READ operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. After the operation completes, the memory returns to read mode.

During erase suspend, DQ2 changes from 0 to 1 to 0, and so forth, with successive bus READ operations from addresses within the blocks being erased. Bus READ operations to addresses within blocks not being erased will output the memory cell data as if in read mode.

After an ERASE operation that causes DQ5 to be set, DQ2 can be used to identify which block or blocks have caused the error. DQ2 changes from 0 to 1 to 0, and so forth, with successive bus READ operations from addresses within blocks that have not erased correctly. DQ2 does not change if the addressed block has erased correctly.

Write to Buffer and Program Abort Bit (DQ1)

DQ1 is set to 1 when a WRITE TO BUFFER AND PROGRAM operation aborts. Otherwise, DQ1 is set to 0. The WRITE TO BUFFER AND PROGRAM ABORT AND RESET command must be issued to return the device to read mode (see Command Interface for more information).

Table 11: Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0
PROGRAM DURING ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	–	0
WRITE TO BUFFER AND PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	0
WRITE TO BUFFER AND PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0
PROGRAM ERROR	Any address	DQ7#	Toggle	1	–	–	–	High-Z
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0
BLOCK ERASE BEFORE TIMEOUT	Erasing block	0	Toggle	0	0	Toggle	–	0
	Non-erasing block	0	Toggle	0	0	No Toggle	–	0

Table 11: Status Register Bits (Continued)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0
	Non-erasing block	0	Toggle	0	1	No Toggle	–	0
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	–	High-Z
	Non-erasing block	Data read as normal					–	High-Z
ERASE ERROR	Good block address	0	Toggle	1	1	No Toggle	–	High-Z
	Faulty block address	0	Toggle	1	1	Toggle	–	High-Z

Note: 1. Unspecified data bits should be ignored.

Figure 6: Data Polling Flowchart

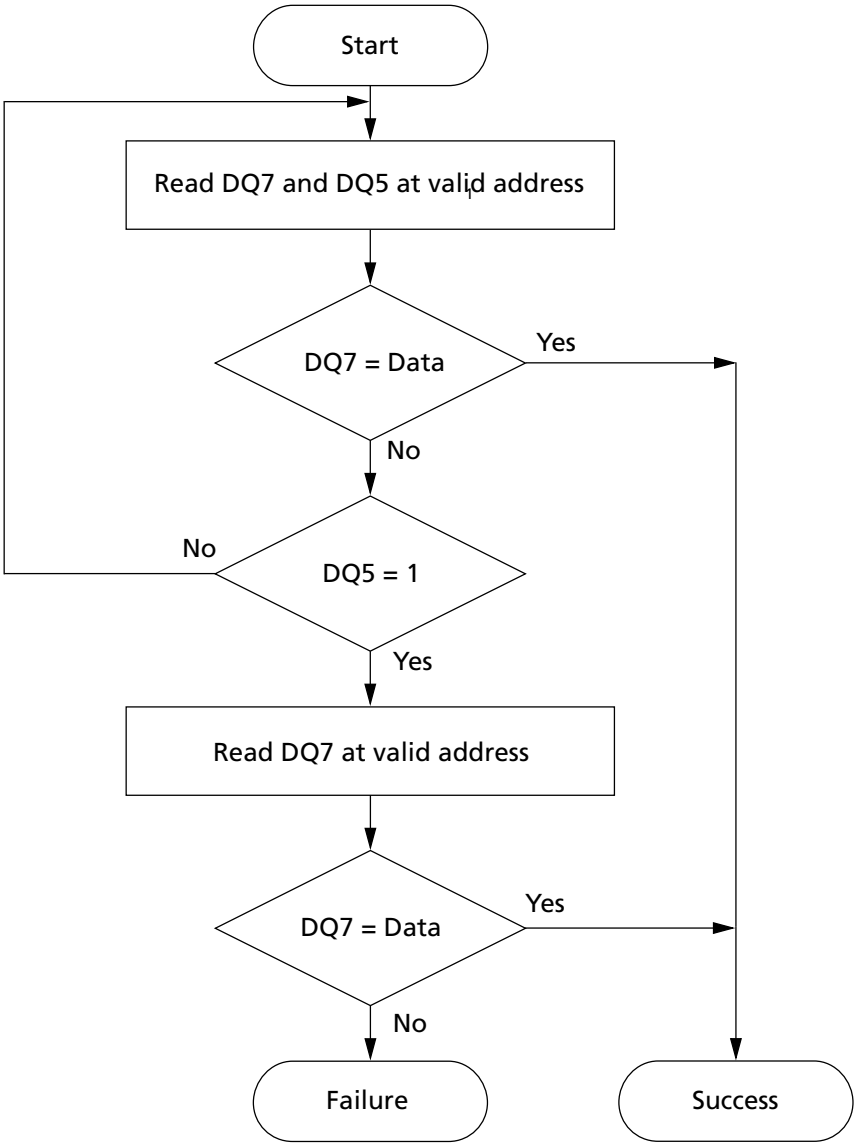
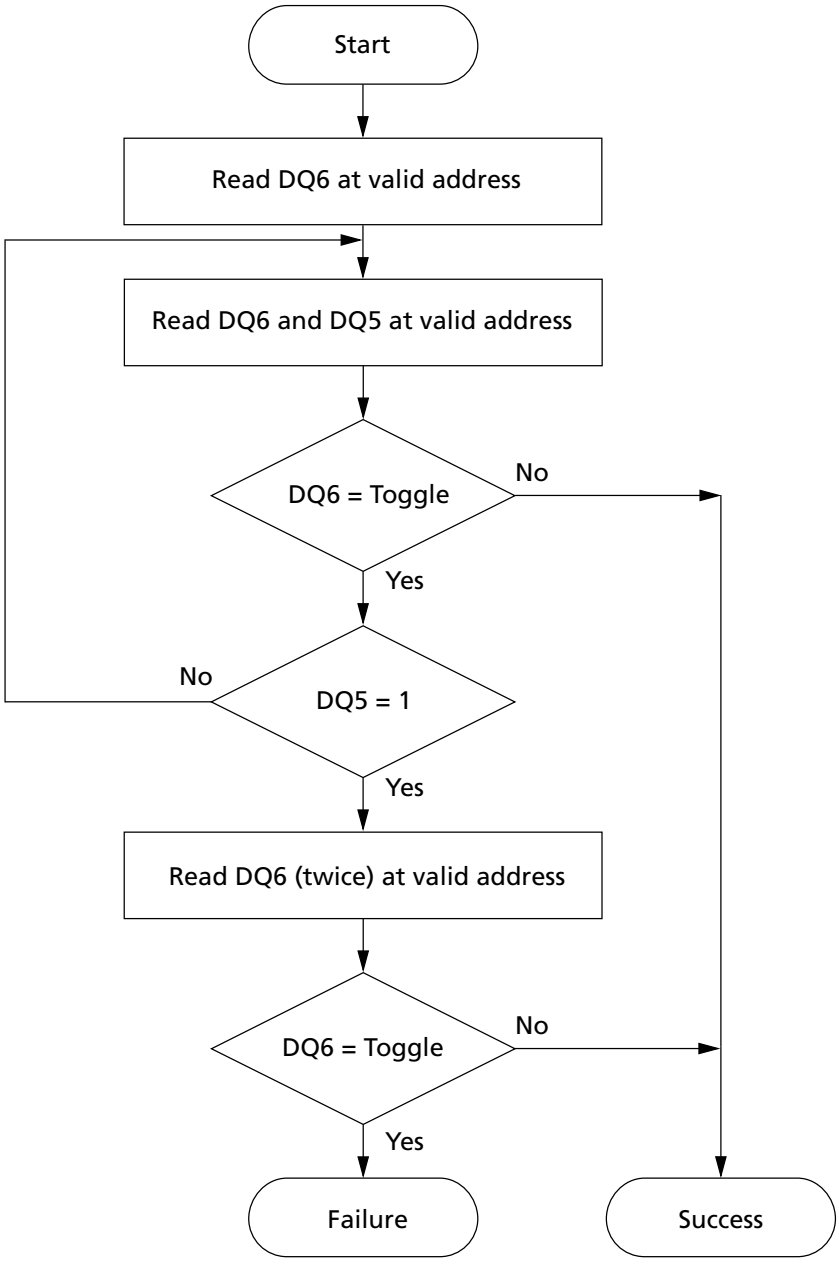


Figure 7: Data Toggle Flowchart



READ Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is valid only when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area. A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

AUTO SELECT Operations

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command or by applying V_{ID} to A9. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information.
- Block protection, which includes the block protection status and extended memory block protection indicator.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

To enter auto select mode by applying V_{ID} to A9 (see the following tables).

Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 12: Read Electronic Signature

Note 1 applies to entire table

Signal	READ Cycle						Notes
	Manufacturer Code	Device Code 1	Device Code 2		Device Code 3		
			GH/GL	GT/GB	GH/GT	GL/GB	
CE#	L	L	L	L	L	L	
OE#	L	L	L	L	L	L	
WE#	H	H	H	H	H	H	
Address Input, 8-Bit and 16-Bit							
A[MAX:10]	X	X	X	X	X	X	
A9	V_{ID}	V_{ID}	V_{ID}	V_{ID}	V_{ID}	V_{ID}	2
A8	X	X		X		X	
A[7:5]	L	L		L		L	
A4	X	X		X		X	
A[3:1]	L	L		H		H	
A0	L	H		L		H	
Address Input, 8-Bit Only							