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SmartFusion2 SoC FPGA Evaluation Kit

User Guide

Microsemi

Table of Contents

1 – Introduction

The SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) Evaluation Kit (M2S-EVAL-KIT) is restriction of hazardous substances (RoHS) compliant and enables the designer to develop applications that involve one or more of the following:

- Motor control
- System management
- Industrial automation
- High-speed serial I/O applications like peripheral component interconnect express (PCIe), serial gigabit media independent interface (SGMII), and user customizable serial interfaces

Kit Contents

Table 1 lists the contents of the M2S-EVAL-KIT.

Table 1 Kit Contents

Quantity	Description
1	SmartFusion2 SoC FPGA 25K LE M2S025T-1FGG484
1	12 V/2 A Wall-Mounted Power Supply
1	FlashPro4 JTAG programmer
1	USB 2.0 A-male to mini-B Y-cable for UART/power interface (up to 1 A) to PC
1	Quickstart Guide
1	Libero SoC Gold Software License
1	PCIe Control Plane Demo Design
Note: The M2S-Eval-KIT is RoHS compliant.	

SmartFusion2 SoC FPGA Evaluation Kit Web Resources

M2S-EVAL-KIT web resources are available at:

www.microsemi.com/products/fpga-soc/design-resources/dev-kits/SmartFusion2/smartfusion2-evaluation-kit#overview

Board Description

The M2S-EVAL-KIT Kit offers a full-featured Evaluation Board for SmartFusion2 SoC FPGAs. This kit inherently integrates the following on a single chip:

- Reliable flash-based FPGA fabric
- A 166 MHz ARM® Cortex™-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded nonvolatile memory (eNVM)
- Industry-required high-performance communication interfaces

The board has numerous interfaces including an RJ45 for 10/100/1000 Ethernet, one full-duplex serializer and deserializer (SERDES) lane through sub miniature version A (SMA) connectors, a 64-bit GPIO Header, and various connectors for serial peripheral interface (SPI) support.

The SmartFusion2 memory management system is supported by 512 Mb of on board mobile low-power double data rate (LPDDR) SDRAM memory and 64 Mb SPI flash. The SERDES block can be accessed through the PCIe edge connector or high-speed sense multiple access (SMA) connectors.

- The board supports the M2S025T device in an FGG484 package
- The board is eight layers PCB and manufactured with FR4 dielectric material.

Block Diagram

Figure 1 shows the M2S-EVAL-KIT block diagram:

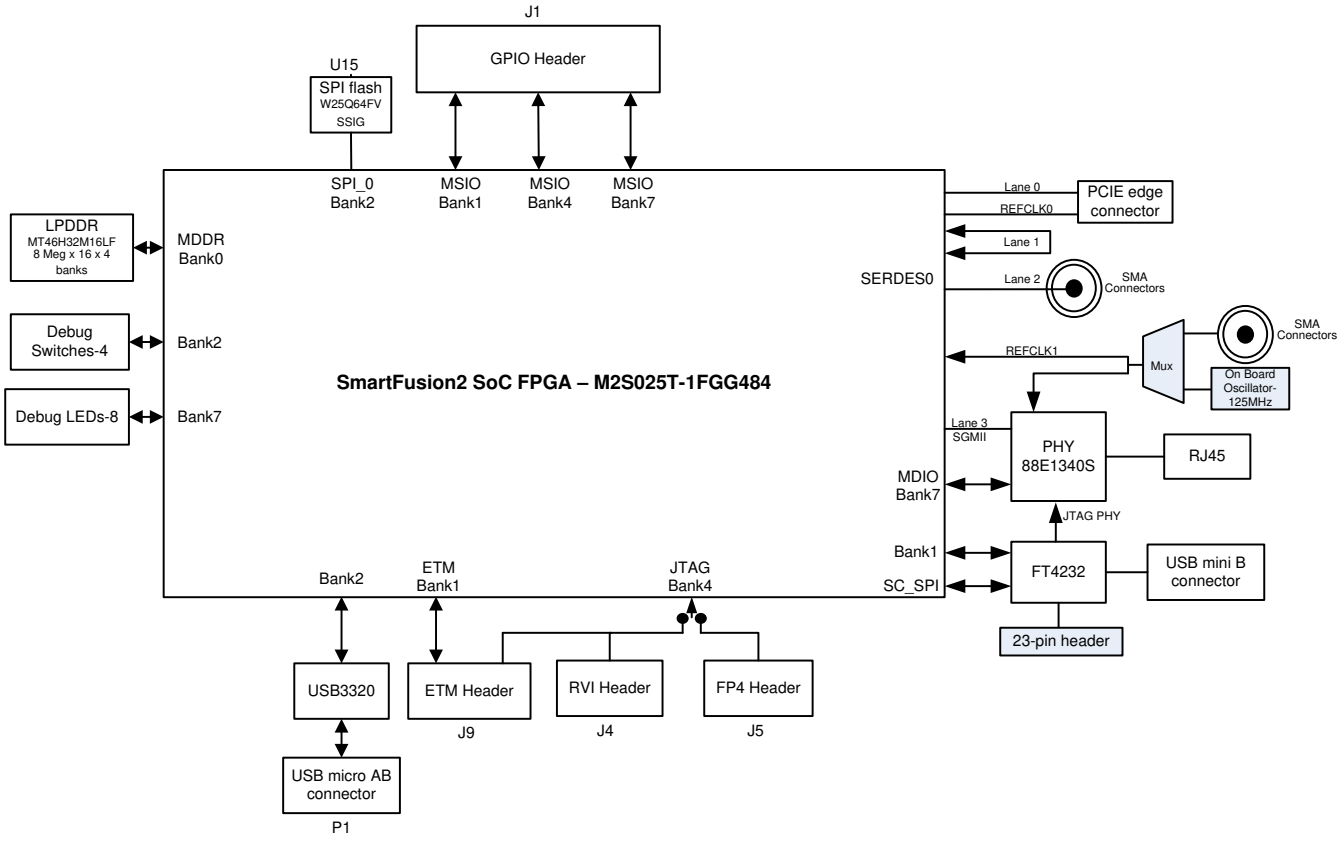

Figure 1 SmartFusion2 SoC FPGA Evaluation Kit Block Diagram

Board Overview

Figure 2 shows an overview of the M2S-EVAL-KIT features.

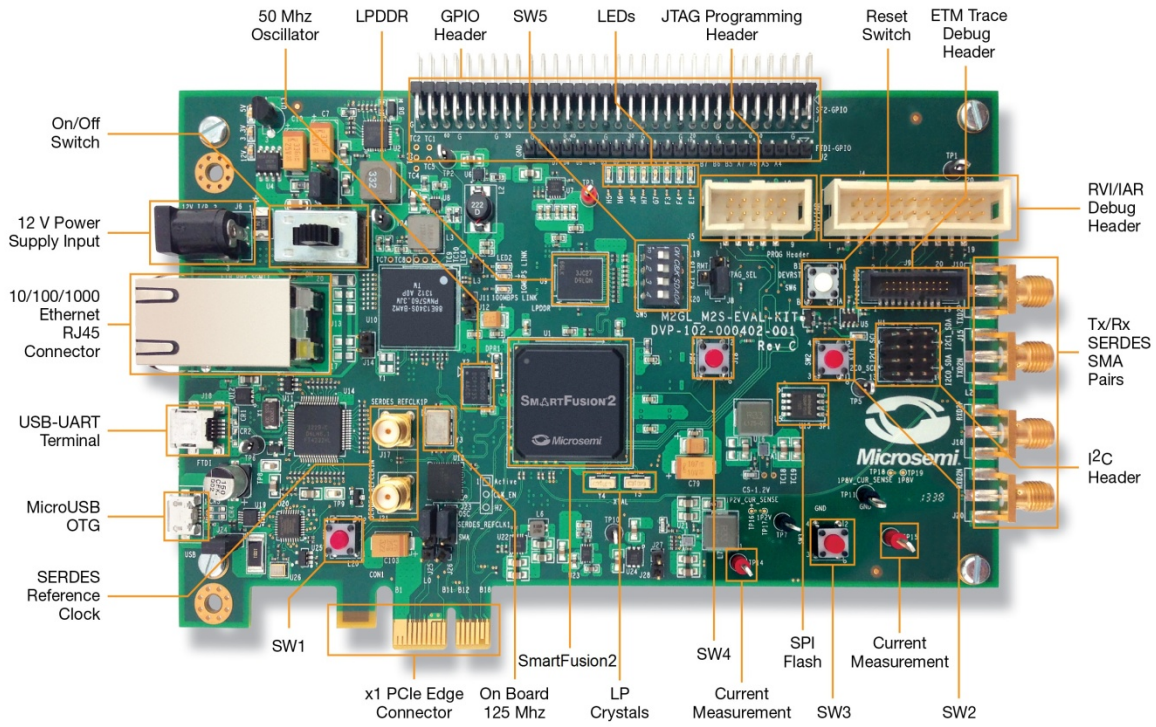

Figure 2 SmartFusion2 SoC FPGA Evaluation Kit Board Overview

Note: Microsemi® recommends SMA Male to SMA Male Precision Cable 12 Inch length using PE-SR405FLJ Coax, RoHS to use with SmartFusion2 Evaluation Kit. For more information, refer to www.pasternack.com/sma-male-sma-male-pe-sr405flj-cable-assembly-pe39429-12-p.aspx

I/O Voltage Rails

Table 2 lists the bank I/Os with voltage rails.

Table 2 I/O Voltage Rails

SmartFusion2 Bank	I/O Rail	Voltage
Bank0	VDDI0	1.8 V
Bank1	VDDI1	3.3 V
Bank2	VDDI2	3.3 V
Bank3	VDDI3	3.3 V
Bank4	VDDI4	3.3 V
Bank5	VDDI5	2.5 V
Bank6	VDDI6	2.5 V
Bank7	VDDI7	3.3 V

Table 3 describes the M2S -EVAL-KIT components.

Table 3 SmartFusion2 SoC FPGA Evaluation Kit Board Components

Name	Description
M2S025T-1FGG484	Microsemi SmartFusion2 SoC FPGA
Mobile Low-Power DDR SDRAM	512 Mb (MT46H32M16LF – 8 Meg x 16 x 4 banks) for storing the data bits.
SPI flash	64 Mb SPI flash Winbond electronics W25Q64FVSSIG connected to SPI port 0 of the SmartFusion2 FPGA high performance memory system (HPMS).
Ethernet	RJ45 connector (Ethernet jack with magnetic) interfacing with Marvell 10/100/1000 BASE-T PHY chip 88E1340S in serial gigabit media independent interface (SGMII) mode, interfacing with the Ethernet port of the SmartFusion2 FPGA (on-chip MAC and external PHY).
RVI header	RVI header for application programming and debugging from Keil ULINK or IAR J-Link.
FP4 header	FlashPro4 programming header for SmartFusion2 programming and debugging with Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J18) to program the external SPI flash.
Embedded trace macro (ETM) cell header	ETM header for debugging.
GPIO header	General purpose input/output(GPIO) header for multi standard I/O(MSIO) signals to be routed.
PCIe edge connector	PCI Express edge connector with one lane
Dual in-line package (DIP) switch	Debug switch for user application.
Light-emitting diodes (LEDs)	Eight active low LEDs that are connected to some of the user I/Os for debug. Three active high LEDs that are used for power supply indication.
Push–button reset	Push-button system reset for SmartFusion2 system.
Push–button switches	Four push-button switches for test and navigation.
USB interface	USB micro AB connector, interfacing with the high-speed USB2.0 ULPI transceiver chip USB3320, interfacing with FPGA pins of the SmartFusion2 HPMS.
OSC-125	125 MHz clock oscillator(differential output)
OSC-50	50 MHz clock oscillator
OSC-32	32.768 KHz low-power oscillator

2 – Installation and Settings

Software Installation

Download and install the latest release of Microsemi Libero® System-on-Chip (SoC) software v11.1 or later, from the Microsemi website and register for a free Gold license. For instructions on how to install Libero and SoftConsole, refer to the *Libero Installation and Licensing Guide* available on the Microsemi website.

Refer to the *Installing IP Cores and Drivers User Guide* to download and install Microsemi DirectCores, SGCores, and driver firmware cores. These must be localized on the PC where Microsemi Libero is installed while designing with Microsemi FPGAs.

Hardware Installation

The FlashPro4 programmer can be used to program the M2S-EVAL-KIT board.

Jumpers, Switches, LEDs, and DIP Switch Settings

The recommended default jumpers, switches, LEDs, and DIP switch settings are defined in Table 4 through Table 6. .

- Table 4.Jumper Settings
- Table 5.LEDs
- Table 6.Test Points

Connect the jumpers using the default settings to enable the pre-programmed demonstration design to function correctly. Table 4 shows the jumpers along with default settings.

Note: Location of all the jumpers and test points are searchable in Figure 18 on page 40 of 5– Board Components Placement section.

Table 4 Jumper Settings

Jumper	Function	Default Settings
J23	Jumper to select switch-side Mux inputs of A or B to the lineside.	–
	Pin 1-2 (Input A to the line side) that is on board 125 MHz differential clock oscillator output will be routed to line side.	Closed
	Pin 2-3 (Input B to the line side) that is external clock required to source through SMA connectors to the line side.	Open
J22	Jumper to select the output enables control for the line side outputs.	–
	Pin 1-2 (Line side output enabled)	Closed
	Pin 2-3 (Line side output disabled)	Open
J24	Jumper to provide the VBUS supply to USB when using in Host mode.	Open
J8	JTAG selection jumper to select between RVI header or FP4 header for application debug.	–
	Pin 1-2 FP4 for SoftConsole/FlashPro	Closed
	Pin 2-3 RVI for Keil ULINK™/IAR J-Link®	Open
	Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.	Open
J3	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.	–

Jumper	Function	Default Settings
	Pin 1-2 for Manual power switching using SW7 switch.	Closed
	Pin 2-3 for Remote power switch using GPIO capability of FT4232 chip.	Open

Table 5 lists the power supply and Ethernet LEDs.

Table 5 LEDs

LED	Comment
DS1 - Green	Indicates the 5 V rail.
DS2 - Green	Indicates the 3.3 V rail.
DS3 - Green	Indicates the 12 V power source.
DS5 - Green	Connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY.
DS4 - Green	Connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY.
DS6 - Green	Connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY.

Table 6 lists the USB, ground, and other test points.

Table 6 Test Points

Test Point	Description
TP8	USB switch in/out for DP signal.
TP9	USB switch in/out for DM signal.
TP1,TP2,TP4,TP5,TP6,TP7,TP10,TP11	GND
TP3	Test point for DDR_VTT
TP12	Test point to measure the voltage at TP12 with reference to GND.
TP14	1.2 V current sensing test point
TP15	1.8 V current sensing test point
TP16, TP17	Test points across current sense resistor 0.05 Ohms for 1.2 V
TP18, TP19	Test points across current sense resistor 0.05 Ohms for 1.8 V

SmartFusion2 Power Sources

All the power supply devices used in the SmartFusion2 SoC FPGA Evaluation Kit are Microsemi devices. For more information on power supply devices refer to www.microsemi.com/product-directory/ics/853-power-management

Voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) provided on the board is shown in Figure 3.

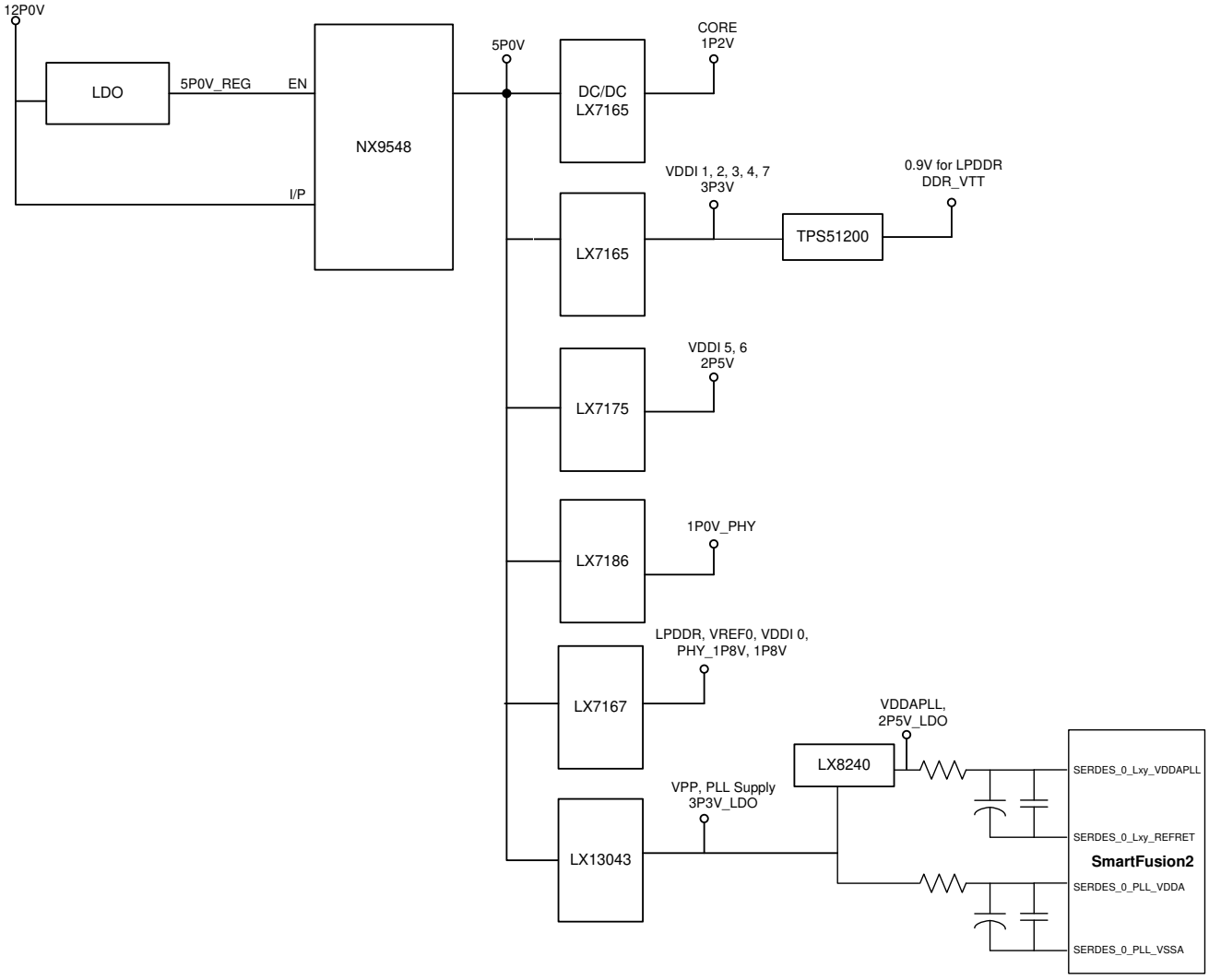

Figure 3 Voltage Rails in the SmartFusion2 SoC FPGA Evaluation Kit

Testing the Hardware

If the board is shipped directly from Microsemi, it contains a test program that determines whether or not the board works properly. If the board is found damaged, the manufacturing test can be rerun to verify the key interfaces of the board functionality.

Refer to www.microsemi.com//download/rsc/?f=%20M2S-EVAL-KIT-PP_Mfg_PF (to be released) for manufacturing test procedures.

3 –Key Components Description and Operation

This chapter describes the key component interfaces. For device datasheets, refer to:
www.microsemi.com/document-portal/doc_download/132042-smartfusion2-fpga-datasheet

Powering Up the Board

The board can be powered through either of two 12 V sources that are, external +12 V/2 A DC jack or PCIe connector as shown in Figure 4 Protection mechanism enables the external DC jack supply, if both the sources are available, simultaneously.

When both the power sources are ON, board takes the power from external DC jack as Diode D3 becomes reverse biased and path will be open for 12P0_PCIE. When the external DC voltage is not present, the board can be powered up using the PCIe connector.

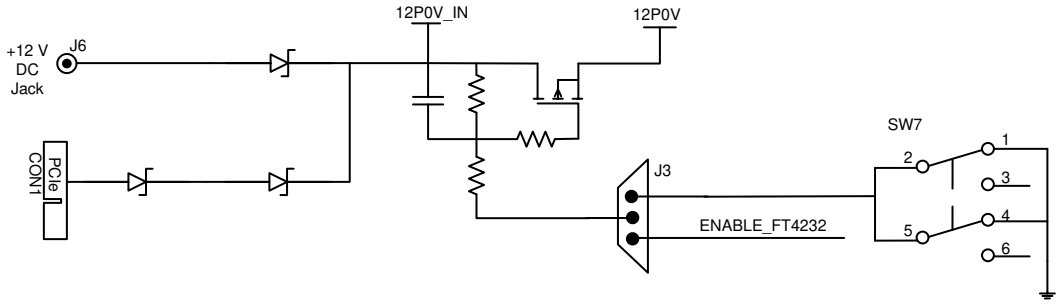

Figure 4 Powering Up the Board

Current Measurement

1.2 V Current Sensing for Normal Operation

For applications which require current measurement high precision operational amplifier circuitry (U31 with gain 100) is placed on the board to measure the output voltage at TP14 test point with reference to the ground.

Core power can be measured by running the following steps:

1. Measure the output voltage (VOUT) at TP14.
2. I = (VOUT/5)
3. Core power consumed P= (1.2 V)*I

For example, when the voltage measured across TP14 as 0.5 V, then the consumed core power is 0.12 W.

Figure 5 shows the onboard core power measurement circuitry.

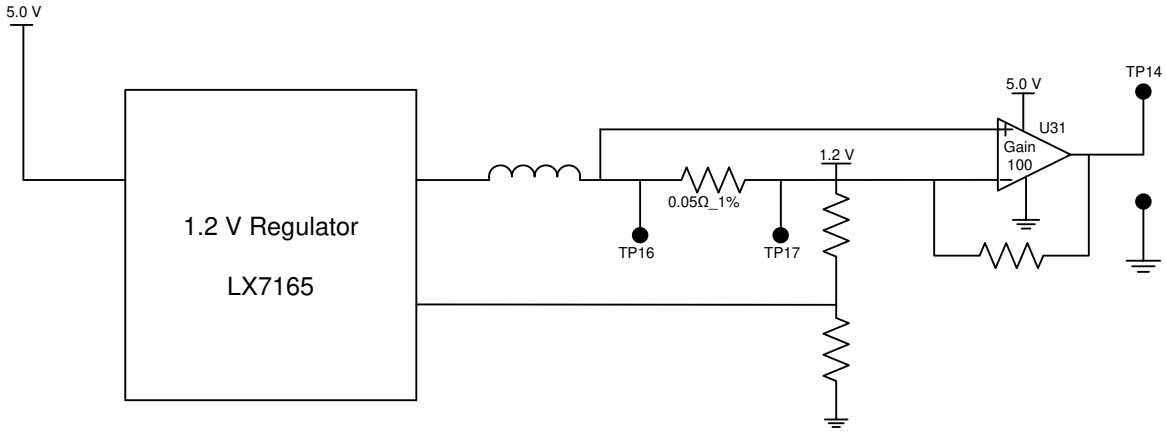

Figure 5 Core Power Measurement Circuitry

1.2 V Current Sensing for Flash*Freeze

The SmartFusion2 device consumes very low-power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ohms) needs to be measured directly using a precision digital multi-meter that can read sub milli-volts. Test points TP16 and TP17 can be used to directly measure voltage across the 1.2 V sense resistor.

To convert the voltage measured across sense resistor to power, use the following equation:

$$Power = (\frac{\text{voltage\_measured\_in\_milli\_volts}}{0.05}) * 1.2$$

1.8 V Current Sensing

For applications which require current measurement high precision Operational Amplifier circuitry (U32 with gain 100) is placed on the board to measure the output voltage at TP15 test point with reference to the ground.

1.8 V power can be measured by running the following steps:

1. Measure the output voltage (VOUT) at TP15.
2. I = (VOUT/5)
3. Power consumed P= (1.8 V)*I

For example, when the voltage measured across TP15 as 0.5 V, then the consumed core power is 0.18 W.

Figure 6 shows the onboard 1.8 V power measurement circuitry.

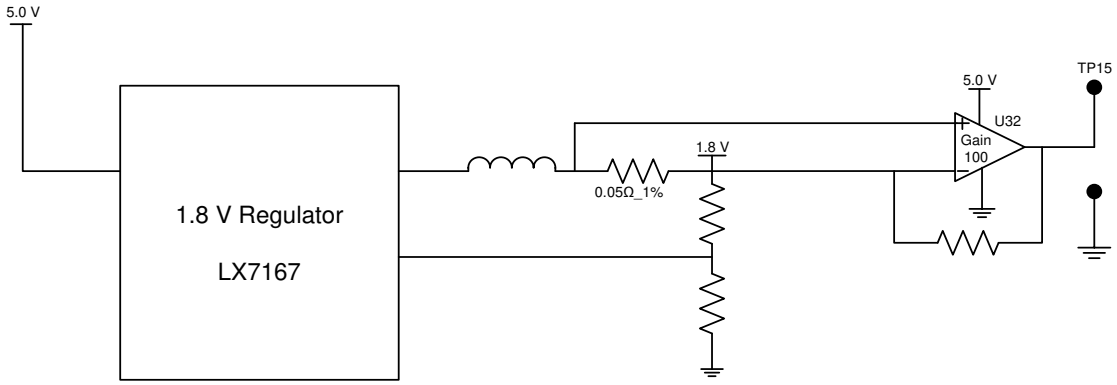

Figure 6 1.8 V Power Measurement Circuitry

Note: The measured accuracy is ± 10%.

Memory Interface

Dedicated I/Os are provided for HPMS DDR and fabric DDR for the SmartFusion2 device. Apart from the dedicated I/Os, regular I/Os can also be used to connect to other memory devices. Refer to Figure 7.

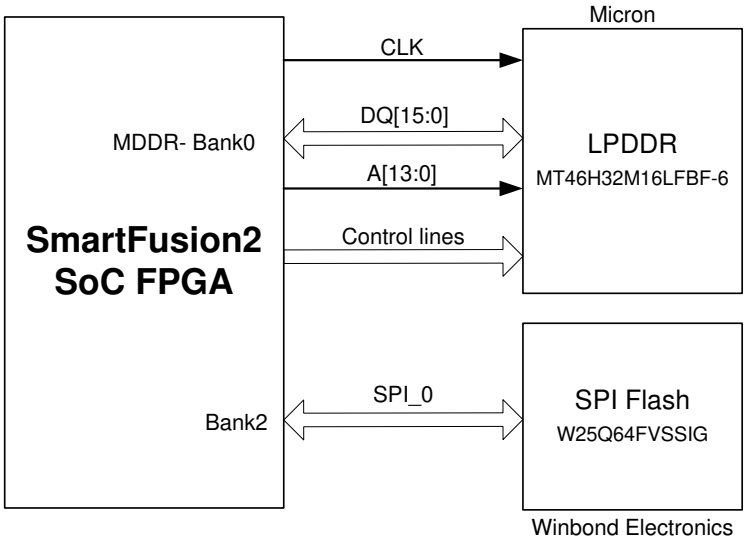

Figure 7 SmartFusion2 Memory Interface

Mobile LPDDR SDRAM

An individual chip, 512 Mb LPDDR SDRAM memory is provided as flexible volatile memory for user applications. The LPDDR interface is implemented in bank 0. The specifications of LPDDR SDRAM are listed below:

- MT46H32M16LF – 8 Meg x 16 x 4 banks
- Density: 512 Mb
- Data rate: LPDDR 16-bit at 400 Mbps = 6.4 Gbps

Note: For more information, refer to page 3 of Board Level Schematics document (provided separately).

SPI Serial Flash

The specifications of SPI Flash are listed below:

- Density: 64 Mb
- Voltage: 2.7 V - 3.6 V
- Frequency: 104 MHz
- Supports: SPI modes 0 and 3
- SmartFusion2 HPMS - SPI0 interfaced to SPI flash

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

SERDES0 Interface

The SERDES0 is having four lanes connected as below:

1. Lane 0 is directly routed to the PCIe connector.
   - TX Pad → trace → AC Coupling→trace →via (to bottom layer)→ trace→PCIe connector pad
   - RX Pad→ trace → PCIe connector pad
2. Lane 1 is used for loopback testing. This path is routed between the Tx and Rx with a 6 inch trace and 2 vias.
   - TX Pad → via (to Bottom layer) → trace → AC Coupling→ trace → via (to top layer) → RX pad
3. Lane 2 routed to SMA connectors.
   - TX Pad → trace → AC Coupling→trace → SMA connector pad
   - RX Pad→trace→via (to bottom layer)→trace→via (to top layer)→ SMA connector Pad
4. Lane 3 is routed to Marvell PHY (88E1340S).
   - TX pad→trace→AC Coupling→trace→via→trace routed in (6th layer)→via (to top layer)→Marvel PHY pin
   - RX pad→via→trace routed in 6th layer→via (to top layer)→trace→AC Coupling→trace→Marvel PHY pin

SERDES0 reference clock 0 is routed directly from the PCIe connector to SmartFusion2 FPGA.

SERDES0 reference clock 1 is routed from the onboard 125 MHz clock oscillator and optionally routed from SMA connectors through LVDS Mux/Buffer chip.

Expected SERDES reference clock specifications:

- Voltage level: 3.3 (± 0.3)V
- Differential LVDS
  - Symmetry: 50% (± 10%)
  - Rise/Fall Time: 1nsec Max @ 20% to 80% of supply (3.3V)
  - Output Voltage Levels: “0”=0.90 Minimum, 1.10 Typical
    “1”=1.43 Typical, 1.60 Maximum
  - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

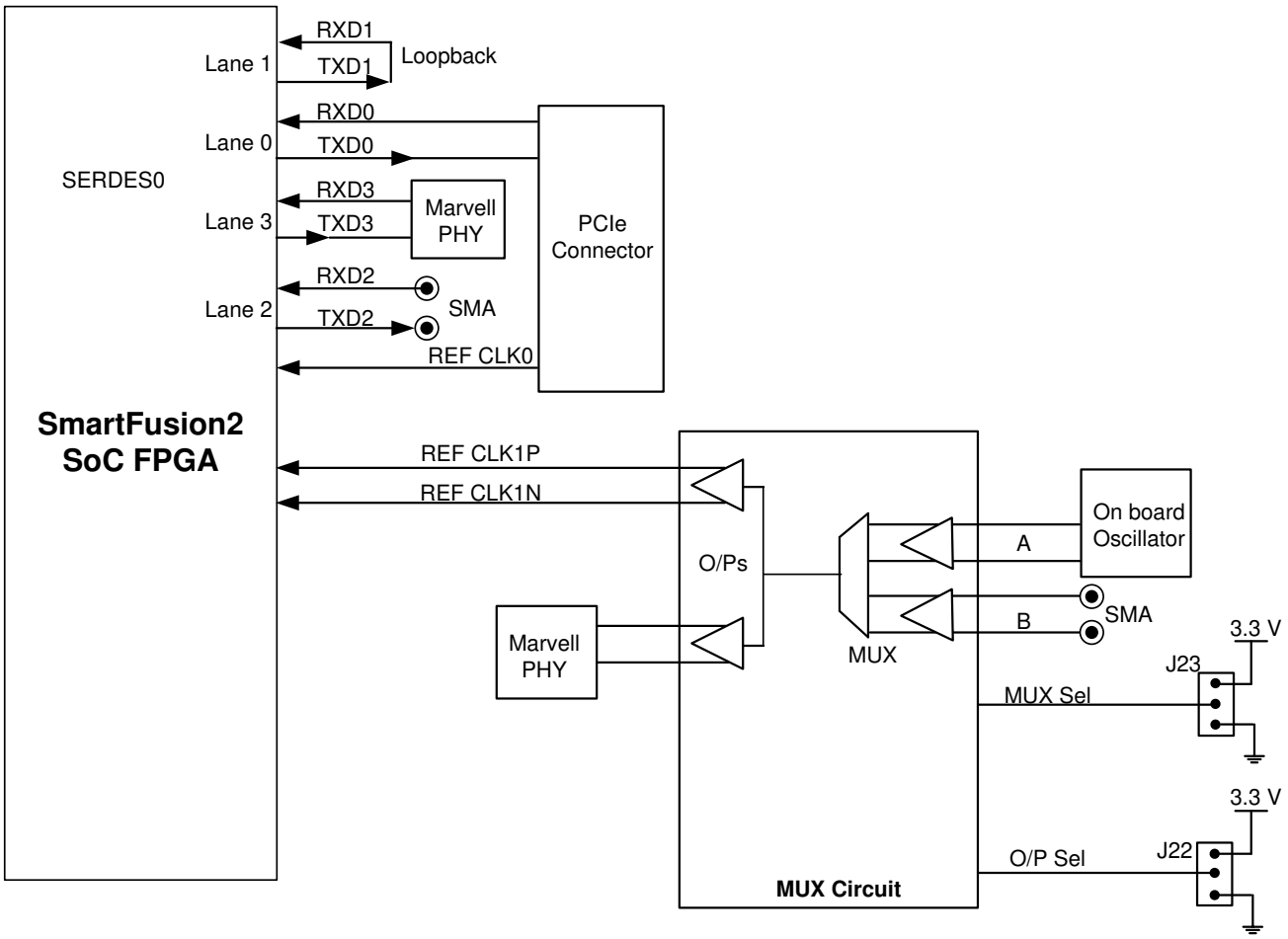

Figure 8 SERDES0 Interface

For more information on J22 and J23 jumpers, refer to Table 4.

Note:

- SERDES0 TXD pairs are capacitively coupled to the SmartFusion2 device. Series AC coupling capacitors are used to provide common mode voltage independence.
- The AC coupling capacitors are not provided for SERDES 0 RXD signals. The mating board should have the AC coupling capacitors.
- For more information, refer to page 4 of Board Level Schematics document (provided separately).

USB Interface

The SMSC USB3320 is a high-speed USB 2.0 ULPI transceiver. It includes full support for the optional OTG protocol.

CPEN: External 5 V supply enables. It controls the external VBUS power switch.

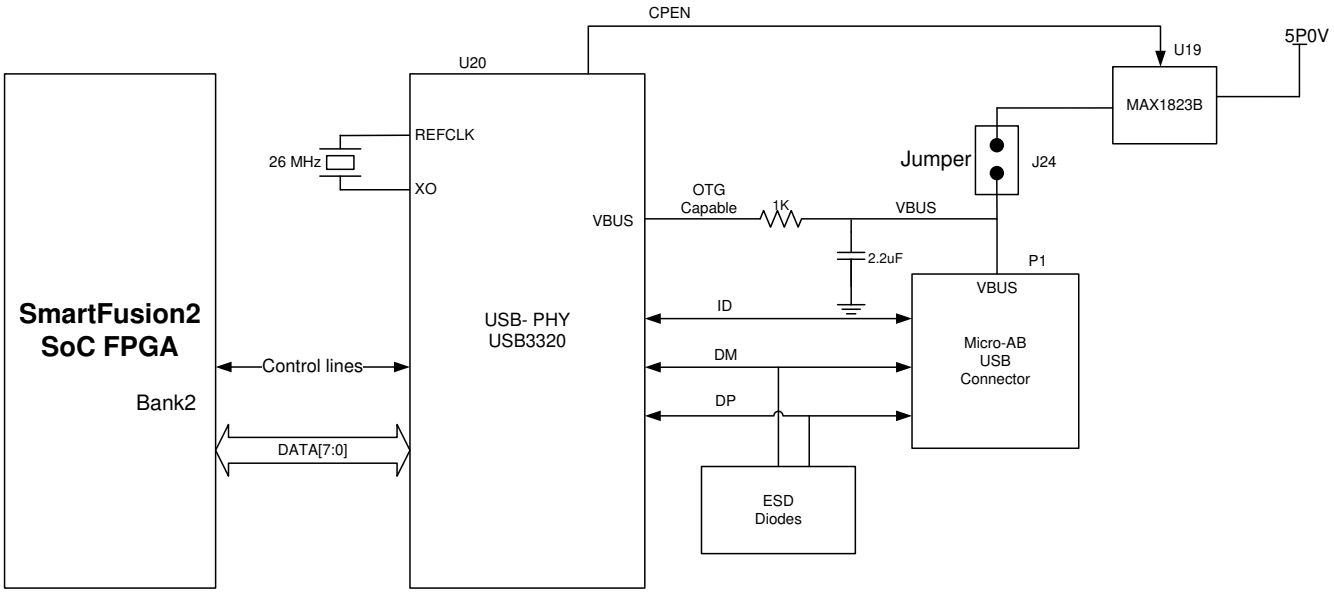

Figure 9 USB Interface

Note: For more information, refer to page 10 of Board Level Schematics document (provided separately).

Marvell PHY (88E1340S)

The SmartFusion2 Evaluation Kit utilizes the on board Marvell Alaska PHY device (88E1340S) for Ethernet communications at 100 or 1000 Mbps. 88E1340S has four independent gigabit Ethernet transceivers, but the board uses only one transceiver. Each transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on CAT5 twisted pair cable. The PHY connection to a user-provided Ethernet cable is through an RJ-45 connector with built-in magnetics.

The 88E1340S device supports the quad SGMII for direct connection to anSmartFusion2 chip. Refer to Figure 10.

The 88E1340S is configured through the CONFIG [3:0] pins and CLK_SEL [1:0].

CLK_SEL [1:0] is used to select the reference clock input option. On board, the status of CLK_SEL0 is High and CLK_SEL1 is Low. REF_CLK is the 125 MHz reference differential clock input. It consists of LVDS differential inputs with a 100Ω differential internal termination resistor.

- RCLK – Gigabit recovered clock
- SCLK – 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications
  - Voltage level: 3.3 (± 0.3)V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/Fall Time: 1nsec Max @ 20% to 80% of supply (3.3V)
    - Output Voltage Levels: 0: 0.90 Minimum, 1.10 Typical
      1: 1.43 Typical, 1.60 Maximum
    - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

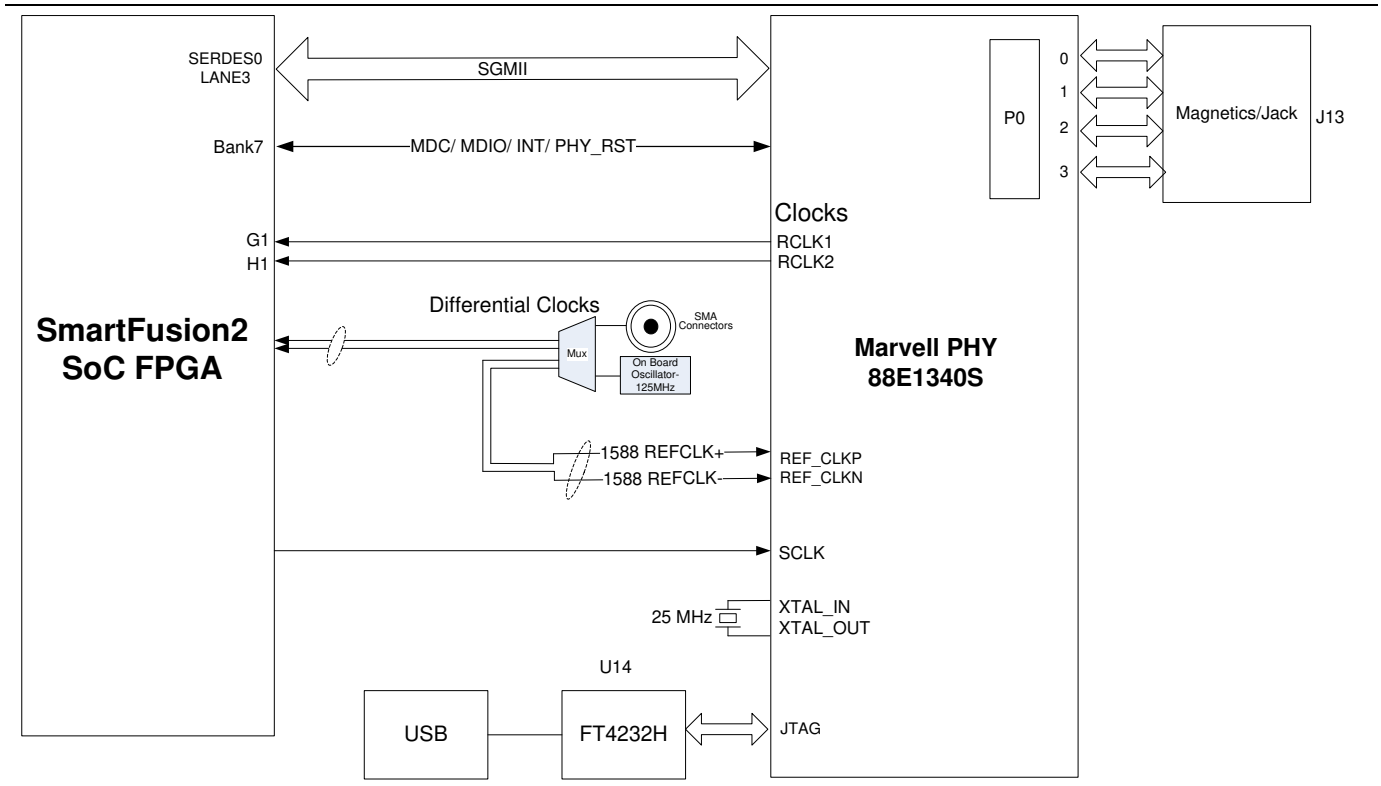

Figure 10 SmartFusion2 Marvell PHY Interface

Note: For more information, refer to page 11 and 12 of Board Level Schematics document (provided separately).

Programming

The SmartFusion2 device can be programmed through the JTAG interface. Figure 11 shows various ways of SmartFusion2 programming.

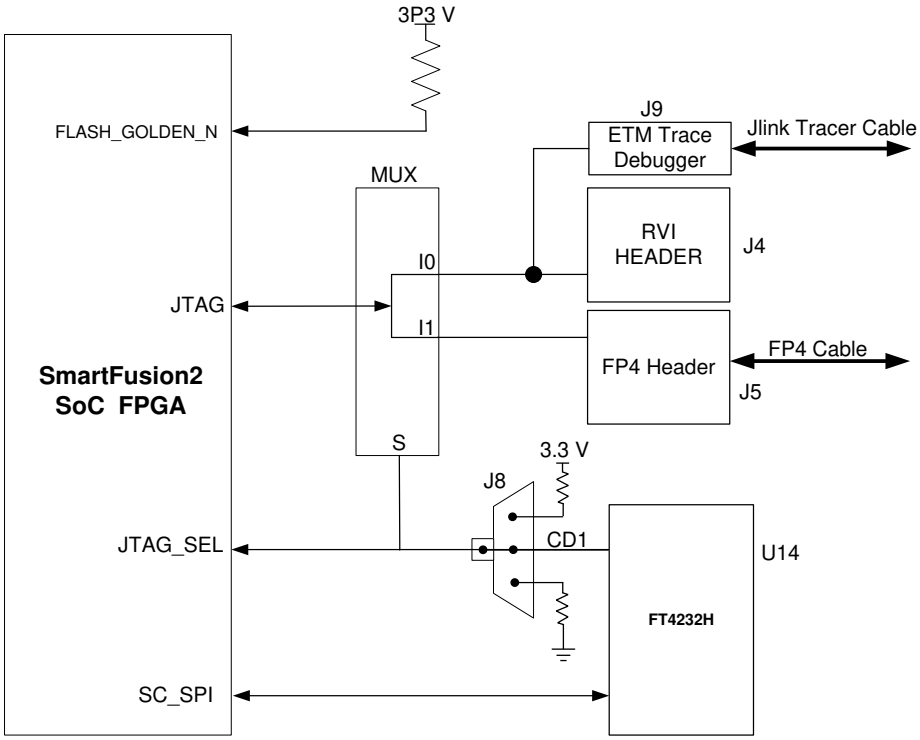

Figure 11 SmartFusion2 Programming Interface

JTAG_SEL: JTAG_SEL is used to switch between FP4 header (High) and RVI header or ETM header (Low).

For more information on J8 jumper, refer to Table 4. .

RVI Header

One 10X2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger.

FlashPro4 Programming Header

The SmartFusion2 device on the Evaluation Kit can be programmed using a FlashPro4 programmer. In addition, FlashPro4 is used for software debugging by SoftConsole.

Note:

- For more information, refer to page 13 of Board Level Schematics document (provided separately).
- For more details, refer to the *SmartFusion2 Programming User Guide*.

FTDI Interface

Following are the FT4232H chip features:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB to quad serial ports with a variety of configurations
- Entire USB protocol handled on the chip. USB specific firmware programming is not required
- USB 2.0 high-speed (480 Mbps) and full Speed (12 Mbps) compatible
- Two MPSSE on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware or X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing (+5 V tolerant)

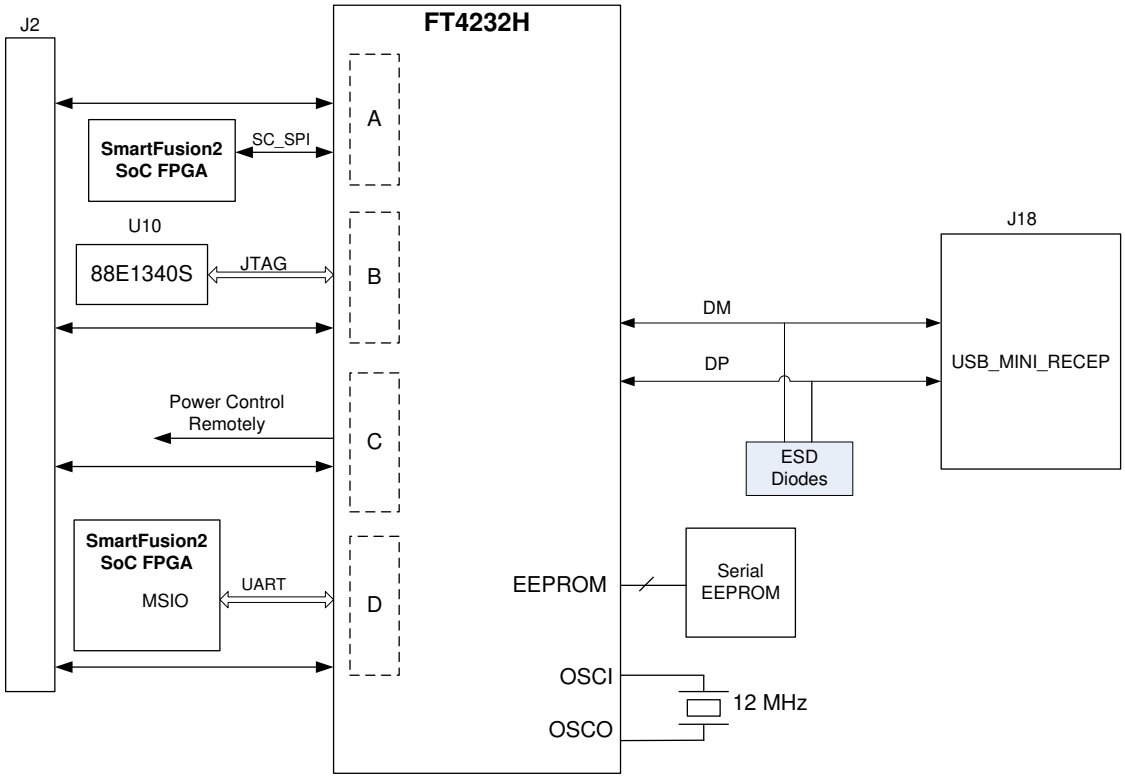

Figure 12 FTDI Interface

Note: For more information, refer to page 14 of Board Level Schematics document (provided separately).

I²C Port Header

Table 7 shows the two I²C ports routed to header – H1:

Table 7 I2C Port Header

Pin Number	SmartFusion2 Pin Name	Board Signal Name	Header - H1
G16	MSIO48NB1/I2C_0_SCL/GPIO_31_B	I2C0_SCL	10, 14
G17	MSIO48PB1/I2C_0_SDA/GPIO_30_B	I2C0_SDA	11, 15
R22	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/ GPIO_1_A	I2C1_SCL	2, 6
P22	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/ GPIO_0_A	I2C1_SDA	3, 7

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

System Reset

The DEVRST_N signal (active low) is asserted, if the power supply level 3.3 V or 1.2 V fall below the threshold level or by pressing the SW6 (push-button switch). DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

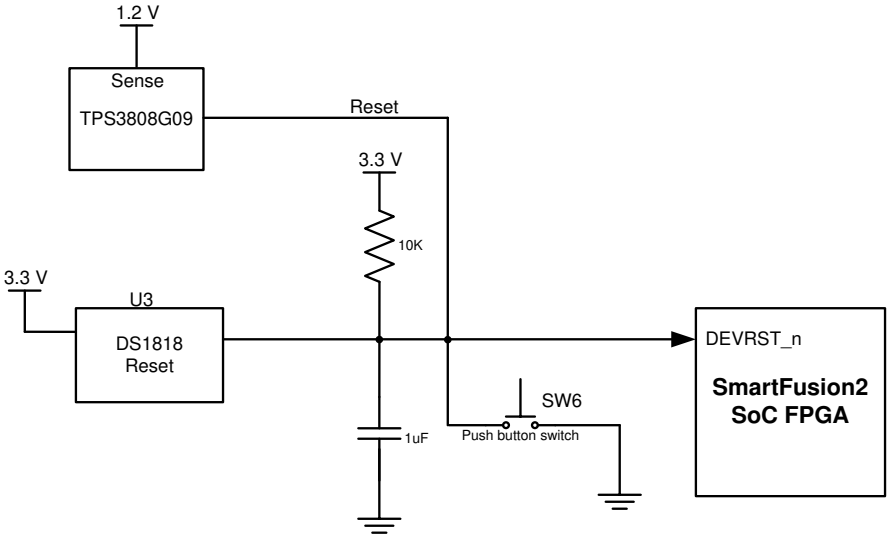

Figure 13 System Reset Interface

Note: For more information, refer to page13 of Board Level Schematics document (provided separately).

Clock Oscillator

50 MHz Clock Source

Figure 14 shows the 50 MHz clock oscillator with +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high precision clock frequencies.

Table 8 50 MHz Clock

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
50MHZ_ SECLK_ WST_K1	K1	MSIOD121PB7/CCC_SW0_CLKI0

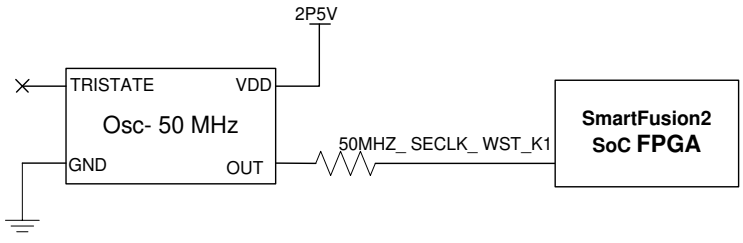

Figure 14 Clock Oscillator Interface

Note: For more information, refer to page 6 of Board Level Schematics document (provided separately).

Different Clock Sources

Following are the different clock sources used in M2S-EVAL-KIT:

- 125 MHz clock oscillator. For more information refer to SERDES0 Interface.
- 32.768 KHz crystal oscillators for main and auxiliary oscillators of SmartFusion2 SoC FPGA.

Debugging

User LEDs

The board provides user access to eight active low LEDs, which are connected to the SmartFusion2 device for debugging applications. Table 9. lists the onboard debugging LEDs.

Table 9 LEDs

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
LED0 - Yellow	E1	MSIO105PB8
LED1 – Yellow	F4	MSIO106NB8
LED2 – Green	F3	MSIO106PB8
LED3 – Green	G7	MSIO107NB8
LED4 – Red	H7	MSIO107PB8
LED5 – Red	J6	MSIO108NB8
LED6 – Blue	H6	MSIO108PB8
LED7 - Blue	H5	MSIO109NB8

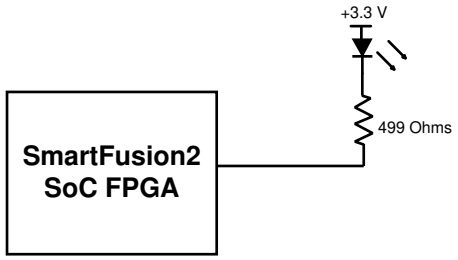

Figure 15 LEDs Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Push-Button Switches

The SmartFusion2 Evaluation Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. Table 10 lists the onboard push-button switches.

Table 10 Push-Button Switches

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
SWITCH1	L20	MSIO17NB3
SWITCH2	K16	MSIO23NB3
SWITCH3	K18	MSIO24PB3
SWITCH4	J18	MSIO24NB3
SW6	R15	DEVRST_N

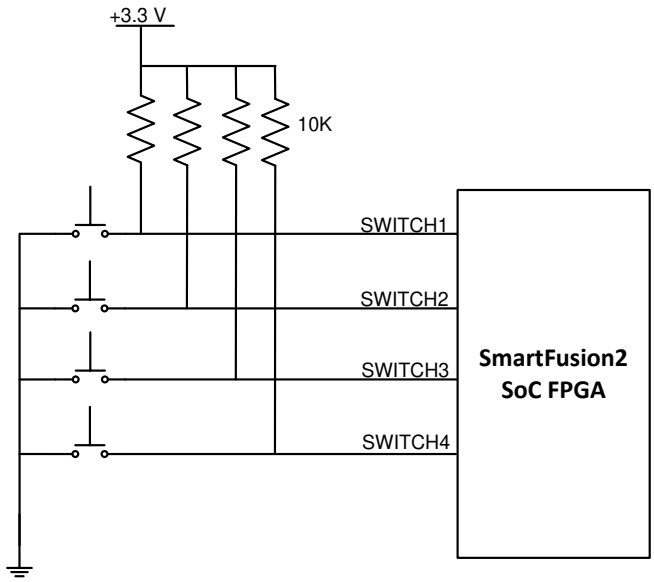

Figure 16 Switches Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Slide Switches–DPDT

SW7–Power ON/OFF switch from external DC Jack, +12 V DC

DIP Switch- SPST

SW5–is a DIP switch that has four connections to the SmartFusion2 device. Table 11. lists the onboard DIP switches.

Table 11 DIP Switches

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
DIP1	L19	MSIO18PB3
DIP2	L18	MSIO18NB3
DIP3	K21	MSIO19PB3
DIP4	K20	MSIO19NB3

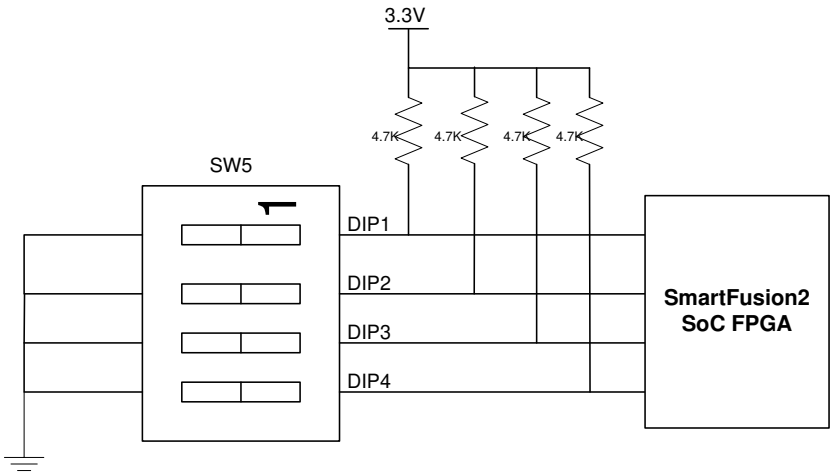

Figure 17 SPST Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

GPIO Header Pin Out

Bank 4, bank 7, and bank 1 signals are routed to the GPIO header for user applications. Table 12 lists the GPIO header pin out details.

Table 12 GPIO Header PinOut

GPIO Header- J1	SmartFusion2 – U1		GPIO Header- J1	SmartFusion2 – U1	
Pin No	**Pkg No**	**Pin Name**	**Pin No**	**Pkg No**	**Pin Name**
1	AB15	DDRIO164PB5	2		3P3V
3	AA15	DDRIO164NB5	4		VSS
5		VSS	6	AA16	DDRIO167PB5
7	AB18	DDRIO177PB5	8	AA17	DDRIO167NB5
9	AB19	DDRIO177NB5	10		VSS
11		VSS	12	AB17	DDRIO174PB5
13	Y18	DDRIO181PB5	14	AA18	DDRIO174NB5
15	Y19	DDRIO181NB5	16		VSS
17		VSS	18	Y17	DDRIO182PB5
19	W16	DDRIO184PB5	20	W17	DDRIO182NB5
21	V16	DDRIO184NB5	22		VSS
23		VSS	24	U14	DDRIO176PB5
25	C22	MSIO47PB1	26	U15	DDRIO176NB5
27	B22	MSIO47NB1	28		VSS
29		VSS	30	V13	DDRIO171PB5
31	Y15	DDRIO172PB5	32	V14	DDRIO171NB5
33	W15	DDRIO172NB5	34		VSS