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PB0115
Product Brief
SmartFusion2 SoC FPGA

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Contents

Tables

Figures

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 25.0

Name change from native SerDes interface to native EPCS SerDes interface in the High-Speed Serial Interfaces, page 25 was updated in revision 25.0.

1.2 Revision 24.0

Following was a summary of changes made in revision 24.0:

- Updated Table 1, page 9 for Automotive grade 2 (SAR 80232).
- Added a note on Automotive grade 2 in the I/Os Per Package, page 10 (SAR 80232)
- Added Automotive grade 2 information in the SmartFusion2 Ordering Information, page 14 (SAR 80232)

1.3 Revision 23.0

Updated Table 1, page 9 with more footnotes. (SAR 66079, SAR 77444, and SAR 73335).

1.4 Revision 22.0

Following was a summary of changes made in revision 22.0:

- Updated Table 1, page 9 (SAR 71992).
- Updated Marking Specification Details, page 16 (SAR 71992).
- Updated Low Power, page 21 (SAR 71992).
- Updated Table 11, page 27 (SAR 71992).

1.5 Revision 21.0

Following was a summary of changes made in revision 21.0:

- Updated Table 3, page 10
- Added Table 6, page 13, Table 7, page 15, Table 8, page 15
- Updated Marking Specification Details, page 16
- Updated Table 11, page 27

1.6 Revision 20.0

Following was a summary of changes made in revision 20.0:

- Updated Table 1, page 9, Table 3, page 10, Table 4, page 11, Table 5, page 12, and Table 10, page 20
- Updated SmartFusion2 Ordering Information, page 14
- Updated Marking Specification Details, page 16
- Updated Table 9, page 19, Table , page 20
- Updated SmartFusion2 Development Tools, page 26

1.7 Revision 19.0

Following was a summary of changes made in revision 19.0:

- Updated Table 1, page 9, Table 3, page 10, Table 4, page 11, Table 5, page 12, and Table 10, page 20
- Removed all instances of and references to M2S100. VQ144 is replaced with TQ144 (SAR 62858).
- Updated SmartFusion2 Ordering Information, page 14
- Updated Table 9, page 19 and Table 10, page 20

- Updated Table 11, page 27

1.8 Revision 18.0

Following was a summary of changes made in revision 18.0:

- Ordering information added to Table 2, page 10 and Table 3, page 10 for the M2S090(T) device in the FCS/FCSG325 package.
- Trademark changed to the Register mark for ARM Cortex-M3.

1.9 Revision 17.0

Updated Device Packages 005-VF256 and 150-FCS536 in Table 2, page 10 and Table 5, page 12.

1.10 Revision 16.0

Updated Table 3, page 10, Table 4, page 11, and Table 5, page 12.

1.11 Revision 15.0

Following was a summary of changes made in revision 15.0:

- Table 1, page 9 to Table 10, page 20 and SmartFusion2 Ordering Information, page 14 were updated with Military device data.
- Table 10, page 20 and the Marking Specification Details, page 16 were added.

1.12 Revision 14.0

Following was a summary of changes made in revision 14.0:

- Tables 3-6 were combined into Table 4, page 11.
- Fabric Interface Controller features were added to Table 1, page 9.
- Packages VQ144 and FCV484 were added to Table 2, page 10 and Table 4, page 11.

1.13 Revision 13.0

Following was a summary of changes made in revision 13.0:

- Data Security Feature sections and Device Status table were removed.
- Figure 1, page 8 was updated.

1.14 Revision 12.0

Following was a summary of changes made in revision 12.0:

- Packages FCS325 and VF256 were added to Table 2, page 10.
- SmartFusion2 Ordering Information, page 14 was updated.
- Typo fixed on Figure 1, page 8.

1.15 Revision 11.0

Following was a summary of changes made in revision 11.0:

- LSRAM x32/36 widths added. In Table 1, page 9, notes are added referring to updates in Table 3, page 10 –Table 5, page 12 and Table 6.
- SmartFusion2 Ordering Information, page 14 was updated. Part Numbers (tables 7 and 8) were removed. SmartFusion2 Device Status, page 16 was updated.
- M2S090-FG676 and M2S005-VF400 package pinouts finalized.

1.16 Revision 10.0

M2S005-FG484 package pinout I/O count finalized. Typos were corrected.

1.17 Revision 9.0

Following was a summary of changes made in revision 9.0:

- A note regarding total logic was added to Table 1, page 9.
- Design Security Features, page 19 and Data Security Features, page 20 were added to show the security features supported.

1.18 Revision 8.0

Following was a summary of changes made in revision 8.0:

- Figure 1, page 8 was revised to clarify the connections between the Cortex-M3 processor and cache (SAR 45967).
- I/O counts were updated in Table 1, page 9 (SAR 46000).
- I/O counts and devices were updated. The FG676 package was added to Table 3, page 10 (SAR 46000).
- Features per Device/Package Combination was divided into four new tables, Table 3 through Table 6 to accommodate new features for package/device combinations for the FG676 package, for T and non-T devices (SAR 46000).
- The status for M2S050T was changed from Advance to Preliminary in the SmartFusion2 Device Status, page 16 (SAR 46967).

1.19 Revision 7.0

Following was a summary of changes made in revision 7.0:

- The SmartFusion2 product brief has been separated from the rest of the SmartFusion2 datasheet. The SmartFusion2 Development Tools, page 26 has been updated and is now part of the product brief (SAR 45184).
- The M2S090 device is new. The product family tables and ordering information have been updated (SAR 45127).

1.20 Revision 6.0

The number of PLLs and CCCs for MS2025 was corrected from 4 to 6 (SAR 44480).

1.21 Revision 5.0

Following was a summary of changes made in revision 5.0:

- Table 1, page 9 and Table 3, page 10 were revised to correct I/O counts for M2S005/M2S025 and the VF400 and FG484 packages (SAR 42618).
- Junction temperature for military, industrial, and commercial SmartFusion2 SoC FPGAs was added to the Reliability section. In the Operating Voltage and I/Os section, market leading number of user I/Os with 5G SerDes was added to the (SAR 42618). LVTTL/LVCMOS 3.3 V was qualified as MSIO only and DDR was removed from the list under DDRIOs (SAR 44652).
- Table 4, page 11 is new (SARs 42618, 44414).
- RMII was removed from as a supported PHY interface in the Triple Speed Ethernet MAC, page 23 (SAR 42618).

1.22 Revision 4.0

Following was a summary of changes made in revision 4.0:

- The SmartFusion2 Ordering Information, page 14 was revised to add Pre-Production as a temperature range. Ambient temperature was corrected to junction temperature in the defined temperature ranges. Speed grades were defined. Table 8 SmartFusion2 Valid Lead-Free Part Numbers for Devices with Design Security is new (SAR 43648).
- The maximum payload size for PCIe was corrected from 256 bytes to up to 2 kbytes. (SAR 42215).
- More information was included on SDRAM Support in the High-Speed Memory Interfaces, page 7 (SAR 42594).

- The phrase, with 16-bit PIPE interface (Gen1/Gen2), was removed from the PCIe bullet in the High-Speed Serial Interfaces, page 25 (SAR 43851).
- In Table 1, page 9, PCIe Endpoint x4 was corrected to PCIe Endpoint ×1, ×2, ×4 (SAR 43851).
- The number of I/Os for M2S025 in the FG484 package was corrected from 267 to 289 in Table 2, page 10 and Table 3, page 10 (SAR 42618).
- The Y security designator was removed from SmartFusion2 Ordering Information (SAR 42231).
- The SGMII PHY Interface, page 24 was revised to change from allocating one of the high-speed serial channels to SGMII and by implementing custom logic in the fabric to allocating one of the high-speed serial channels to and utilizing the CoreTBI soft IP block (SAR 43851).
- The PCI Express, page 25 was corrected to state the SmartFusion2 family has up to four high-speed serial interface blocks rather than two. The following bullets were removed (SAR 43851):
  - Intel's PIPE interface (8-bit/16-bit) to interface between the PHY MAC and PHY (SerDes)
  - Fully compliant PHY PCS sub-layer (125/250 MHz)
- Support for SDRAM memories was removed from the High-Speed Memory Interfaces: DDRx Memory Controllers , page 25 (SAR 42594). The text was corrected to state there are up to three, rather than two, DDR subsystems (SAR 43851).
- The MDDR Subsystem, page 26 was revised to explain that support for 3.3 V Single Data Rate DRAMs (SDRAM) can be obtained by using the SMC_FIC interface (SAR 42594).
- The FDDR Subsystem, page 26 was revised to remove the statement that the APB configuration bus can be mastered by the MSS directly (SAR 42594).
- The SmartFusion2 Development Tools, page 26chapter was revised to indicate that Libero SoC includes SoftConsole (GNU/Eclipse) (SAR 41972).

1.23 Revision 3.0

Following was a summary of changes made in revision 3.0:

- Figure 1, page 8 was updated.
- Table 7, page 15 was added.

1.24 Revision 2.0

Information was updated based on ongoing development of specifications.

1.25 Revision 1.0

Information was reorganized and updated based on ongoing development of specifications.

2 SmartFusion2 SoC FPGAs Product Brief

Microsemi SmartFusion®2 SoC FPGAs integrate the fourth generation flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communications interfaces on a single chip. The SmartFusion2 family is the industry's lowest power, most reliable, and highest security programmable logic solution. SmartFusion2 FPGAs offer up to 3.6X the gate density, up to 2X the performance of previous flash-based FPGA families, and also include multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with an embedded trace macrocell (ETM), memory protection unit (MPU), 8 Kbyte instruction cache, and additional peripherals, including controller area network (CAN), Gigabit Ethernet, and high-speed universal serial bus (USB). High-speed serial interfaces include PCI Express (PCIe), 10 Gbps attachment unit interface (XAUI) / XGMII extended sublayer (XGXS) plus native serialization/deserialization (SerDes) communication, while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

2.1 SmartFusion2 SoC FPGA Features

2.1.1 Reliability

- Single event upset (SEU) immune
  - Zero FIT FPGA configuration cells
- Junction temperature
  - 125 °C—military temperature
  - 100 °C—industrial temperature
  - 85 °C—commercial temperature
  - 125 °C—automotive
- Single error correct double error detect (SECDED) protection on the following:
  - Ethernet buffers
  - CAN message buffers
  - Cortex-M3 embedded scratch pad memory (eSRAMs)
  - USB buffers
  - PCIe buffer
  - DDR memory controllers with optional SECDED modes
- Buffers implemented with SEU resistant latches on the following:
  - DDR bridges (MSS, MDDR, and FDDR)
  - Instruction cache
  - MMUART FIFOs
  - SPI FIFOs
- NVM integrity check at power-up and on-demand
- No external configuration memory required—instant-on, retains configuration when powered off

2.1.2 Security

- Design security features (available on all devices)
  - Intellectual property (IP) protection through unique security features and use models new to the PLD industry
  - Encrypted user key and bitstream loading, enabling programming in less-trusted locations
  - Supply-chain assurance device certificate
  - Enhanced anti-tamper features
  - Zeroization
- Data security features
  - Non-deterministic random bit generator (NRBG)
  - User cryptographic services (AES-256, SHA-256, and elliptical curve cryptographic (ECC) engine)

- User physically unclonable function (PUF) key enrollment and regeneration
- CRI pass-through DPA patent portfolio license
- Hardware firewalls protecting microcontroller subsystem (MSS) memories

2.1.3 Low Power

- Low static and dynamic power
  - Flash*Freeze (F*F) mode for fabric
- Power as low as 13 mW/Gbps per lane for SerDes devices
- Up to 50% lower total power than competing SoC devices

2.1.4 High-Performance FPGA

- Efficient 4-input look-up tables (LUTs) with carry chains for high-performance and low power
- Up to 236 blocks of dual-port 18 Kbit SRAM (Large SRAM) with 400 MHz synchronous performance (512 x 36, 512 x 32, 1 kbit x 18, 1 kbit x 16, 2 kbit x 9, 2 kbit x 8, 4 kbit x 4, 8 kbit x 2, or 16 kbit x 1)
- Up to 240 blocks of three-port 1 Kbit SRAM with 2 read ports and 1 write port (micro SRAM)
- High-performance DSP signal processing
  - Up to 240 fast mathblocks with 18 x 18 signed multiplication, 17 x 17 unsigned multiplication and 44-bit accumulator

2.1.5 Microcontroller Subsystem

- Hard 166 MHz 32-Bit ARM Cortex-M3 processor
  - 1.25 DMIPS/MHz
  - 8 Kbyte instruction cache
  - Embedded trace macrocell (ETM)
  - Memory protection unit (MPU)
  - Single cycle multiplication, hardware divide
  - JTAG debug (4 wires), serial wire debug (SWD, 2 wires), and serial wire viewer (SWV) interfaces
- 64 KB embedded SRAM (eSRAM)
- Up to 512 KB embedded nonvolatile memory (eNVM)
- Triple speed Ethernet (TSE) 10/100/1000 Mbps MAC
- USB 2.0 high speed on-the-go (OTG) controller with ULPI interface
- CAN controller, 2.0B compliant, conforms to ISO11898-1, 32 transmit and 32 receive buffers
- Two each: SPI, I^2C, and multi-mode UARTs (MMUART) peripherals
- Hardware based watchdog timer
- One general purpose 64-bit (or two 32-bit) timer(s)
- Real-time calendar/counter (RTC)
- DDR bridge (4 port data R/W buffering bridge to DDR memory) with 64-bit AXI interface
- Non-blocking, multi-layer AHB bus matrix allowing multi-master scheme supporting 10 masters and 7 slaves
- Two AHB-Lite/APB3 interfaces to FPGA fabric (master/slave capable)
- Two DMA controllers to offload data transactions from the Cortex-M3 processor
  - 8-channel peripheral DMA (PDMA) for data transfer between MSS peripherals and memory
  - High-performance DMA (HPDMA) for data transfer between eSRAM and DDR memories

2.1.6 Clocking Resources

- Clock sources
  - Up to two high precision 32 KHz to 20 MHz main crystal oscillator
  - 1 MHz embedded RC oscillator
  - 50 MHz embedded RC oscillator
- Up to 8 clock conditioning circuits (CCCs) with up to 8 integrated analog PLLs
  - Output clock with 8 output phases and 45° phase difference (multiply/divide, and delay capabilities)
  - Frequency: input 1 MHz to 200 MHz, output 20 MHz to 400 MHz

2.1.7 High-Speed Serial Interfaces

- Up to 16 SerDes lanes, each supporting
  - XGXS/XAUI extension (to implement a 10 Gbps (XGMII) Ethernet PHY interface)
  - Native EPCS SerDes interface facilitates implementation of serial rapidIO (SRIO) in fabric or an SGMII interface to the Ethernet MAC in MSS
- PCI express (PCIe) endpoint controller
  - ×1, ×2, and ×4 lane PCI express core
  - Up to 2 Kbytes maximum payload size
  - 64-Bit/32-Bit AXI and 64-Bit/32-Bit AHB master and slave interfaces to the application layer

2.1.8 High-Speed Memory Interfaces

- Up to 2 high-speed DDRx memory controllers
  - MSS DDR (MDDR) and fabric DDR (FDDR) controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz DDR clock rate
  - SECDED enable/disable feature
  - Supports various DRAM bus width modes, ×8, ×9, ×16, ×18, ×32, ×36
  - Supports command reordering to optimize memory efficiency
  - Supports data reordering, returning critical word first for each command
- SDRAM support through the SMC_FIC and additional soft SDRAM memory controller

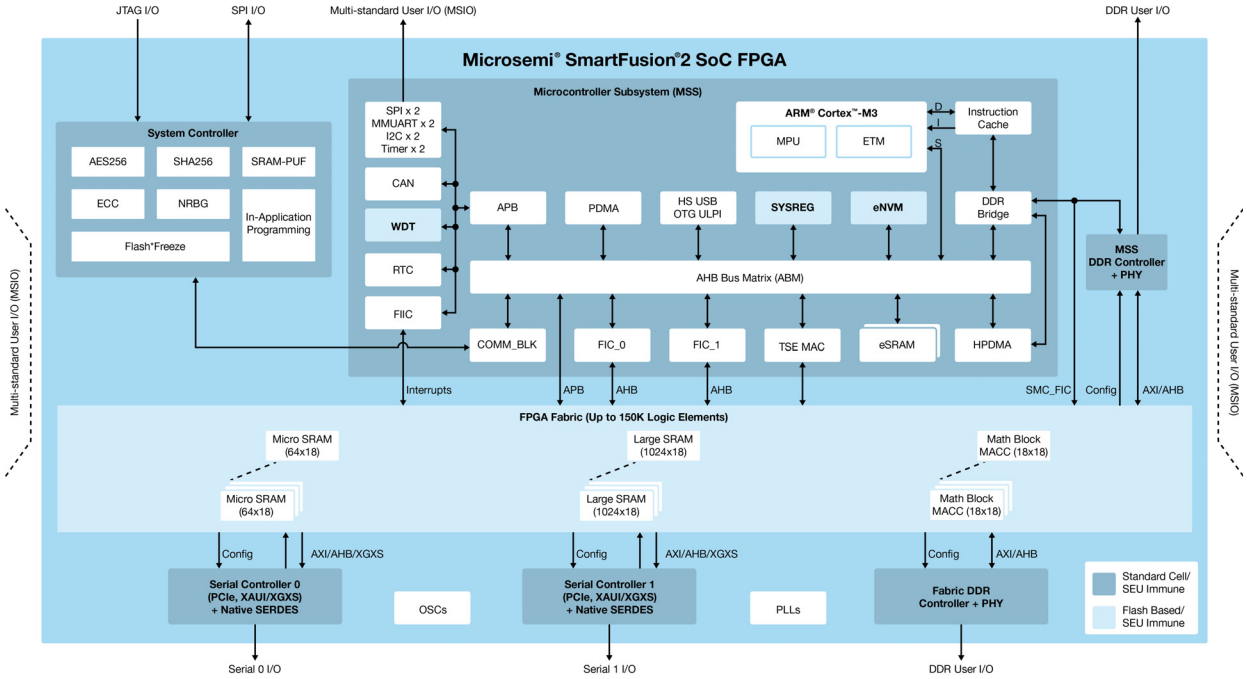
2.1.9 Operating Voltage and I/Os

- 1.2 V core voltage
- Multi-standard user I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO Only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS differential standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
- Market leading number of user I/Os with 5G SerDes

2.2 SmartFusion2 SoC FPGA Block Diagram

The following figure shows the various available blocks in SmartFusion2 such as MSS, system controller, FPGA fabric LEs, and user I/Os.

Figure 1 • **SmartFusion2 Block Diagram**



The following table lists features and devices that are supported in the SmartFusion2 SoC FPGA family.

Table 1 • **SmartFusion2 SoC FPGA Product Family [1, 2]**

Peripherals	Features	M2S005 (S)	M2S010 (S/T/TS)	M2S025 (T/TS)	M2S050 (T/TS)	M2S060 (T/TS)	M2S090 (T/TS)	M2S150 (T/TS)
Logic/DSP	Maximum Logic Elements (4 LUT + DFF)[3]	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	Fabric Interface Controllers	1	1	1	2	1	1	2
	PLLs and CCCs	2	2	6	6	6	6	8
	Data Security	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF
MSS	Cortex-M3 + Instruction Cache	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eNVM (K Bytes)	128	256	256	256	256	512	512
	eSRAM (K Bytes)	64	64	64	64	64	64	64
	eSRAM (K Bytes) Non SECDED	80	80	80	80	80	80	80
	CAN, 10/100/1000 Ethernet, HS USB	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Multi-Mode UART, SPI, I^2C, Timer	2 each	2 each	2 each	2 each	2 each	2 each	2 each
Fabric Memory	LSRAM 18 K Blocks	10	21	31	69	69	109	236
	uSRAM 1 K Blocks	11	22	34	72	72	112	240
	Total RAM (K bits)	191	400	592	1314	1314	2074	4488
High Speed	DDR Controllers (Count x Width)	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes (T)	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3 V)	119	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), and Automotive (T2)	C, I, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M

1. *Feature availability is package dependent.*
2. *Data security features are only available in S and TS devices.*

3. *Total logic may vary based on utilization of DSP and memories in the design. See UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for details.*

2.3 I/Os Per Package

The following tables list the package options and I/Os per package.

Table 2 • **Package Options**

Packages[1]	Pitch (mm)	Length × Width (mm)
FCS(G)325[2]	0.5	11 × 11
VF(G)256[1, 3]	0.8	14 × 14
FCS(G)536[1]	0.5	16 × 16
VF(G)400[1, 2]	0.8	17 × 17
FCV(G)484[1, 2]	0.8	19 × 19
TQ(G)144[1, 4]	0.5	20 × 20
FG(G)484[1]	1.0	23 × 23
FG(G)676[1, 2]	1.0	27 × 27
FG(G)896[1]	1.0	31 × 31
FC(G)1152[1]	1.0	35 × 35

1. All the packages mentioned above are available with lead and lead free.
2. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.
3. Automotive T2 grade devices are only available in the VF(G)256, VF(G)400, FG(G)484, and FG(G)676 packages.
4. The TQ(G)144 package will be available in T2 grade by end of February, 2017.

Table 3 • **I/Os per Package**

Packages		M2S005 (S)	M2S010 (S/T/TS)[1,2]	M2S025 (T/TS)[1]	M2S050 (T/TS)[1]	M2S060 (T/TS)[1]	M2S090 (T/TS)[1, 3, 4]	M2S150 (T/TS)[5]
FCS(G)325	I/Os			180	200	200	180	
	Lanes			2	2	2	4	
VF(G)256	I/Os	161	138	138				
	Lanes		2	2				
FCS(G)536	I/Os							293
	Lanes							4
VF(G)400	I/Os	171	195	207	207	207		
	Lanes		4	4	4	4		
FCV(G)484	I/Os							248
	Lanes							4
TQ(G)144	I/Os	84	84					
	Lanes							
FG(G)484	I/Os	209	233	267	267	267	267	
	Lanes		4	4	4	4	4	
FG(G)676	I/Os					387	425	
	Lanes					4	4	

Table 3 • **I/Os per Package *(continued)***

Packages		M2S005 (S)	M2S010 (S/T/TS)[1,2]	M2S025 (T/TS)[1]	M2S050 (T/TS)[1]	M2S060 (T/TS)[1]	M2S090 (T/TS)[1, 3, 4]	M2S150 (T/TS)[5]
FG(G)896	I/Os				377			
	Lanes				8			
FC(G)1152	I/Os							574
	Lanes							16

1. Military temperature 010/025/050/060/090 are only available in the FG(G)484 package.
2. M2S010S device is only available in TQ(G)144 package.
3. 090 FCSG325 is 11 × 13.5 package dimension.
4. The M2S090 (T/TS) device in the FCS(G)325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microsemi sales office for details.
5. Military temperature 150 devices are only available in the FC(G)1152 package.

Note: Shaded cells indicate that the device packages have vertical migration capability.

The following table lists the package details along with the supported devices and their features.

Table 4 • **Features per Device/Package Combination**

		Features										
Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	ULPI	UTMI	MSIO (3.3 V max)[2]	MSIOD (2.5 V max)[3]	DDRIO (2.5 V max)	Total User I/Os
TQ(G)144[4]	M2S005 (S)			2			1	1	52	9	23	84
	M2S010 (S)			2			1	1	50	11	23	84
VF(G)256[4]	M2S005 (S)			2			1	1	119	12	30	161
	M2S010 (T/TS)	×18[5]		2	2	1	1	1	66	8	64	138
	M2S025 (T/TS)	×18[5]		2	2	1	1	1	66	8	64	138
FCS(G)325[4]	M2S025 (T/TS)	×18[5]		2	2	1	1	1	94	22	64	180
	M2S050 (T/TS)	×18[6]		1	2	1	0	1	90	22	88	200
	M2S060 (T/TS)	×18[5]		2	2	2	1	1	114	22	64	200
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	104	12	64	180
VF(G)400[4]	M2S005 (S)	×18[5]		2			1	1	79	28	64	171
	M2S010 (T/TS)	×18[5]		2	4	1	1	1	99	32	64	195
	M2S025 (T/TS)	×18[5]		2	4	1	1	1	111	32	64	207
	M2S050 (T/TS)	×18[6]		1	4	1	0	1	87	32	88	207
	M2S060 (T/TS)	×18[5]		2	4	2	1	1	111	32	64	207
FCV(G)484[4]	M2S150 (T/TS)	×18[5]	×18[5]	2	4	4[7]	1	1	91	34	123	273
FG(G)484[4]	M2S005 (S)	×18[5]		2			1	1	115	28	66	209
	M2S010 (T/TS)	×18[5]		2	4	1	1	1	123	40	70	233
	M2S025 (T/TS)	×18[5]		2	4	1	1	1	157	40	70	267
	M2S050 (T/TS)	×18[6]		1	4	1	0	1	105	40	122	267
	M2S060 (T/TS)	×18[5]		2	4	2	1	1	157	40	70	267
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	157	40	70	267

Table 4 • **Features per Device/Package Combination *(continued)***

		Features										
Package	**Devices**	**MDDR**	**FDDR**	**Crystal Oscillators**	**5G SerDes Lanes[1]**	**PCIe Endpoints**	**ULPI**	**UTMI**	**MSIO (3.3 V max)[2]**	**MSIOD (2.5 V max)[3]**	**DDRIO (2.5 V max)**	**Total User I/Os**
FCS(G)536[4]	M2S150 (T/TS)	×18[5]	×18[5]	2	4	4[7]	1	1	151	16	126	293
FG(G)676[4]	M2S060 (T/TS)	×18[5]		2	4	2	1	1	271	40	76	387
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	309	40	76	425
FG(G)896 [4, 8]	M2S050 (T/TS)	×36[9]	×36[9]	1	8	2	1	1	139	62	176	377
FC(G)1152[4]	M2S150 (T/TS)	×36[10]	×36[10]	2	16	4	1	1	292	106	176	574

1. *Maximum SerDes rate for Military temperature devices is 3.125 Gbps.*
2. *Number of differential MSIO is Number of MSIOs/2 for even and (Number of MSIOs-1)/2 for odd MSIO supports LVDS 3.3/2.5 standard.*
3. *Number of differential MSIOD is Number of MSIODs/2 for even and (Number of MSIODs-1)/2 for odd MSIOD supports only LVDS 2.5 standard.*
4. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
5. *DDR supports ×18, ×16, ×9, and ×8 modes.*
6. *DDR supports ×18 and ×16 modes.*
7. *4 PCIe Gen1/Gen2 endpoints ×1 lane configuration.*
8. *DDR3 is non-compliant. Call technical support for details.*
9. *DDR supports ×36, ×32, ×18, and ×16 modes.*
10. *DDR supports ×36, ×32, ×18, ×16, ×9, and ×8 modes.*

The following table lists the available programming interfaces.

Table 5 • **Available Programming Interfaces**

Package	**Devices**	**JTAG**	**SPI_0**	**Flash_GOLDEN_N**	**System Controller SPI Port**
TQ(G)144[1]	M2S005 (S)	Yes	Yes	No	No
	M2S010 (S)	Yes	Yes	No	No
VF(G)256[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	No
	M2S025 (T/TS)	Yes	Yes	Yes	No
FCS(G)325[1]	M2S025 (T/TS)	Yes	Yes	No	No
	M2S050 (T/TS)	Yes	Yes	No	No
	M2S060 (T/TS)	Yes	Yes	No	No
	M2S090 (T/TS)	Yes	Yes	No	No
VF(G)400[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	Yes
	M2S025 (T/TS)	Yes	Yes	Yes	Yes
	M2S050 (T/TS)	Yes	Yes	Yes	Yes
	M2S060 (T/TS)	Yes	Yes	Yes	Yes
FCV(G)484[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes

Table 5 • **Available Programming Interfaces *(continued)***

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
FG(G)484[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	Yes
	M2S025 (T/TS)	Yes	Yes	Yes	Yes
	M2S050 (T/TS)	Yes	Yes	Yes	Yes
	M2S060 (T/TS)	Yes	Yes	Yes	Yes
	M2S090 (T/TS)	Yes	Yes	Yes	Yes
FCS(G)536[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)676[1]	M2S060 (T/TS)	Yes	Yes	Yes	Yes
	M2S090 (T/TS)	Yes	Yes	Yes	Yes
FG(G)896[1]	M2S050 (T/TS)	Yes	No	Yes	Yes
FC(G)1152[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

The following table lists the programming modes that are required for chip resources.

Table 6 • **Chip Resources Needed for Programming Modes**

Programming Mode	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
External FlashPro4/5	Yes	No	No	No
External uP – JTAG slave	Yes	No	No	No
External uP – SPI Slave	No	No	No	Yes
Auto Programming	No	Yes	Yes	No
2-Step IAP	No	Yes	No	No
Programming Recovery	No	Yes	No	No

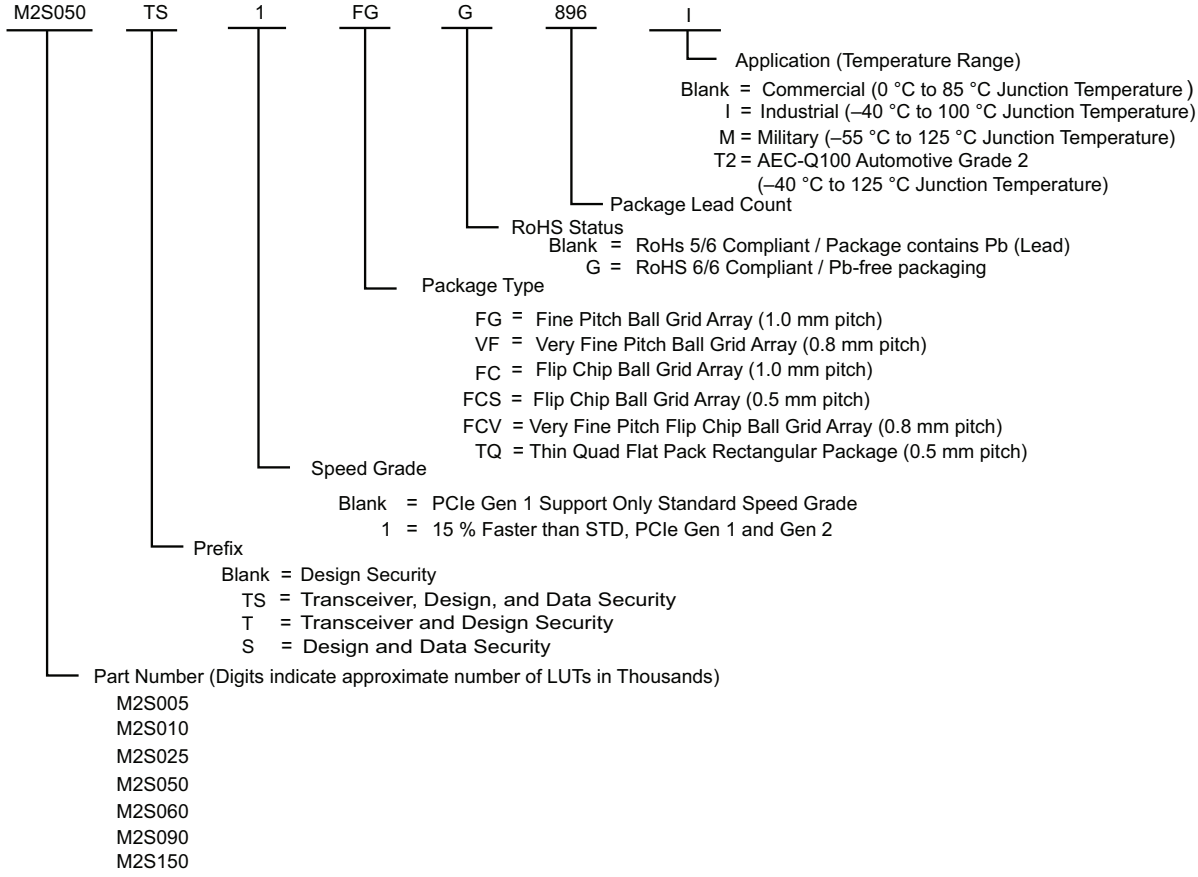
2.4 Acronyms

AES	Advanced Encryption Standard
AHB	advanced high-performance bus
APB	advanced peripheral bus
AXI	advanced eXtensible interface
COMM_BLK	communication block
DDR	double data rate
DPA	differential power analysis
ECC	elliptic curve cryptography
EDAC	error detection and correction
ETM	embedded trace macrocell
FDDR	DDR2/3 controller in FPGA fabric
FIC	fabric interface controller
FIIC	fabric interface interrupt controller
HS USB OTG	high-speed USB 2.0 on-the-go
IAP	in-application programming
MACC	multiply accumulate
MDDR	DDR2/3 controller in MSS
MMUART	multi-mode UART
MPU	memory protection unit
MSIO	multi-standard I/O
MSS	microcontroller subsystem
PUF	physically unclonable function
SECDED	single error correct double error detect
SEU	single event upset
SHA	Secure Hashing Algorithm
SMC_FIC	soft memory controller
TSE	triple speed Ethernet (10/100/1000 Mbps)
ULPI	UTMI + low pin interface
UTMI	USB 2.0 transceiver macrocell interface
WDT	watchdog timer
XAUI	10-gigabit attachment unit interface
XGMII	10-gigabit media independent interface
XGXS	XGMII extended sublayer

2.5 SmartFusion2 Ordering Information

The M2S050 device is taken as an example and is explained each part of the device and its purpose.

Figure 2 • **M2S050 Ordering Information**



Note: M2S005 devices are not available with transceivers or in the military temperature grade.

Note: Automotive grade devices are available with S and TS.

2.6 SmartFusion2 Commercial and Industrial Temperature Grade Devices

The following table lists SmartFusion2 devices and device ranges that are supported without data security.

Table 7 • **SmartFusion2 Devices without Data Security (All Speed Grades, C, and I Temperature)[1]**

M2S	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005										
010		T		T			T			
025	T	T		T			T			
050	T			T			T		T	
060	T			T			T	T		
090	T						T	T		
150			T		T					T

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

Note: T indicates that the devices are available with Transceiver. Example ordering code: M2S025T-FCSG325

Note: Shaded cells indicate that the devices are available without Transceiver. Example ordering code: M2S025-FCSG325

The following table lists SmartFusion2 devices and device ranges that are supported with data security.

Table 8 • **SmartFusion2 Data Security S Devices (All Speed Grades, C, and I Temperature)[1]**

M2S	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005		S		S		S	S			
010		TS		TS		S	TS			
025	TS	TS		TS			TS			
050	TS			TS			TS		TS	
060	TS			TS			TS	TS		
090	TS						TS	TS		
150			TS		TS					TS

1. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

Note: S indicates that the devices are available with Data Security.
Example ordering code: M2S005S-VFG400.

Note: TS indicates that the devices are available with Transceiver and Data Security.
Example ordering code: M2S025TS-FCSG325.

2.6.1 SmartFusion2 Military Temperature Grade Devices

Following are the SmartFusion2 military temperature grade devices:

- M2S010 (T/TS)-1FG(G)484M
- M2S025 (T/TS)-1FG(G)484M
- M2S050 (T/TS)-1FG(G)484M
- M2S060 (T/TS)-1FG(G)484M
- M2S090 (T/TS)-1FG(G)484M
- M2S150 (T/TS)-1FC(G)1152M

Note: Gold Wire bonds are available for the FG484 package by appending X399 to the part number when ordering, for example: M2S090 (T/TS)-1FG484MX399.

Note: All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

2.7 SmartFusion2 Device Status

See *DS0128: IGLOO2 and SmartFusion2 Datasheet* for device status.

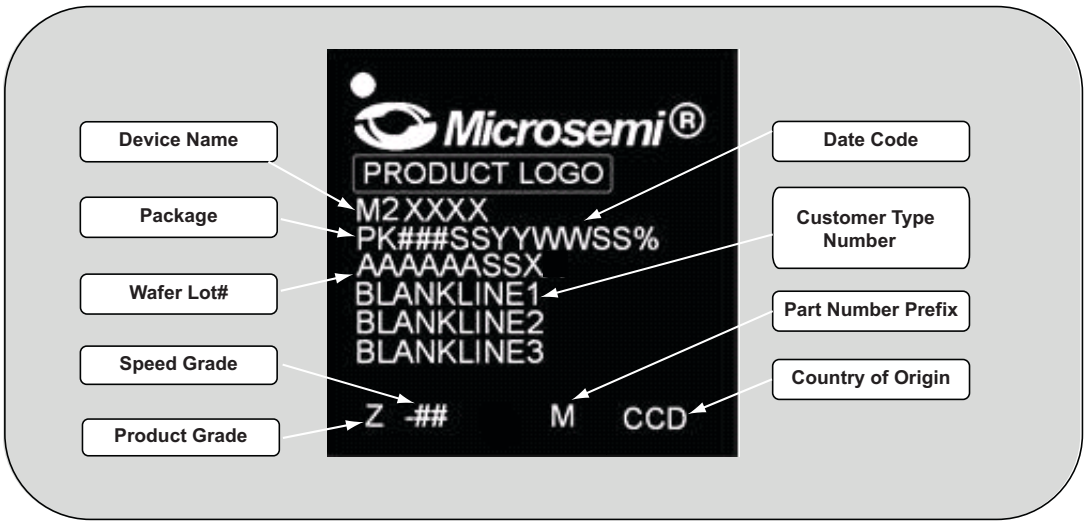
2.8 SmartFusion2 Datasheet and Pin Descriptions

The datasheet and pin descriptions are published separately:

- *DS0128: IGLOO2 and SmartFusion2 Datasheet*
- *DS0134: SmartFusion2 and IGLOO2 Automotive Grade 2 Datasheet*
- *PB0136: Automotive Grade 2 SmartFusion2 SoC FPGAs Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions Datasheet*

2.9 Marking Specification Details

Microsemi normally topside marks the full ordering part number on each device. The following figure provides the details for each character code present on Microsemi's SmartFusion2 SoC FPGA devices.



2.9.1 Description

- Device Name (M2XXXX): M2S for SmartFusion2 Devices
  - Example: M2S050TS
- Package (PK###): Available Package as below
  - *PK: Package code*[1]*:*
  - FG(G): Fine Pitch BGA, 1.00 mm pitch
  - FC(G): Flip Chip Fine Pitch BGA with Metal LID on top, 1.00 mm pitch
  - FCV(G): Flip Chip Very Fine Pitch BGA with Metal LID on top, 0.8 mm pitch
  - FCS(G): Flip Chip Ultra Fine Pitch BGA with Metal LID on top, 0.5 mm pitch
  - VF(G): Very Fine Pitch BGA, 0.8 mm pitch
  - TQ(G): Ultra Fine Pitch Thin Quad Flat Pack Package, 0.5 mm pitch
  - ###: Number of Pins: Can be three or four digits. For example,144, 256, or 1152
- Wafer Lot (AAAAAASSX): Microsemi Wafer lot #
  - AAAAAA: Wafer lot number
  - X: One digit die revision code
  - SS: Two blank spaces
- Speed Grade (-##): Speed Binning Number
  - Blank: Standard speed grade
  - -1: -1 Speed grade
- Product grade (Z): Product Grade; assigned as follows
  - Blank/C: Commercial
  - ES: Engineering Samples
  - I: Industrial
  - M: Military Temperature
  - PP: Pre Production
  - T2: AEC-Q100 Automotive Grade 2
- Date Code (YYWWSS%): Assembly Date Code
  - YY: Last two digits for seal year
  - WW: Work week the part was sealed
  - SS: Two blank spaces
  - %: Can be digital number or character for new product
- Customer Type Number: As specified on lot traveler
  - GW: Gold Wire bond
- Part number Prefix: Part number prefix, assigned as below
  - Blank: Design Security
  - T: Transceivers and Design Security
  - S: Design and Data Security
  - TS: Transceiver, Design, and Data Security
- Country of Origin (CCD): Assembly house country location
  - *Country name: Country Code*
  - China: CHN
  - Hong Kong: HKG
  - Japan: JPN
  - Korea, South: KOR
  - Philippines: PHL
  - Taiwan: TWN
  - Singapore: SGP
  - United States: USA
  - Malaysia: MYS

1. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

3 SmartFusion2 Device Family Overview

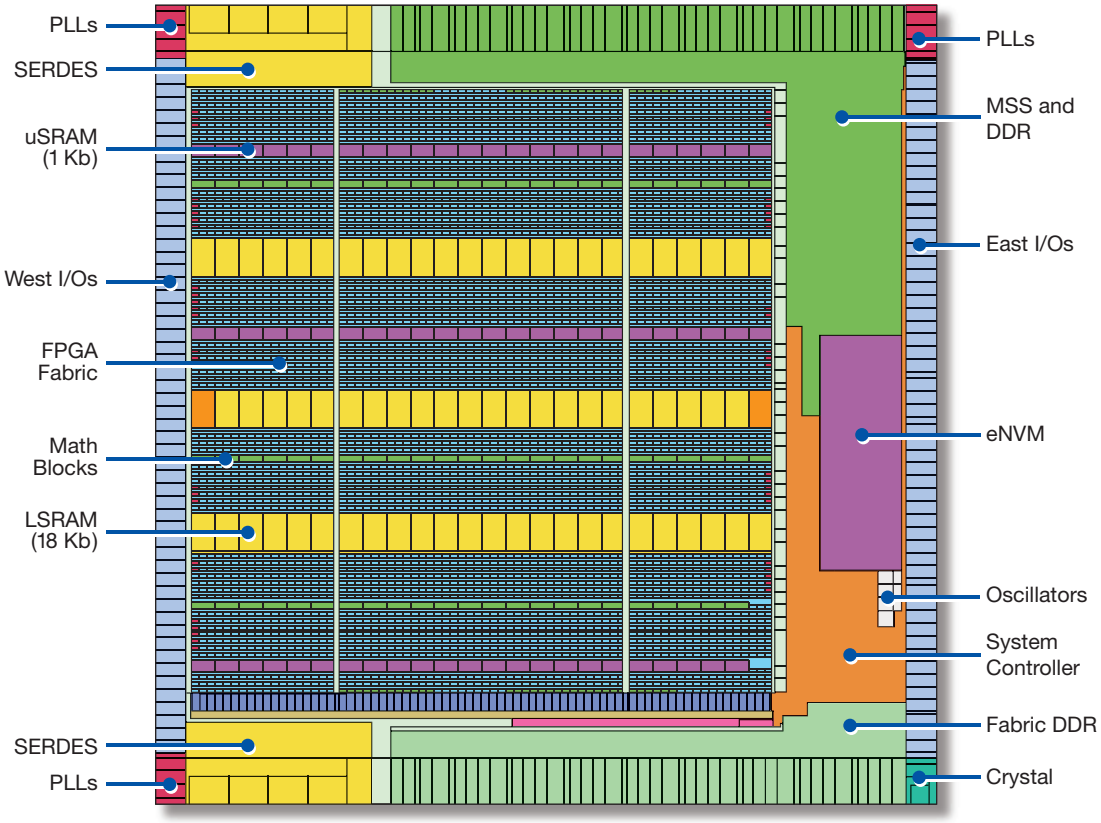
Microsemi's SmartFusion2 SoC FPGAs integrate the fourth generation flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communication interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution.

SmartFusion2 FPGAs offer up to 3.6X the gate density, up to 2X the performance of previous flash-based FPGA families, and include multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high-speed USB. High-speed serial interfaces enable PCIe, XAUI/XGXS plus native SerDes communication while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

3.1 SmartFusion2 Chip Layout

The following figure shows the SmartFusion2 chip layout and its various parts highlighted.

Figure 3 • **SmartFusion2 Chip Layout**



3.2 Reliability

SmartFusion2 flash-based fabric has zero FIT configuration rate due to its SEU immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, SmartFusion2 devices add reliability to many other aspects of the device. Single error correct double error detect (SECDED) protection is implemented on the Cortex-M3 embedded scratch pad memory, Ethernet, CAN, and USB buffers, and is optional on the DDR memory controllers. This means that if a one-bit error is detected, the error is corrected automatically. If errors of more than

one bit are detected, they are not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in DDR bridges (MSS, MDDR, and FDDR), instruction cache and MMUART, SPI, and PCIe FIFOs.

3.3 Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the SmartFusion2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 SoC FPGAs add many unique design, data security features, and use models new to the PLD industry.

3.3.1 Design Security vs. Data Security

When classifying the security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

3.3.2 Design Security

Design security protects the intent of the owner of the design such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following are the main design security features supported.

Table 9 • **Design Security Features**

Features (all devices)	M2S005, M2S010, M2S025, and M2S050	M2S060, M2S090, and M2S150
Software memory protection unit (MPU)	•	•
FlashLock® passcode security (256-bit)	•	•
Flexible security settings using flash lock-bits	•	•
Encrypted/authenticated design key loading	•	•
Symmetric key design security (256-bit)	•	•
Design key verification protocol	•	•
Encrypted/authenticated configuration loading	•	•
Certificate-of-conformance (C-of-C)	•	•
Back-tracking prevention (also known as, versioning)	•	•
Device certificate(s) (anti-counterfeiting)	•	•
Support for configuration variations	•	•
Fabric NVM and eNVM integrity tests	•	•
Information services (S/N, Cert., USERCODE, and others)	•	•