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Military Grade IGLOO2 FPGA and SmartFusion2 SoC FPGA

DS0120 Datasheet

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IGLOO2 and SmartFusion2 SoC FPGA Military Grade AC/DC Electrical Characteristics

1. Introduction

Microsemi®'s military grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

For more information on device status, refer to the "Datasheet Categories".

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	Status
010T	Production
025T	Production
050T	Production
060T	Preliminary
090T	Production
150T	Production
Data Security Device Densities	**Status**
010TS	Production
025TS	Production
050TS	Production
060TS	Preliminary
090TS	Production
150TS	Production

3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

- PB0121: IGLOO2 Product Brief
- DS0124: IGLOO2 Pin Descriptions
- PB0115: SmartFusion2 SoC FPGA Product Brief
- DS0115: SmartFusion2 Pin Descriptions

4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

Table 2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	–0.3	1.32	V	–
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	–0.3	3.63	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	–0.3	3.63	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	–0.3	3.63	V	–
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	–0.3	2.75	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	–0.3	1.32	V	–
SERDES_[01]_VDD	PCIe®/PCS power supply	–0.3	1.32	V	–
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	–0.3	3.63	V	–
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	–0.3	2.75	V	–
VI	I/O Input voltage for MSIO I/O Bank	–0.3	3.63	V	–
	I/O Input voltage for MSIOD/DDRIO I/O Bank	–0.3	2.75	V	–
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	–0.3	3.63	V	–

Table 2 • Absolute Maximum Ratings (continued)

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
T_{STG}	Storage temperature	–65	150	°C	*
T_J	Junction temperature	–	135	°C	–

*Note: * For flash programming and retention maximum limits, refer to Table 4 on page 14. For recommended operating conditions, refer to Table 3.*

Table 3 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Tj	Operating Junction Temperature	Military	-55	25	125	°C	–
	Programming Junction Temperature	–	0	25	85	°C	–
		–	-40	25	100	°C	1
VDD	DC core supply voltage. Must always power this pin.	–	1.14	1.2	1.26	V	–
VPP	Power Supply for Charge Pumps (for Normal Operation and Programming) for 010, 025, 050 Devices	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
	Power Supply for Charge Pumps (for Normal Operation and Programming) for 090, and 150 devices	3.3 V Range	3.15	3.3	3.45	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Table 3 • **Recommended Operating Conditions (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V Range	2.375	2.5	2.625	V	2
		3.3 V Range	3.15	3.3	3.45	V	2
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lanes 0-3. It is a +2.5 V SERDES internal PLL supply.	–	2.375	2.5	2.625	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. It is a +1.2 V SERDES PMA supply.	–	1.14	1.2	1.26	V	–
SERDES_[01]_VDD	PCIe/PCS Power supply	–	1.14	1.2	1.26	V	–
VDDIx	1.2 V DC supply voltage	–	1.14	1.2	1.26	V	–
	1.5 V DC supply voltage	–	1.425	1.5	1.575	V	–
	1.8 V DC supply voltage	–	1.71	1.8	1.89	V	–
	2.5 V DC supply voltage	–	2.375	2.5	2.625	V	–
	3.3 V DC supply voltage	–	3.15	3.3	3.45	V	–
	LVDS differential I/O	–	2.375	2.5	3.45	V	–
	BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O	–	2.375	2.5	2.625	V	–
	LVPECL differential I/O	–	3.15	3.3	3.45	V	–
VREFx	Reference Voltage Supply for FDDR (Bank0) and MDDR(Bank5)	–	0.49 × VDDIx	0.5 × VDDIx	0.51 × VDDIx	V	–

Table 3 • Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Notes:
1. *Programming at this temperature range is available only with VPP in 3.3 V Range*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 4 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)	Note
Military	FPGA	Min T_J = 0°C Max T_J = 85°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	–
		Min T_J = -40°C Max T_J = 100°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	*

*Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range*

Table 5 • Embedded Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Military	Embedded flash	Min T_J = -55°C Max T_J = 125°C	Min T_J = -55°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (Tstg)	Retention
Military	Min T_J = -55°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3. Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA}			θ_{JB}	θ_{JC}	**Units**
	Still Air	**1.0 m/s**	**2.5 m/s**			
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050-FG484 package at Military temperature and in still air, where:

θ_{JA} = 15.29°C/W (taken from Table 7 on page 15)

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{15.29°C/W} = 0.981\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

4.3.3 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

4.3.4 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

5. Power Consumption

5.1 Quiescent Supply Current

Table 8 • **Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
FPGA Core	On	Off	–
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	–
MDDR_PLL_VDDA CCC_XX[01]_PLL_VDDA PLL0_PLL1_MDDR_VDDA FDDR_PLL_VDDA	0 V	0 V	–
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	–
MSSDDR CLK	32 kHz	32 kHz	–
RAM	On	Sleep state	–
HPMS Controller	50 MHz	50 MHz	–
50 MHz Oscillator (enable/disable)	Enabled	Disabled	–
1 MHz Oscillator (enable/disable)	Disabled	Disabled	–
Crystal Oscillator (enable/disable)	Disabled	Disabled	–

Notes:

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.*

Table 9 • **SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process**

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	
IDC1	Non-Flash*Freeze	Typical (T_J = 25°C)	6.9	8.9	13.1	15.4	27.5	mA
		Military (T_J = 125°C)	73.0	106.4	180.9	217.5	390.5	mA
IDC2	Flash*Freeze	Typical (T_J = 25°C)	2.6	3.7	5.1	5.1	8.9	mA
		Military (T_J = 125°C)	55.6	74.2	98.5	99.5	161.0	mA

Table 10 • **SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process**

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	
IDC1	Non-Flash*Freeze	Military (T_J = 125°C)	151.5	227.4	358.9	443.1	660.4	mA
IDC2	Flash*Freeze	Military (T_J = 125°C)	127.2	144.2	174.6	195.0	236.3	mA

5.2 Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 11 • **Currents During Program Cycle, 0°C < = T_J <= 85°C, Typical Process**

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	42	52	mA	–
VPP	3.46	11	6	10	12	12	mA	–
VPPNVM	3.46	2	2	3	3	–	mA	*
VDDI	2.62	16	17	1	12	81	mA	**
	3.46	31	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–

Notes:

** VPP and VPPNVM are internally shorted.*

*** The current for 050 represents JTAG I/O Bank only.*

Table 12 • **Currents During Verify Cycle, 0°C <= T_J <= 85°C, Typical Process**

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	41	51	mA	–
VPP	3.46	5	3	15	11	12	mA	–
VPPNVM	3.46	0	0	1	1	–	mA	*
VDDI	2.62	16	17	1	11	81	mA	**
	3.46	32	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–

Notes:

** VPP and VPPNVM are internally shorted.*

*** The current for 050 represents JTAG I/O Bank only.*

Table 13 • **Inrush Currents at Power up, –55°C <= T_J <=125°C, Typical Process**

Power Supplies	Voltage (V)	010	025	050	090	150	Units
VDD	1.26	53	78	57	98	140	mA
VPP	3.46	57	50	180	36	51	mA

Table 13 • **Inrush Currents at Power up, –55°C <= T_J <=125°C, Typical Process**

VDDI	2.62	141	161	187	283	404	mA
Number of banks		8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays (Normalized to T_J = 125°C, Worst-Case VDD = 1.14 V)**

Core Voltage VDD (V)	**Junction Temperature (°C)**							
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

7. Timing Model

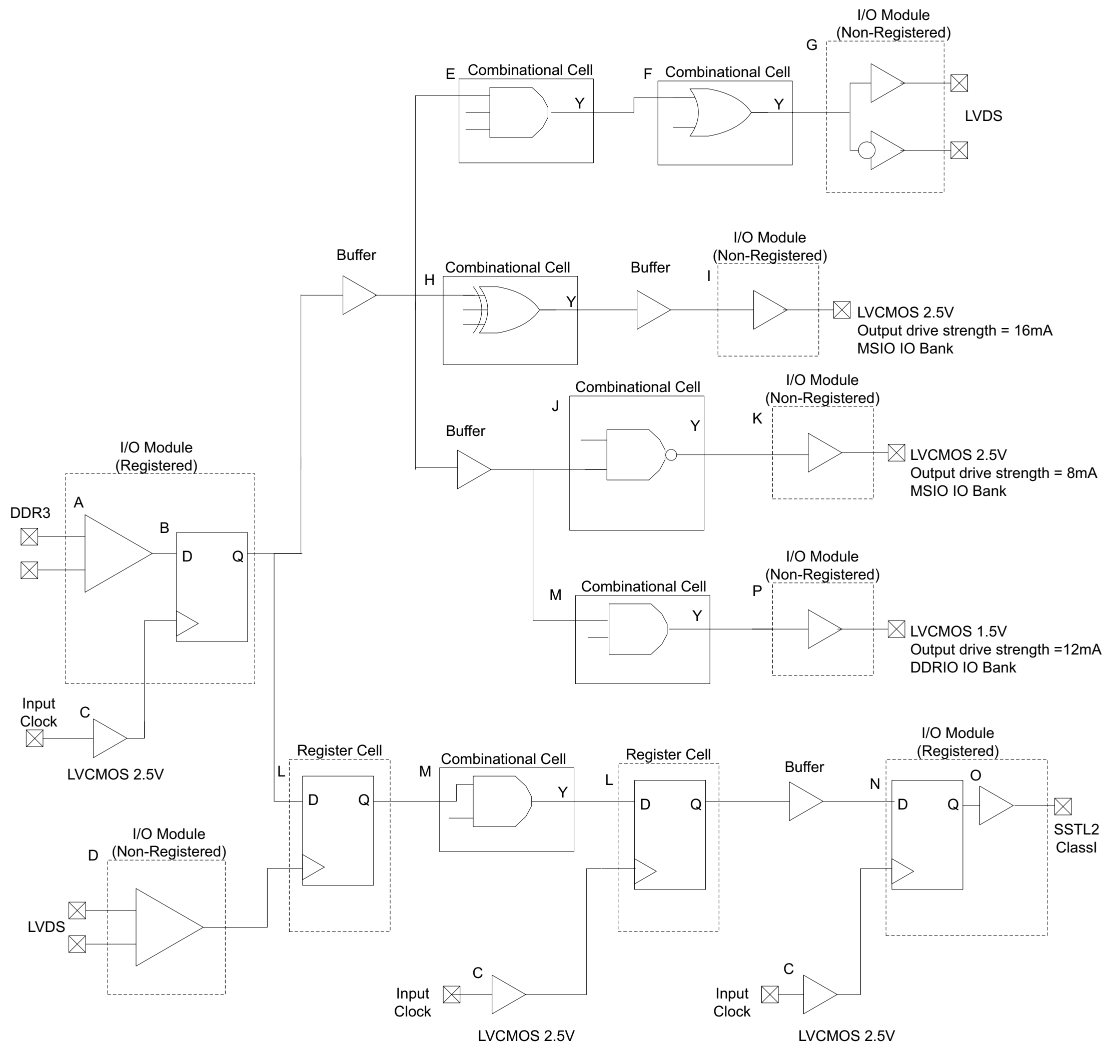

***Figure 1* • Timing Model**

Table 15 • **Timing Model Parameters**

Index	Parameter	Description	Speed Grade –1	Units	Notes
A	t_{PY}	Propagation Delay of DDR3 Receiver	1.672	ns	Refer to page 52 for more information
B	t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.165	ns	Refer to page 67 for more information
	t_{ISUD}	Setup Time of the Input Data Register	0.369	ns	Refer to page 67 for more information
C	t_{RCKH}	Input High Delay for Global Clock	1.55	ns	Refer to page 78 for more information
	t_{RCKL}	Input Low Delay for Global Clock	0.861	ns	Refer to page 78 for more information
D	t_{PY}	Input Propagation Delay of LVDS Receiver	3.061	ns	Refer to page 58 for more information
E	t_{DP}	Propagation Delay of a three input AND Gate	0.217	ns	Refer to page 76 for more information
F	t_{DP}	Propagation Delay of a OR Gate	0.17	ns	Refer to page 76 for more information
G	t_{DP}	Propagation Delay of a LVDS Transmitter	2.299	ns	Refer to page 58 for more information
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.236	ns	Refer to page 76 for more information
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16mA on the MSIO Bank	2.717	ns	Refer to page 31 for more information
J	t_{DP}	Propagation Delay of a two input NAND Gate	0.17	ns	Refer to page 76 for more information
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8mA on the MSIO Bank	2.594	ns	Refer to page 31 for more information
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.112	ns	Refer to page 67 for more information
	t_{SUD}	Setup Time of the Data Register	0.262	ns	Refer to page 67 for more information
M	t_{DP}	Propagation Delay of a two input AND gate	0.17	ns	Refer to page 76 for more information
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.272	ns	Refer to page 69 for more information
	t_{OSUD}	Setup Time of the Output Data Register	0.196	ns	Refer to page 69 for more information

Table 15 • **Timing Model Parameters (continued)**

Index	Parameter	Description	Speed Grade –1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 47 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 38 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*

8.1 Input Buffer and AC Loading

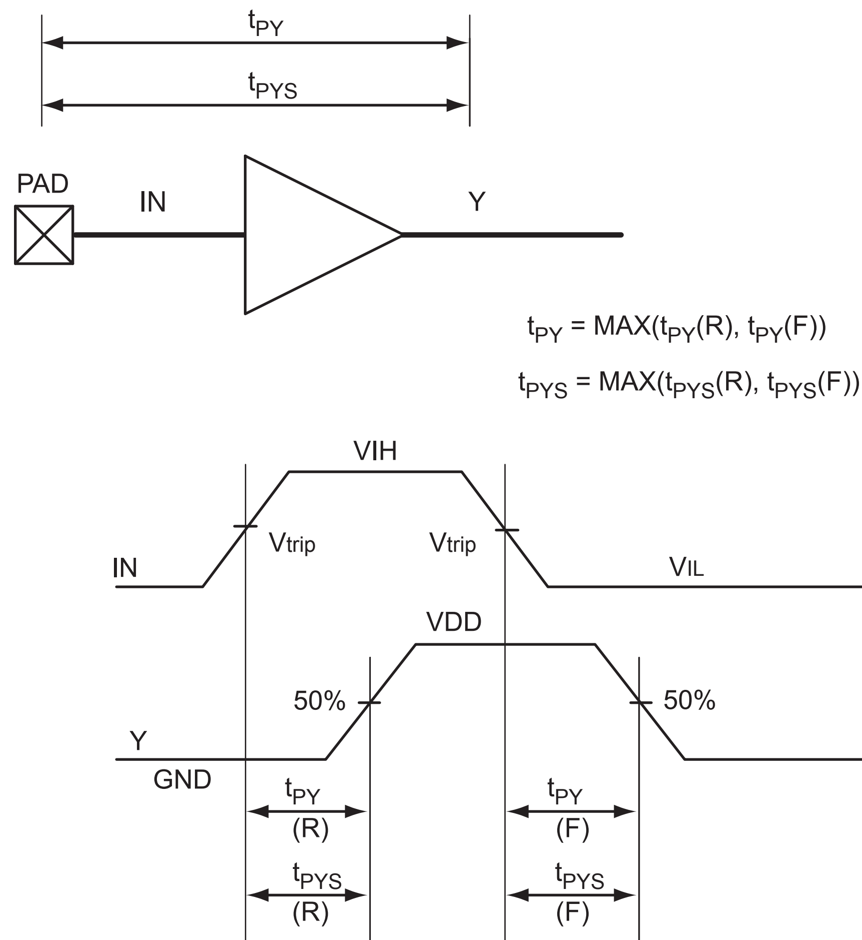

Figure 2 • **Input Buffer AC Loading**

8.2. Output Buffer and AC Loading

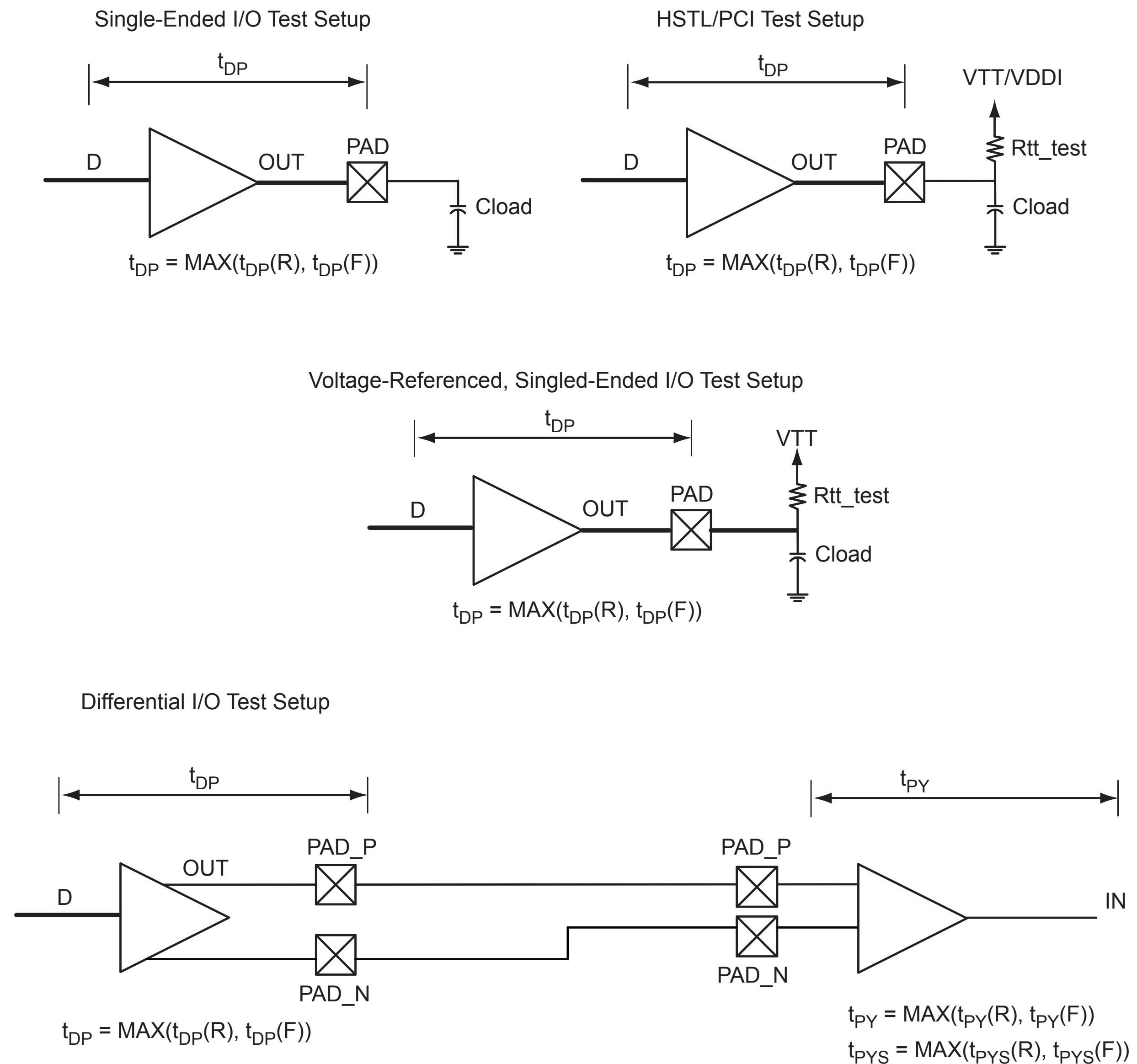

***Figure 3* • Output Buffer AC Loading**

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

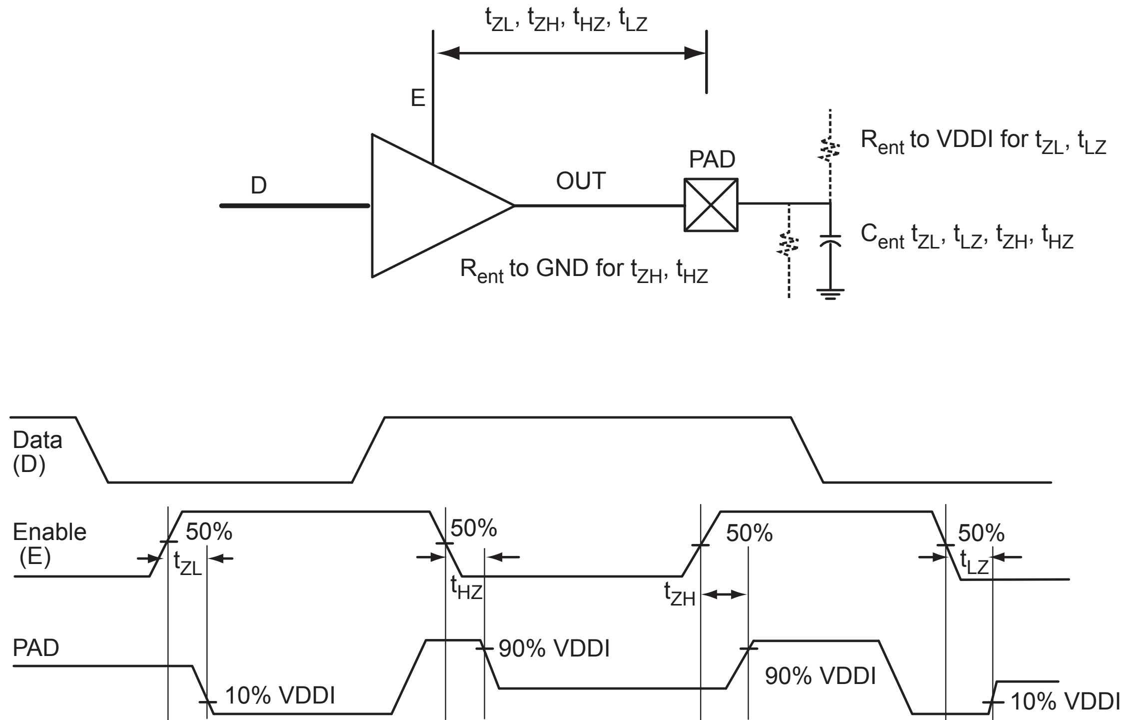

***Figure 4* • Tristate Buffer for Enable Path Test Point**

8.4 I/O Speeds

Table 16 • **Maximum Data Rate Summary for Worst-Case Military Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVCMOS 3.3 V	540	–	–	Mbps
LVCMOS 2.5 V	360	370	360	Mbps
LVCMOS 1.8 V	260	360	360	Mbps
LVCMOS 1.5 V	140	190	210	Mbps
LVCMOS 1.2 V	100	140	180	Mbps
LPDDR – LVCMOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RSDS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps