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UG0557
User Guide
SmartFusion2 SoC FPGA Advanced Development Kit

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

PCIe edge card ribbon cable was removed from the kit contents. For more information, see Kit Contents, page 2.

1.2 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Throughout the document, the part number was updated from M2S150-ADV-DEV-KIT-ES to M2S150-ADV-DEV-KIT (SAR 66855).
- Throughout the document, the device number was updated from M2S150T-1FCG1152ES to M2S150TS-1FCG1152 (SAR 66855).
- The MTD files link was updated. For more information, see Manufacturing Test, page 75 (SAR 60671 and 68260).
- Pin details were updated. For more information, see Validating Power Supply, page 75 (SAR 61171).
- Information about FMC connectors was updated. For more information, see FMC Connectors, page 25 (SAR 67950).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The RoHS-compliant SmartFusion®2 SoC FPGA Advanced Development Kit (M2S150-ADV-DEV-KIT) enables you to develop the following.

- Microprocessor applications
- Embedded ARM® Cortex®-M3 processor-based systems
- Motor control applications
- Industrial automation applications
- High-speed serial I/O applications
- Universal serial bus (USB) applications (with OTG support)

2.1 Kit Contents

The following table lists the contents of the SmartFusion2 Advanced Development Kit.

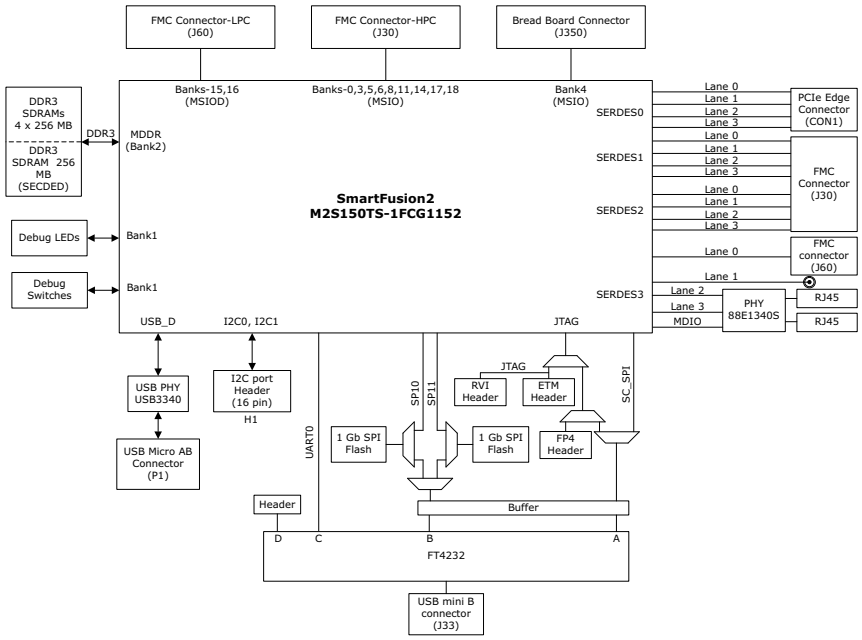
Table 1 • **Kit Contents**

Item	Quantity
SmartFusion2 Advanced Development Board with 150K LE M2S150TS-1FCG1152 device	1
USB A to Micro B cable	1
USB Micro A to A cable	1
USB A to Mini B cable	1
12 V/5 A power adapter	1

2.2 Block Diagram

The following figure is the block diagram of the SmartFusion2 Advanced Development Kit.

Figure 1 • **SmartFusion2 Advanced Development Kit Block Diagram**



2.3 Web Resources

More information about the SmartFusion2 Advanced Development Kit is available at *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2/smartfusion2-advanced-development-kit#overview*.

2.4 Board Description

M2S150-ADV-DEV-KIT offers a full-featured development board for SmartFusion2 SoC FPGAs. The board integrates the following features on a single chip.

- Reliable flash-based FPGA fabric
- 166 MHz ARM Cortex-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

The SmartFusion2 Advanced Development Board has several standard interfaces including:

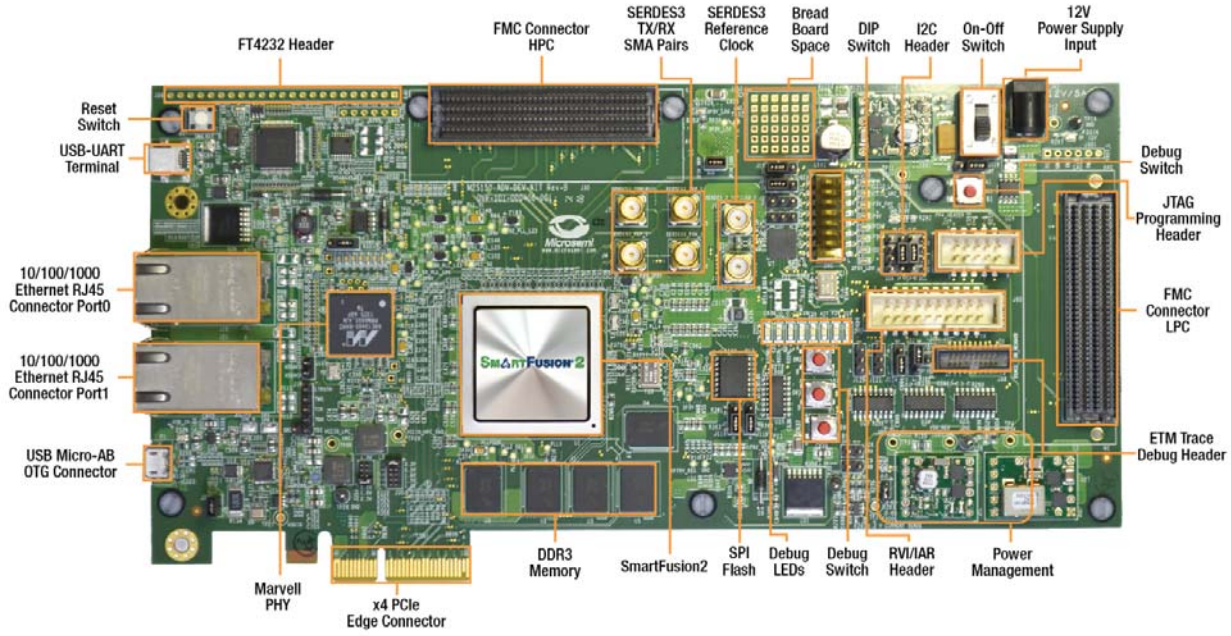
- USB
- x4 serializer and deserializer (SerDes)
- DDR3 memory
- JTAG
- Inter-integrated circuit (I2C)
- Serial peripheral interface (SPI)
- Universal asynchronous receiver/transmitter (UART)
- Dual gigabit Ethernet

The SmartFusion2 memory management system supports 1 GB (4 × 256 MB) on-board DDR3 memory for data storage, 256 MB DDR3 memory for error detection and correction (ECC-SECDED), and 2 GB (2 × 1 GB) memory for SPI flash devices. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60). Unused MSIOD signals are routed to the J60 connector from the SmartFusion2 device. Unused MSIO signals are routed to another on-board FMC connector—HPC (J30), and although the bread board connector (J350) space available for Bank 4 (MSIO) pins.

The SmartFusion2 device can be programmed through embedded FlashPro5. The Advanced Development Kit has the current measurement feature (see Current Measurement, page 11).

The following figure is a snapshot of the SmartFusion2 Advanced Development Board with its engineering silicon.

Figure 2 • **SmartFusion2 Advanced Development Board**



2.5 Board Key Components

The following table lists key components of the SmartFusion2 Advanced Development Board.

Table 2 • **SmartFusion2 Advanced Development Board Components**

Name	Description
SmartFusion2 FPGA	M2S150TS-1FCG1152 FPGA with a hard Cortex-M3 processor.
DDR3 synchronous dynamic random access memory (SDRAM)	4 × 256 MB (256 MB Micron DDR3 memories MT41K256M8DA-125 IT:K) for storing data, and 256 MB (1 × 256 MB Micron DDR3 memory MT41K256M8DA-125 IT:K) for storing ECC bits.
SPI flash	A 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to SPI port 0 of the SmartFusion2 microcontroller subsystem (MSS), and another 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to the SmartFusion2 fabric.
Ethernet	Two RJ45 connectors (Ethernet jacks with built-in magnetics) interfacing with a Marvell 10/100/1000 BASE-T physical layer (PHY) chip—88E1304S—in Serial Gigabit Media Independent Interface (SGMII) mode. The Marvell PHY device, in turn, interfaces with the Ethernet port of the SmartFusion2 MSS (on-chip MAC and external PHY).
RVI header	RVI header for application programming and debugging using Keil ULINK or IAR J-Link.
Embedded FlashPro5	Embedded FlashPro5 for programming and debugging the SmartFusion2 FPGA using Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J33) to program the external SPI flash. An FTDI chip is also used to change the JTAG_SEL signal (*high* or *low*) remotely for switching between the RVI header and JTAG mode.
Embedded Trace Macro (ETM) cell header	ETM header for debugging.

Table 2 • **SmartFusion2 Advanced Development Board Components *(continued)***

PCI Express (PCIe) edge connector	PCIe edge connector with four lanes.
Light-emitting diodes (LEDs)	Eight active-high LEDs connected to some of the user I/Os for debugging.
Push-button reset	Push-button system reset for the SmartFusion2 device.
Push-button switches	Four push-button switches for testing and navigation.
FMC HPC connector (J30)	High pin count FMC header to connect the external daughter boards. Connector array socket 400 pins (40 × 10), 1.27 mm pitch. Unused MSIO pins routed from the SmartFusion2 device to the J30 connector.
FMC LPC connector (J60)	Low pin count FMC header to connect the external daughter boards. Connector array socket 160 pins (40 × 4), 1.27 mm. Unused MSIOD pins routed from the SmartFusion2 device to the J60 connector.
USB interface	USB Micro-AB connector, interfacing with the high speed USB2.0 ULPI transceiver chip USB3320, which, in turn, interfaces with USB-D port of the SmartFusion2 MSS.
DS1818 3.3V EconoReset	A simple three-pin voltage monitor and power-on reset that holds reset for 150 ms for stabilization after power returns to tolerance.
OSC-100	100 MHz clock oscillator with differential output.
OSC-125	125 MHz clock oscillator with differential output.
OSC-50	50 MHz clock oscillator.
OSC-32	32.768 KHz low-power oscillator.
FT4232H	USB-to-quad serial ports in various configurations.
TPS3808G09DBVR	Supervisory circuit that monitors system voltage of 0.9 V, asserting an open-drain reset signal when the sense voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logical low.
I2C port header	16-pin header available for I2C0 and I2C1 interfaces of the SmartFusion2 device.

3 Installation and Settings

This section provides information about the software and hardware settings for the SmartFusion Advanced Development Kit.

3.1 Software Installation

Download and install the Microsemi Libero® SoC software v11.4 or later from the Microsemi website, and register for a free Gold license to the software. The Libero SoC v11.4 or later installer has FlashPro5 drivers. For instructions on how to install Libero SoC and SoftConsole, see *Libero Software Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, which must be installed on the PC where Libero SoC is installed, see *Installing IP Cores and Drivers User Guide*.

The SmartFusion2 FPGA is supported by the latest IAR Embedded Workbench from IAR Systems for ARM IP. It is also supported by the latest Keil MDK-ARM Microcontroller Advanced Development Kit.

3.2 Hardware Settings

This section provides information about default jumper settings, switches, LEDs, and DIP switches for the M2S150-ADV-DEV-KIT.

3.2.1 Jumper Settings

Connect the jumpers with the default settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Settings
Power Supply			
J123	Jumper to select a core voltage (VDD_REG) of 1.0 V or 1.2 V.	Pin 1-2 for 1.0 V.	Open
		Pin 2-3 for 1.2 V.	Close
J353	Jumper to select a core voltage (VCCIO_HPC_VADJ) of 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2V.	Pin 1-2 for 3.3 V.	Closed
		Pin 3-4 for 2.5 V.	Open
		Pin 5-6 for 1.8 V.	Open
		Pin 7-8 for 1.5 V.	Open
		Pin 9-10 for 1.2 V.	Open
J354	Jumper to select a core voltage (VCCIO_LPC_VADJ) of 2.5 V, 1.8 V, 1.5 V, or 1.2V.	Pin 1-2 for 2.5 V.	Closed
		Pin 3-4 for 1.8 V.	Open
		Pin 5-6 for 1.5 V.	Open
		Pin 7-8 for 1.2 V.	Open
J116	Jumpers to select either SW7 input or signal ENABLE_FT4232 from FT4232H chip.	Pin 1-2 for **SW7** switch selection.	Closed
		Pin 2–3 for Enable_FT4232 signal control.	Open

Table 3 • **Jumper Settings *(continued)***

Clocks			
J10	Jumper to select switch-side MUX inputs of A or B to the line side.	Pin 1-2 (Input A to the line side) for external clock required to source the line side through FMC connector.	Open
		Pin 2-3 (Input B to the line side) for external clock required to source the line side through SMA connectors.	Open
J9	Jumper to select the output-enable control for the line side outputs.	Pin 1-2 (line-side output enabled).	Open
		Pin 2-3 (line-side output disabled).	Open
J8	Jumper to select the output-enable control for the line side outputs.	Pin 1-2 (line-side output enabled).	Closed
		Pin 2-3 (line-side output disabled).	Open
J11	Jumper to select switch-side MUX inputs of A or B to the line side.	Pin 1-2 (Input A to the line side), that is, on-board 125 MHz differential clock oscillator output is routed to line side.	Closed
		Pin 2-3 (Input B to the line side), that is, on-board 100 MHz differential clock oscillator output is routed to line side.	Open
Marvell PHY			
J14	Jumper to select either PHY_CONFIG1 or M2S_PHY_CONFIG1 for global hardware configuration (CONFIG[1]).	Pin 1-2 CONFIG [1] connects to P2_LED[2] pin of 88E1340S.	Open
		Pin 2-3 CONFIG [1] connects to SmartFusion2 J8 pin (MSIO80NB3).	Open
J15	Jumper to short AC test points for debugging. It is recommended not to connect this jumper; refer to the Marvell PHY Datasheet.	Two-pin header.	Open
J23	Jumper to provide the VBUS supply to USB when used in host mode.	Two-pin header.	Open
Programming			
J32	JTAG selection jumper to select RVI header or FP4 header for application debug.	Pin 1-2 FP4 for SoftConsole/FlashPro.	Closed
		Pin 2-3 RVI for Keil ULINK or IAR J-Link.	Open
		Pin 2-4 for JTAG_SEL pin to DD1 signal of FT4232H chip.	Open
J121	Jumper to select FTDI JTAG or SPI slave programming.	Pin 1-2 for FTDI JTAG programming.	Closed
		Pin 2-3 for FTDI SPI slave programming.	Open
J124	Jumper to select JTAG programming via FP4 or FTDI.	Pin 1-2 for JTAG programming via FTDI.	Open
		Pin 2-3 for JTAG programming via FP4.	Closed
J125	Jumper to select FTDI SPI-0 or FTDI SPI-1 slave programming	Pin 1-2 for FTDI SPI-1 slave programming.	Open
		Pin 2-3 for FTDI SPI-0 slave programming.	Open

Table 3 • **Jumper Settings *(continued)***

J118	Jumper to select programming SPI-0 flash through FTDI SPI-0 (Port-B) or SmartFusion2 SPI-0.	Pin 1-2 for programming SPI-0 flash via SmartFusion2 SPI-0.	Closed
		Pin 2-3 for programming SPI-0 flash via FTDI SPI-0 (Port-B). J125 pin 2-3 must be shorted.	Open
J119	Jumper to select programming SPI-1 flash through FTDI SPI (Port-B) or SmartFusion2 SPI-1.	Pin 1-2 for programming SPI-1 flash via SmartFusion2 SPI-1.	Closed
		Pin 2-3 for programming SPI-1 flash via FTDI SPI (Port-B). J125 pin 1-2 must be shorted.	Open

For locations of various jumpers and test points on the SmartFusion2 Advanced Development Board, see Figure 20, page 72 and Figure 21, page 73.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

Table 4 • **LEDs**

LED	Description
DS26	Indicates USB_5V supply
DS18	Indicates 0P75V_REG supply
DS19	Indicates 1P5V_REG supply
DS20	Indicates VDD_REG supply
DS21	Indicates 2P5V_LDO supply
DS22	Indicates VCCIO_LPC_VADJ supply
DS23	Indicates VCCIO_HPC_VADJ supply
DS24	Indicates 1P0V_PHY supply
DS25	Indicates 1P8V supply
DS28	Indicates 3P3V_LDO supply
DS17	Indicates 5P0V supply
DS29	Indicates 3P3V supply
DS16	Indicates 12P0V supply
DS27	Indicates VSS_BUS supply
DS8	Indicates that DS8 is connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS9	Indicates that DS9 is connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS10	Indicates that DS10 is connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY
DS14	Indicates that DS14 is connected to parallel LED output port 1 (P1_LED[0]) of Marvell PHY
DS13	Indicates that DS13 is connected to parallel LED output port 1 (P1_LED[1]) of Marvell PHY
DS12	Indicates that DS12 is connected to parallel LED output port 1 (P1_LED[2]) of Marvell PHY
DS11	Indicates that DS11 is connected to parallel LED output port 1 (P1_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists USB, ground, and other test points.

Table 5 • **Test Points**

Test Point	Description
TP20, TP33,TP16	GND
TP7	VDD_REG
TP12	12 V
TP11	5 V
TP4	3.3 V
TP29	VCCIO_HPC_VADJ
TP28	VCCIO_LPC_VADJ
TP30	3P3V_LDO
TP31	2P5V_LDO
TP9	1.5 V
TP10	0.75 V
TP14	1.8 V
TP27	VDDIO for the USB device
TP24	PHY 1.0 V

3.3 Power Sources

The following table lists the key power supplies required for normal operation of the SmartFusion2 Advanced Development Kit.

Table 6 • **I/O Voltage Rails**

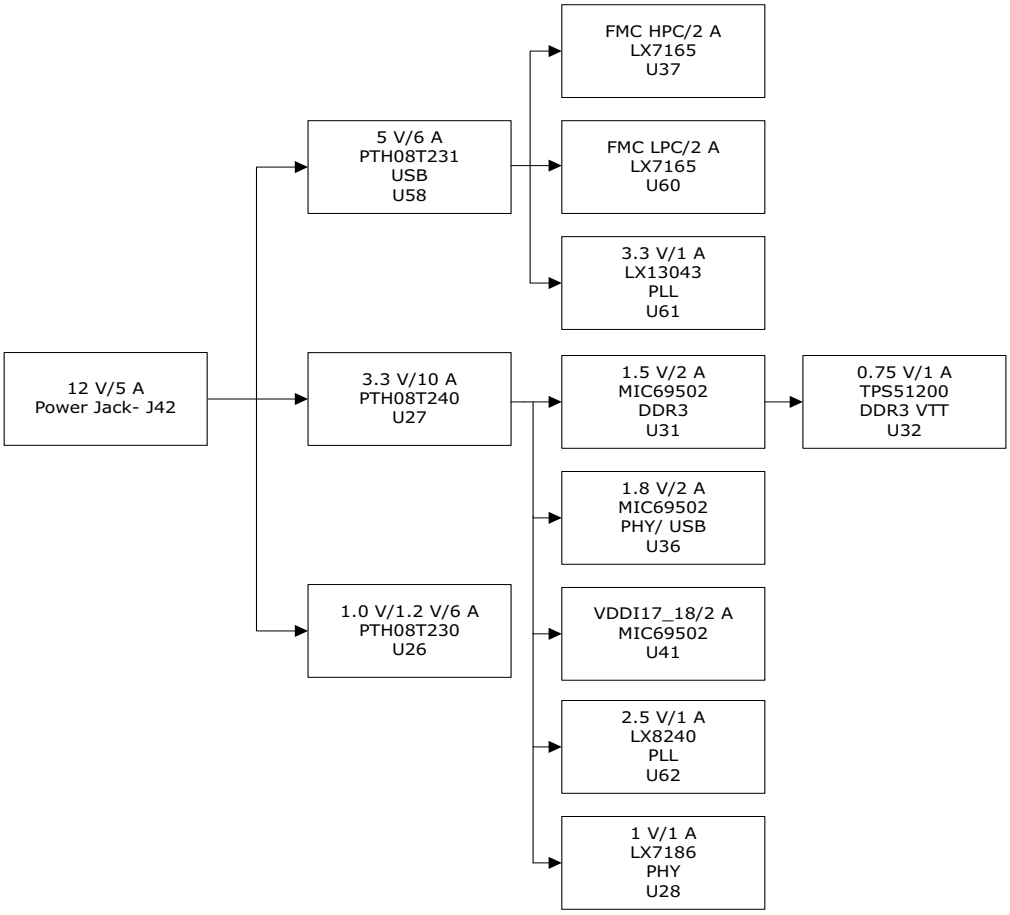
SmartFusion2 Bank	I/O Rail	Voltage
Bank0	VCCIO_HPC_VIO_B_M2S	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank1	2P5V_LDO	2.5 V
Bank2	1P5V_REG	1.5 V
Bank3	3P3V	3.3 V
Bank4	3P3V	3.3 V
Bank5	VCCIO_HPC_VIO_B_M2S	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank6	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank7	3P3V	3.3 V
Bank8	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank9	2P5V_LDO	2.5 V
Bank10	2P5V_LDO	2.5 V
Bank11	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank12	2P5V_LDO	2.5 V
Bank13	2P5V_LDO	2.5 V
Bank14	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V

Table 6 • **I/O Voltage Rails *(continued)***

Bank15	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank16	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank17	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Bank18	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or1.2 V
VDD	VDD_REG	1.2 V or 1.0 V
VPP	3P3V_VPP	3.3 V
VREF1	VREF1	0.75 V
VREF2	0P75V_VTT_REF	0.75 V
SERDES_*x*_PLL_VDDA	PLL_SERDES*x*_VDDA	3.3 V
SERDES_*x*_L01_VDDAPLL	SERDESx_VDDPLL	2.5 V
SERDES_x_VDD	VDD_REG	1.2 V or 1.0 V

The following figure shows the voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.75 V) available in the SmartFusion2 Advanced Development Kit.

Figure 3 • **Voltage Rails in SmartFusion2 Advanced Development Kit**



4 Key Components Description and Operation

This section describes the key component interfaces of the SmartFusion2 Advanced Development Kit. For device datasheets, go to *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2-kits*.

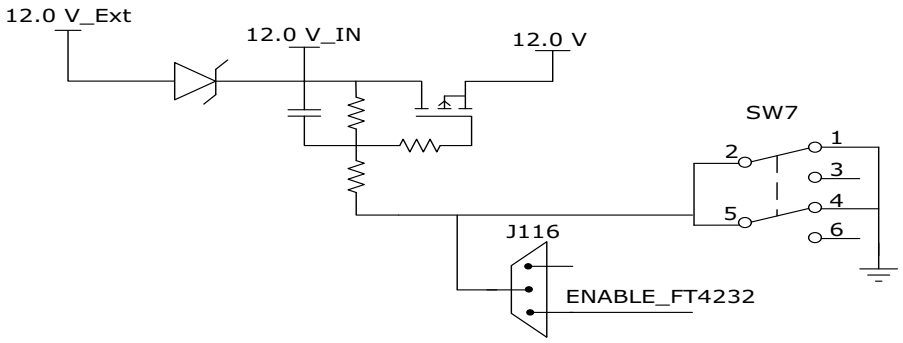
4.1 Powering Up the Board

The SmartFusion2 Advanced Development Board is powered using a 12 V external DC jack (12P0V_Ext), as shown in the following figure.

To power up the board:

1. Connect the 12 V power supply brick to the **J42** jumper to supply power to the board.
2. Switch ON the **SW7** power supply switch.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing in various modes.

4.2.1 1.0 V or 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U59 with gain 100) is provided on the board to measure the output voltage at the **TP17** test point.

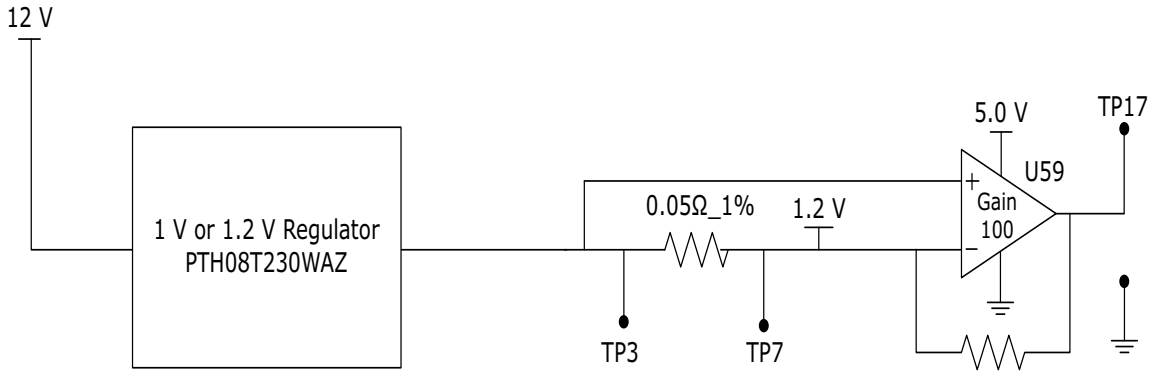
The following steps describe how to measure the core power.

1. Measure the output voltage (V_{OUT}) at TP17.
2. I = (V_{OUT}/5).
3. Core power consumed (P) = (1.2 V) × I.

For example, when the voltage measured across TP17 is 0.5 V, the core power consumed is 0.12 W.

The following figure shows the on-board core power measurement circuitry.

Figure 5 • **Core Power Measurement Circuitry**



4.2.2 1.2 V Current Sensing for Flash*Freeze Mode

The SmartFusion2 device consumes very less power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multimeter that can read sub-millivolts. The **TP16** and **TP17** test points can be used to directly measure the voltage across the 1.2 V sense resistor.

To convert the voltage measured across a sense resistor to power, use the following equation.

$$\text{Power} = \left(\frac{\text{voltage\_in\_millivolts}}{0.05}\right) \times 1.2$$

Note: Accuracy is ± 10%.

4.3 Memory Interface

Dedicated I/Os for MSS DDR and fabric DDR are available in the SmartFusion2 device.

4.3.1 DDR3 SDRAM

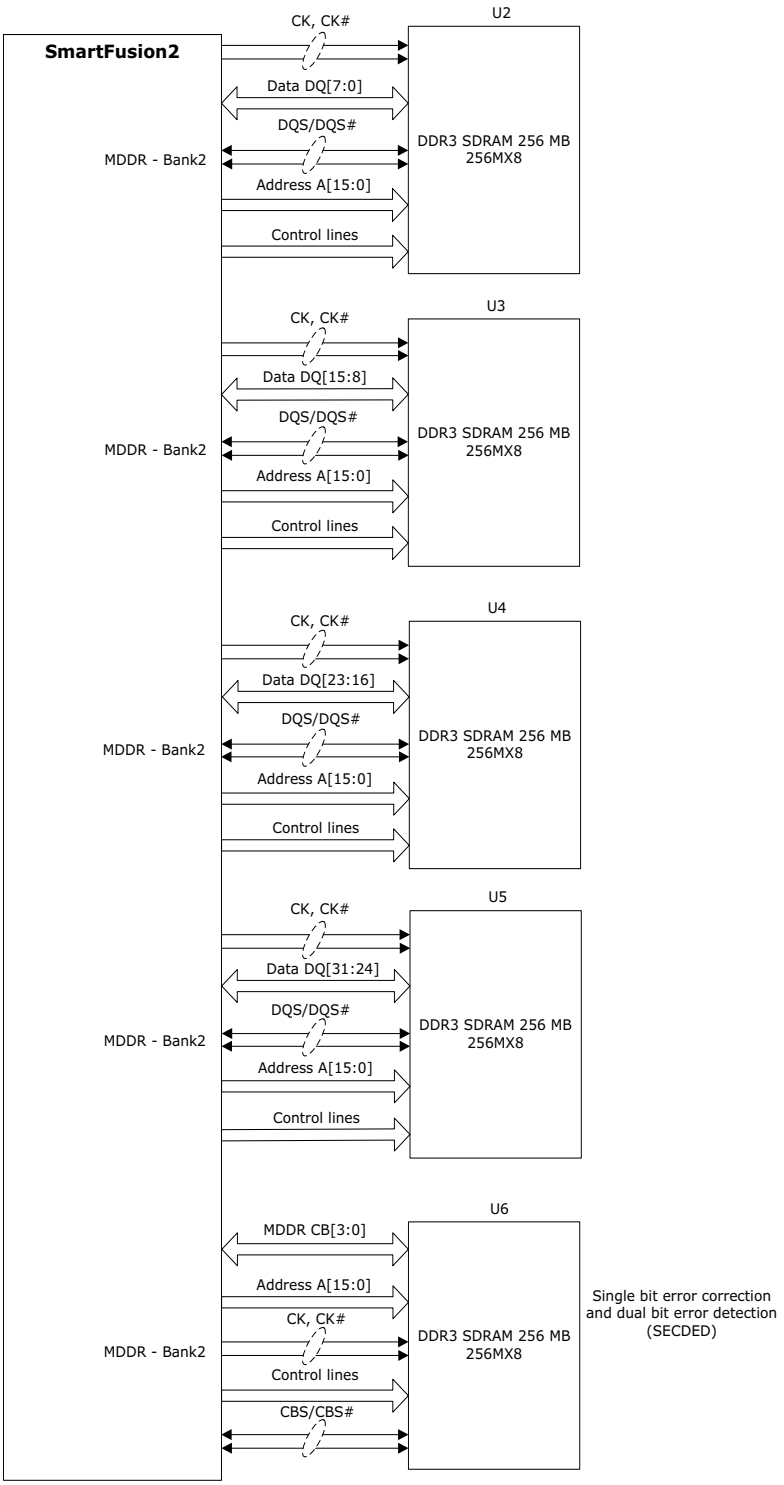
Four chips with 256 MB DDR3 memory are provided in the SmartFusion2 device as flexible volatile memory for user applications. Additionally, one chip with 256 MB DDR3 memory is provided for ECC. You can enable the SECDED feature using ECC. The DDR3 interface is implemented in Bank2.

DDR3 SDRAM specifications for the SmartFusion2 device are as follows.

- MT46H32M16LF: 32 Meg × 8 × 8 banks
- Density: 256 MB
- Clock rate: 800 MHz
- Data rate: DDR3 - 1600
- Total capacity: 1 GB across four chips

The following figure shows the SmartFusion2 memory interface.

Figure 6 • **SmartFusion2 Memory Interface**



For more information, see the Board Level Schematics document (provided separately).

4.4 SerDes Interface

The SmartFusion2 Advanced Development Kit has x4 SerDes interfaces. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, and/or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60).

Note: All SerDes TXD pairs (SERDES0, SERDES1, SERDES2, and SERDES3) are capacitively coupled to the SmartFusion2 device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.

For more information, see the Board Level Schematics document (provided separately).

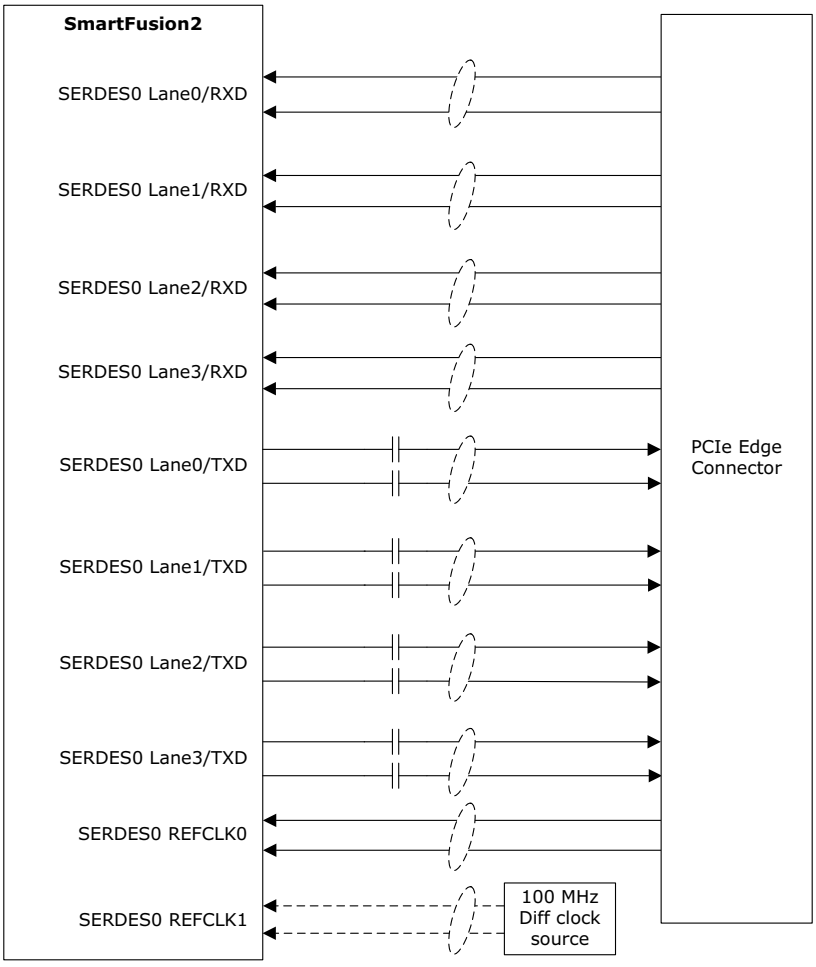
4.4.1 SERDES0 Interface

The SERDES0 interface (Lane 0,1, 2, or 3) is directly routed to the PCIe connector. The SerDes reference clocks are routed as follows.

- SERDES0 reference clock 0 is directly routed from the PCIe connector to the SmartFusion2 device.
- SERDES0 reference clock 1 is routed from the 100 MHz differential clock source (LVDS clock oscillator) through resistors.

The following figure shows the SERDES0 interface of the SmartFusion2 Advanced Development Board.

Figure 7 • **SERDES0 Interface**



Note: Mount R977 and R978 to source the clock from 100 MHz differential oscillator to the SERDES0 REFCLK1.

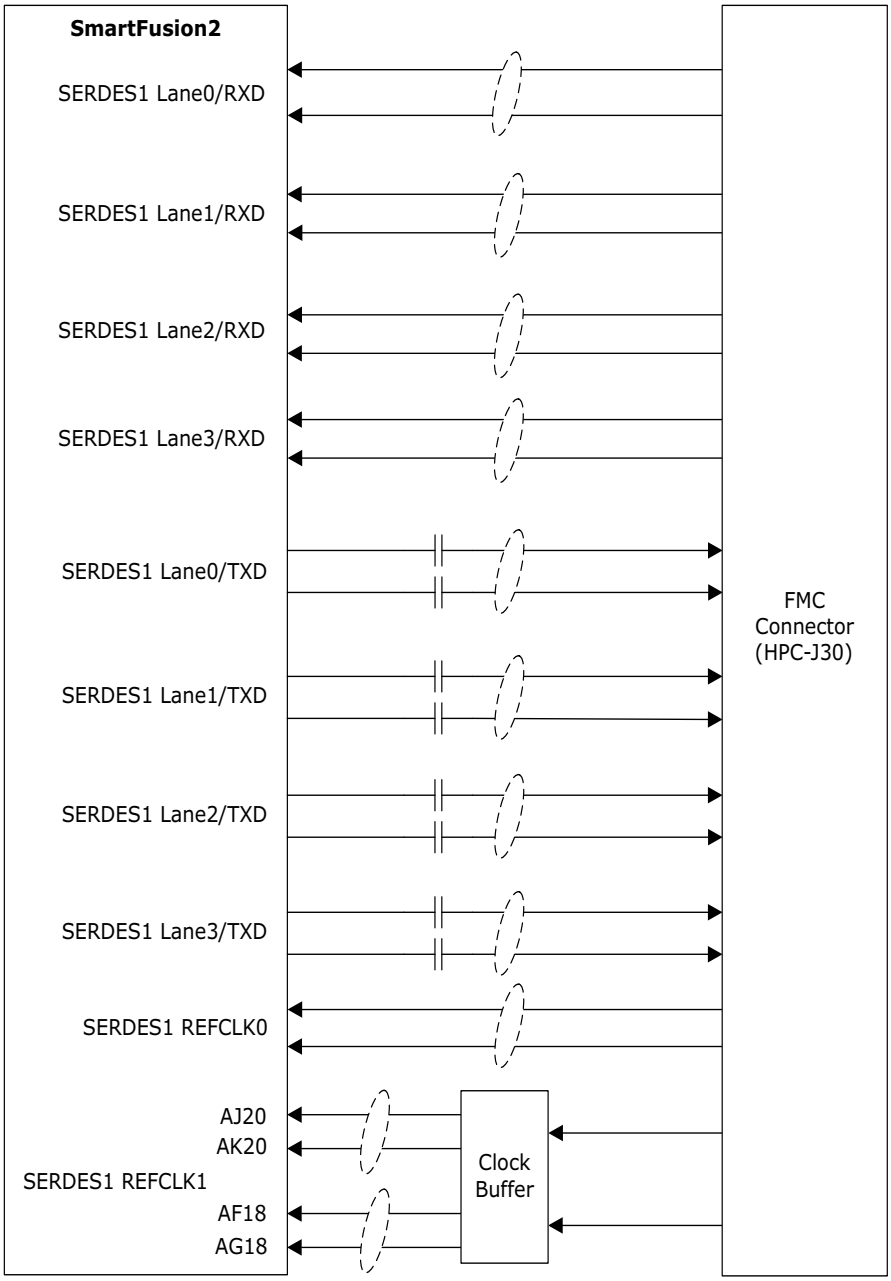
4.4.2 SERDES1 Interface

The SERDES1 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES1 reference clock 0 is routed from the FMC connector.
- SERDES1 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AF18 and AG18.

The following figure shows the SERDES1 interface of the SmartFusion2 Advanced Development Board.

Figure 8 • **SERDES1 Interface**



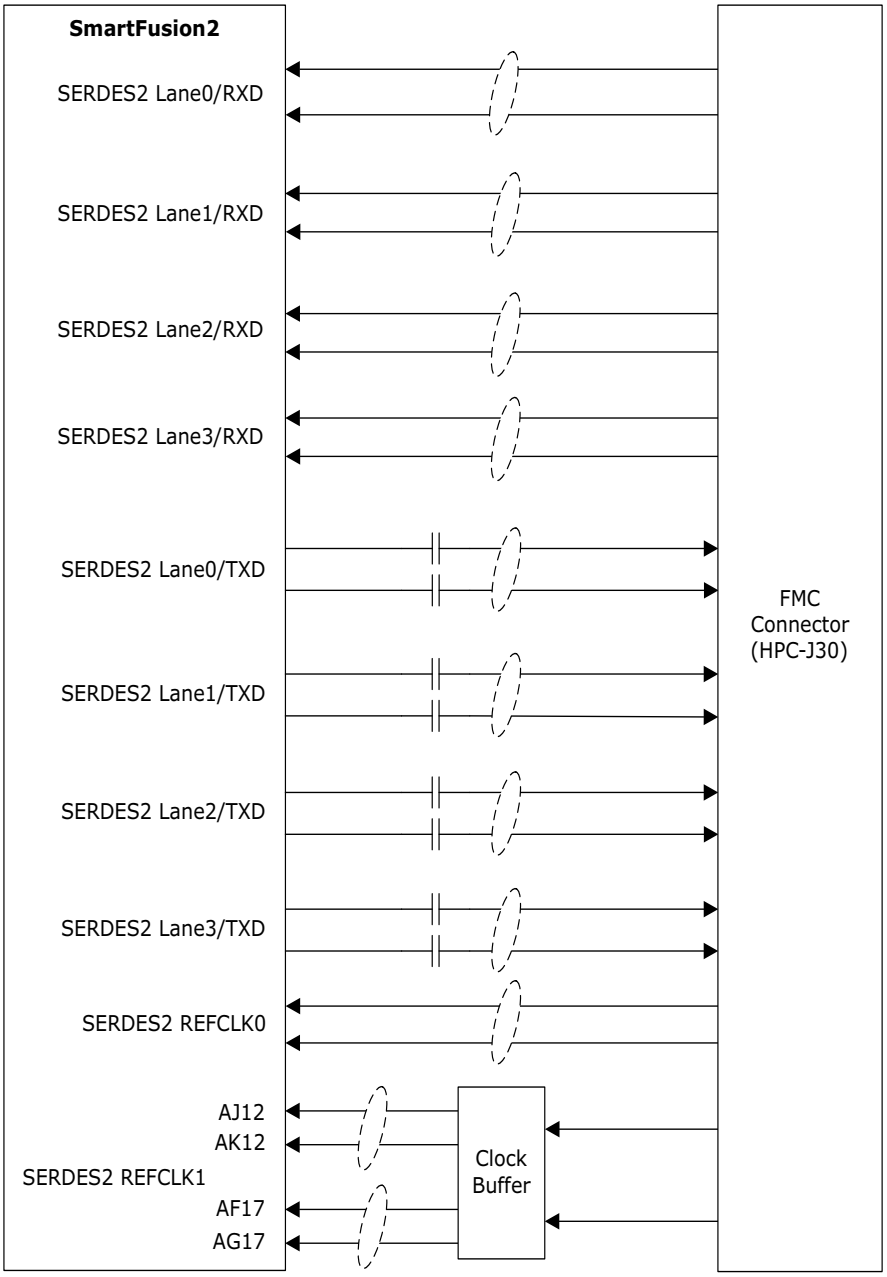
4.4.3 SERDES2 Interface

The SERDES2 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES2 reference clock 0 is routed from the FMC connector.
- SERDES2 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AE17 and AF17.

The following figure shows the SERDES2 interface of the SmartFusion2 Advanced Development Board.

Figure 9 • **SERDES2 Interface**



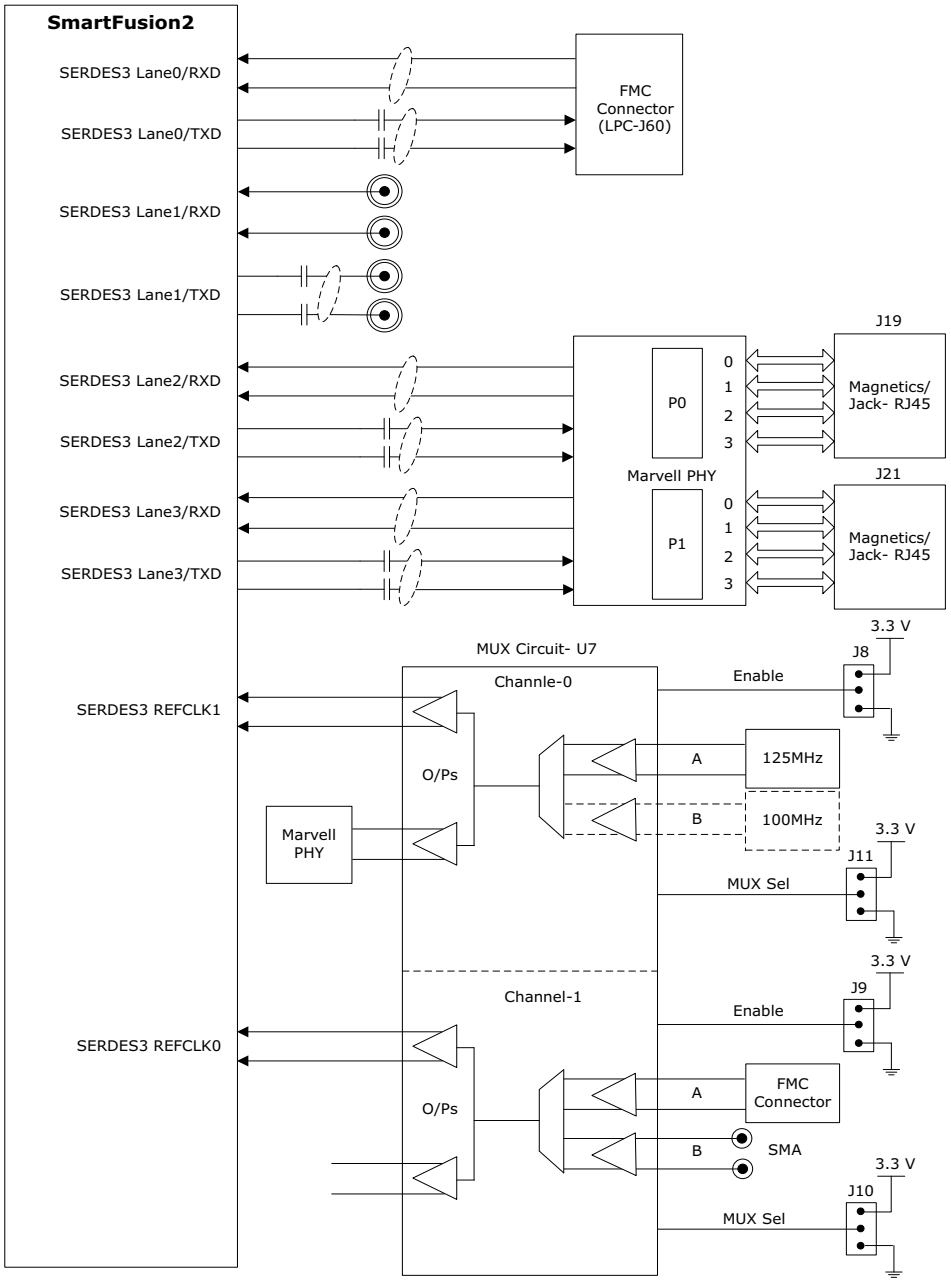
4.4.4 SERDES3 Interface

The SERDES3 lanes are connected as follows.

- Lane 0 is connected to the FMC connector.
- Lane 1 is connected to the SMA connectors.
- Lanes 2 and 3 are connected to the Marvell PHY device ports 0 and 1, respectively.
- SERDES3 reference clock 0 is connected from FMC connector or SMA connector through MUX.
- SERDES3 reference clock 1 is connected from 125 MHz or 100 MHz through MUX.

The following figure shows the SERDES3 interface of the SmartFusion2 Advanced Development Board.

Figure 10 • **SERDES3 Interface**

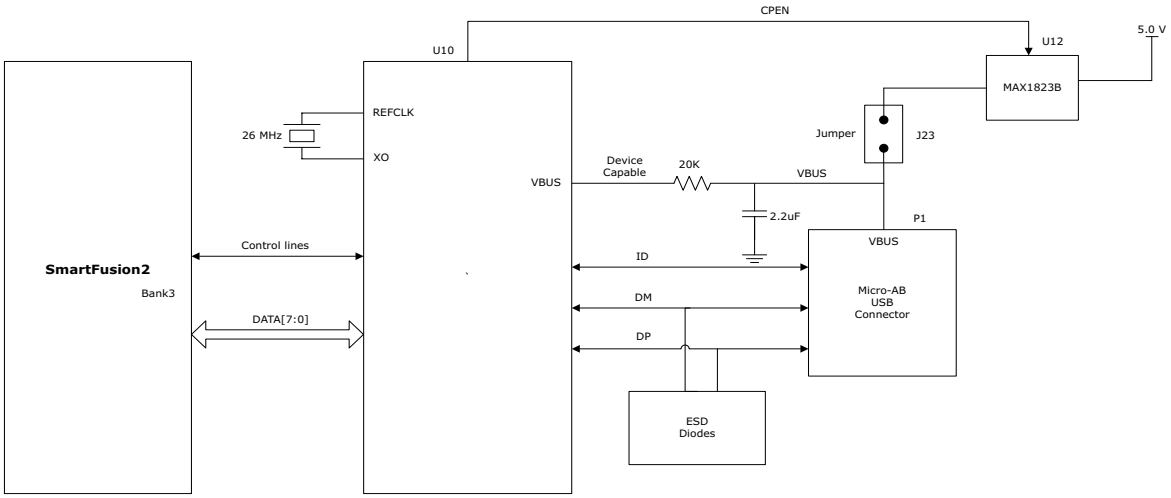


4.5 USB Interface

The following figure shows the USB interface of the SmartFusion2 Advanced Development Board. The SMSC USB3320 shown in the following figure is a high-speed USB 2.0 ULPI transceiver that provides the industry standard UTMI+ low pin interface to connect the USB transceiver to the link. CPEN (shown in the figure) is the external 5 V supply enable pin that controls the external VBUS power switch.

In the SmartFusion2 Advanced Development Kit, the USB interface can operate in host, device, and OTG modes. To use device mode, J23 can either be in open or shorted. To use host or OTG mode, pins 1 and 2 of the **J23** jumper must be closed.

Figure 11 • **USB Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Marvell PHY (88E1340S)

The SmartFusion2 Advanced Development Kit uses the on-board Marvell Alaska PHY device 88E1340S for Ethernet communications at 10 or 1000 Mbps. The device has four independent gigabit Ethernet transceivers; however, the board uses only two of these transceivers. Each transceiver performs all the PHY functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

Device 88E1340S supports Quad SGMII for direct connection to a SmartFusion2 chip. It is configured through the CONFIG [3:0] and CLK_SEL [1:0] pins.

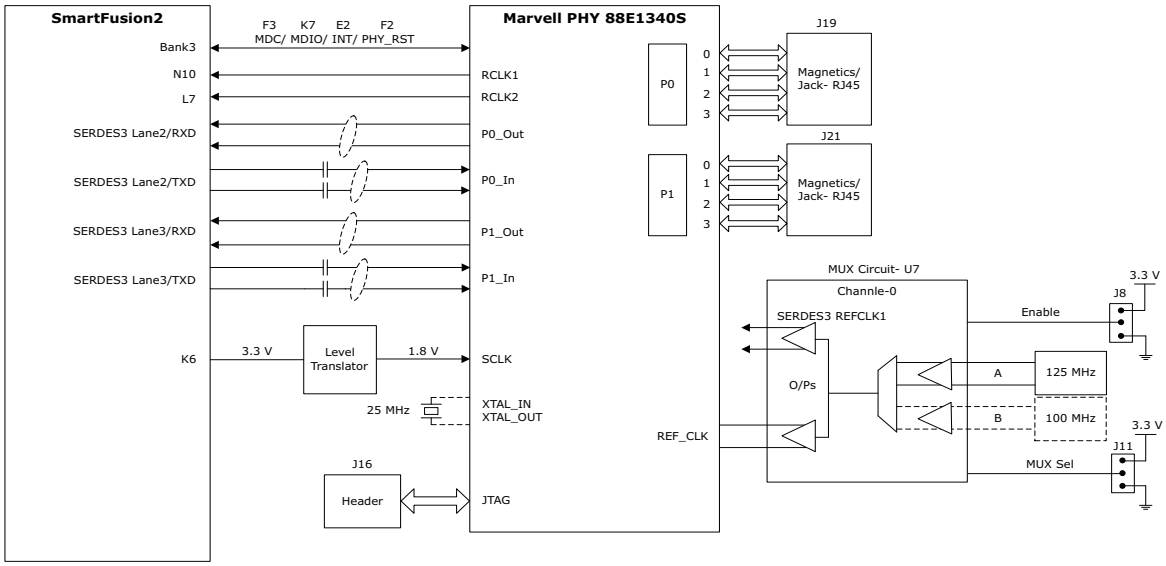
The CLK_SEL [1:0] pin is used to select the reference clock input. On the board, the status of the CLK_SEL0 pin is *high* and the status of the CLK_SEL1 pin is *low*. REF_CLK is a 125 MHz reference differential clock input (Y11). It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

Key features of Marvell PHY 88E1340S are as follows.

- RCLK: Gigabit recovered clock
- SCLK: 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications:
  - Voltage level: 3.3 (± 0.3) V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SmartFusion2 Marvell PHY interface.

Figure 12 • **Marvell PHY Interface**



For more information, see the Board Level Schematics document (provided separately).

4.7 Programming

SmartFusion2 SoC FPGAs support multiple programming interfaces and can address a wide range of platform requirements. A SmartFusion2 device can be programmed through the JTAG and SPI interfaces.

The dedicated programming SPI port can operate in SPI slave or SPI master modes.

For more information, see *SmartFusion2 and IGLOO2 Programming User Guide*.

The following figure shows the programming interface of the SmartFusion2 Advanced Development Board.

Figure 13 • **Programming Interface**