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M30LW128D

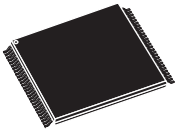
128 Mbit (two 64Mbit, x8/x16, Uniform Block, Flash Memories) 3V Supply, Multiple Memory Product

PRELIMINARY DATA

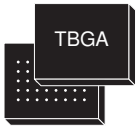
FEATURES SUMMARY

- TWO M58LW064D 64Mbit FLASH MEMORIES STACKED IN A SINGLE PACKAGE
- WIDE x8 or x16 DATA BUS for HIGH BANDWIDTH
- SUPPLY VOLTAGE
  - V_{DD} = 2.7 to 3.6V for Program, Erase and Read operations
  - V_{DDQ} = 1.8 to V_{DD} for I/O buffers
- ACCESS TIME
  - Random Read 110ns
  - Page Mode Read 110/25ns
- PROGRAMMING TIME
  - 16 Word Write Buffer
  - 16µs Word effective programming time
- 128 UNIFORM 64 KWord/128KByte MEMORY BLOCKS
- BLOCK PROTECTION/ UNPROTECTION
- PROGRAM and ERASE SUSPEND
- 128 bit PROTECTION REGISTER
- COMMON FLASH INTERFACE
- 100, 000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code M30LW128D: 8817h

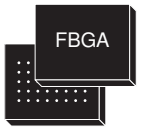
Figure 1. Packages



TSOP56 (N)
14 x 20 mm



TBGA64 (ZA)
10 x 13mm



LFBGA88 (ZE)
8 x 10mm

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SUMMARY DESCRIPTION

The M30LW128D is a 128 Mbit device that is composed of two separate 64 Mbit M58LW064D Flash memories. The device can be erased electrically at block level and programmed in-system using a 2.7V to 3.6V (V_{DD}) supply for the circuitry and a 1.8V to V_{DD} (V_{DDQ}) supply for the Input/Output pins.

The bus width can be configured for x8 or x16 for the devices available in the TSOP56 (14 x 20 mm) and TBGA64 (10x13mm**,** 1mm pitch) packages. The bus width is set to x16 for the devices available in the LFBGA88 (8x10mm, 0.8mm pitch) package.

Each internal M58LW064D has 3 Chip Enable signals to allow up to 4 memories to be connected together without the use of additional glue logic. In this way the address space is contiguous and the microprocessor only requires one Chip Enable, $\overline{E}$, to control both memories.

The device is divided into 128 blocks of 1Mbit (2 x 64 x 1Mb) that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the device. An on-chip Program/Erase Controller (P/E.C) simplifies the process of programming or erasing the device by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the device is consistent with JEDEC standards.

The Write Buffer allows the microprocessor to program from 1 to 16 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

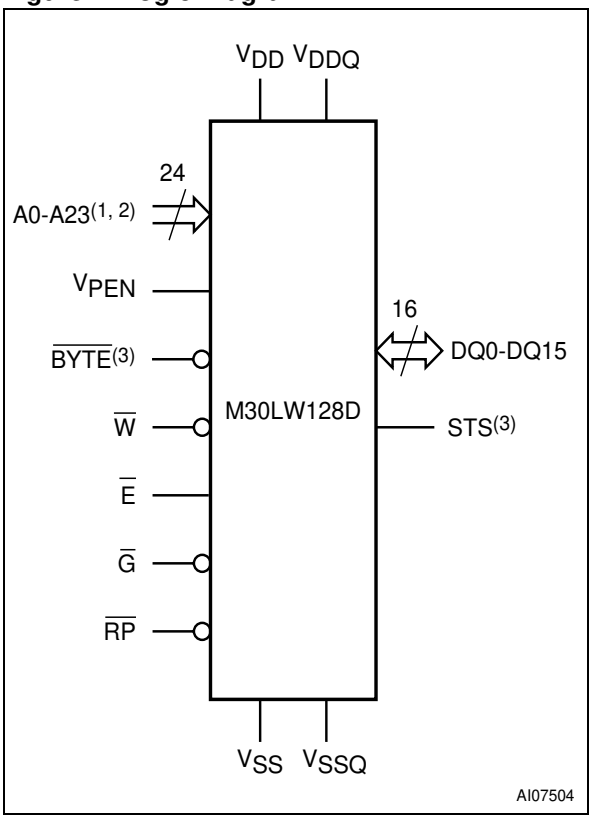
Individual block protection against Program or Erase is provided for data security. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed. Software commands are provided to allow protection of some or all of the blocks and to cancel all block protection bits simultaneously. All Program or Erase operations are blocked when the Program Erase Enable input V_{PEN} is low.

The Reset/Power-Down pin is used to apply a Hardware Reset to the enabled memory and to set the device in power-down mode.

The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes: Ready/Busy mode where a static signal indicates the status of the P/E.C, and Status mode where a pulsing signal indicates the end of a Program or Block Erase operation. In both modes it can be used as a system interrupt signal, useful for saving CPU time. The STS signal is only available with the TSOP56 and TBGA64 packages.

Each memory includes a 128 bit Protection Register. The Protection Register is divided into two 64 bit segments, the first one is written by the manufacturer (contact STMicroelectronics to define the code to be written here), while the second one is programmable by the user. The user programmable segment can be locked.

Figure 2. Logic Diagram



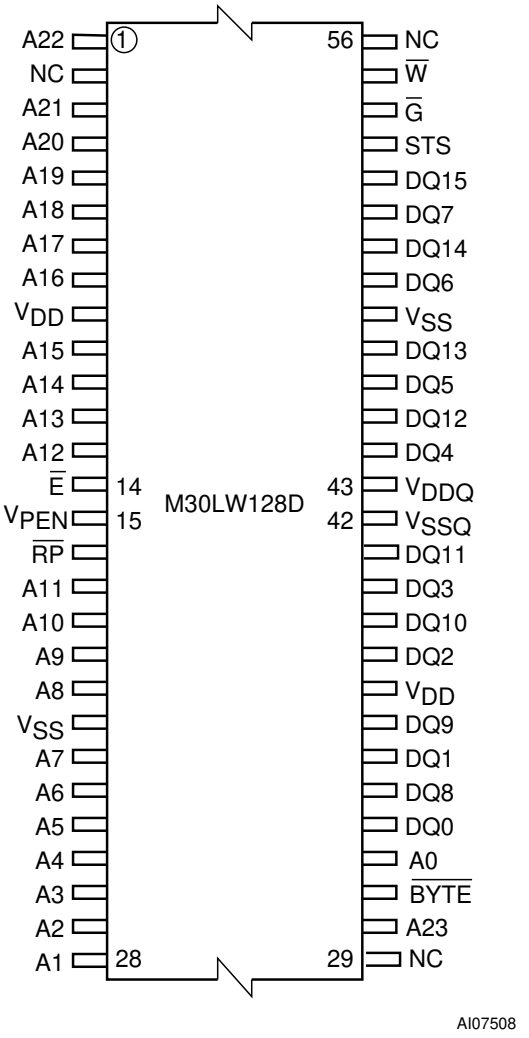
Note: 1. A0-A22 for LFBGA package (x16 only), A0 is the least significant address.
2. A0-A23 for TSOP and TFBGA packages, in x8 mode A0 is the least significant address, in x16 mode A1 is the least significant address and A0 is don't care.
3. Not available with LFBGA package.

Table 1. Signal Names

A0-A23(1, 2)	Address inputs
$\overline{BYTE}$ (3)	Byte/Word Organization Select
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{RP}$	Reset/Power-Down
STS (3)	Status/(Ready/Busy)
V_{PEN}	Program/Erase Enable
$\overline{W}$	Write Enable
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally
DU	Do Not Use

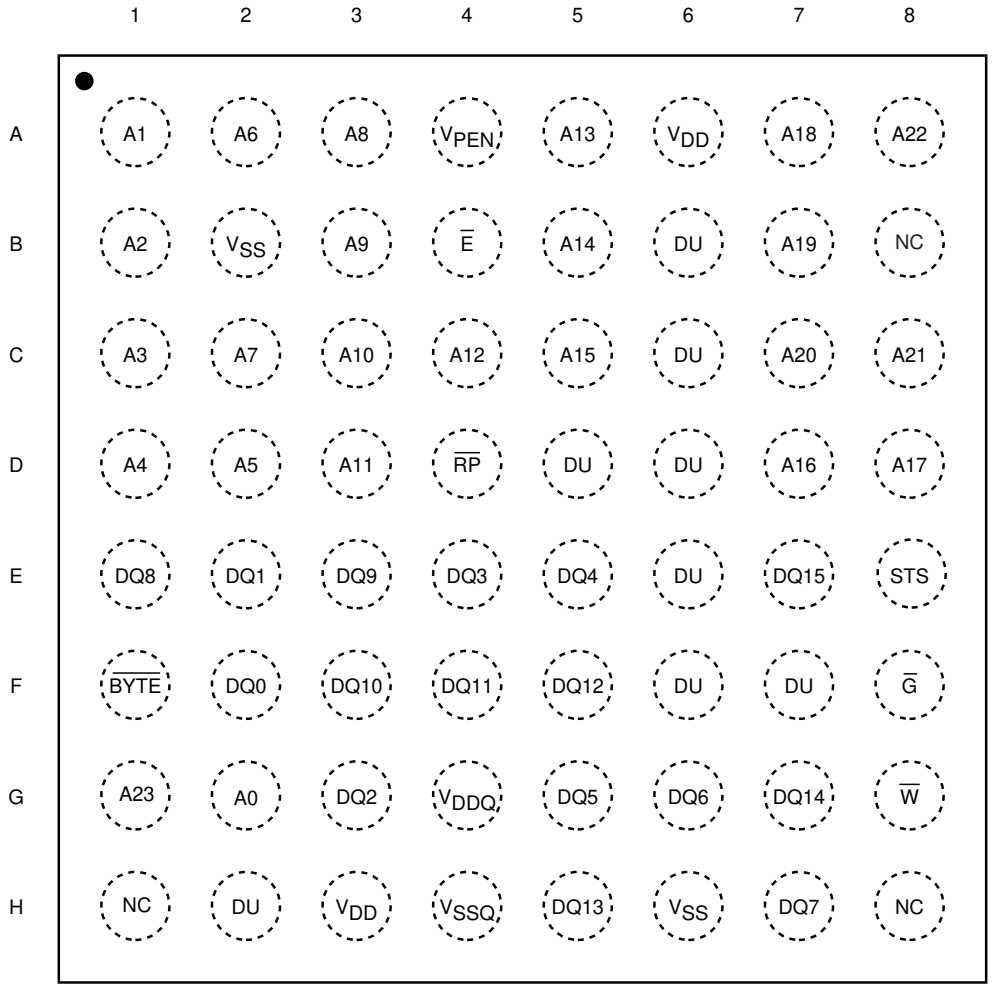
Note: 1. A0-A22 for LFBGA package (x16 only), A0 is the least significant address.
2. A0-A23 for TSOP and TFBGA packages, in x8 mode A0 is the least significant address, in x16 mode A1 is the least significant address and A0 is don't care.
3. Not available with LFBGA package.

Figure 3. TSOP56 Connections



Note: Pin 2 (E1 for a single M58LW064D device) and pin 29 (E2 for a single M58LW064D device) are NC (not connected). They should be tied to ground (V_{SS}) to assure compatibility with a single chip 128Mbit device.

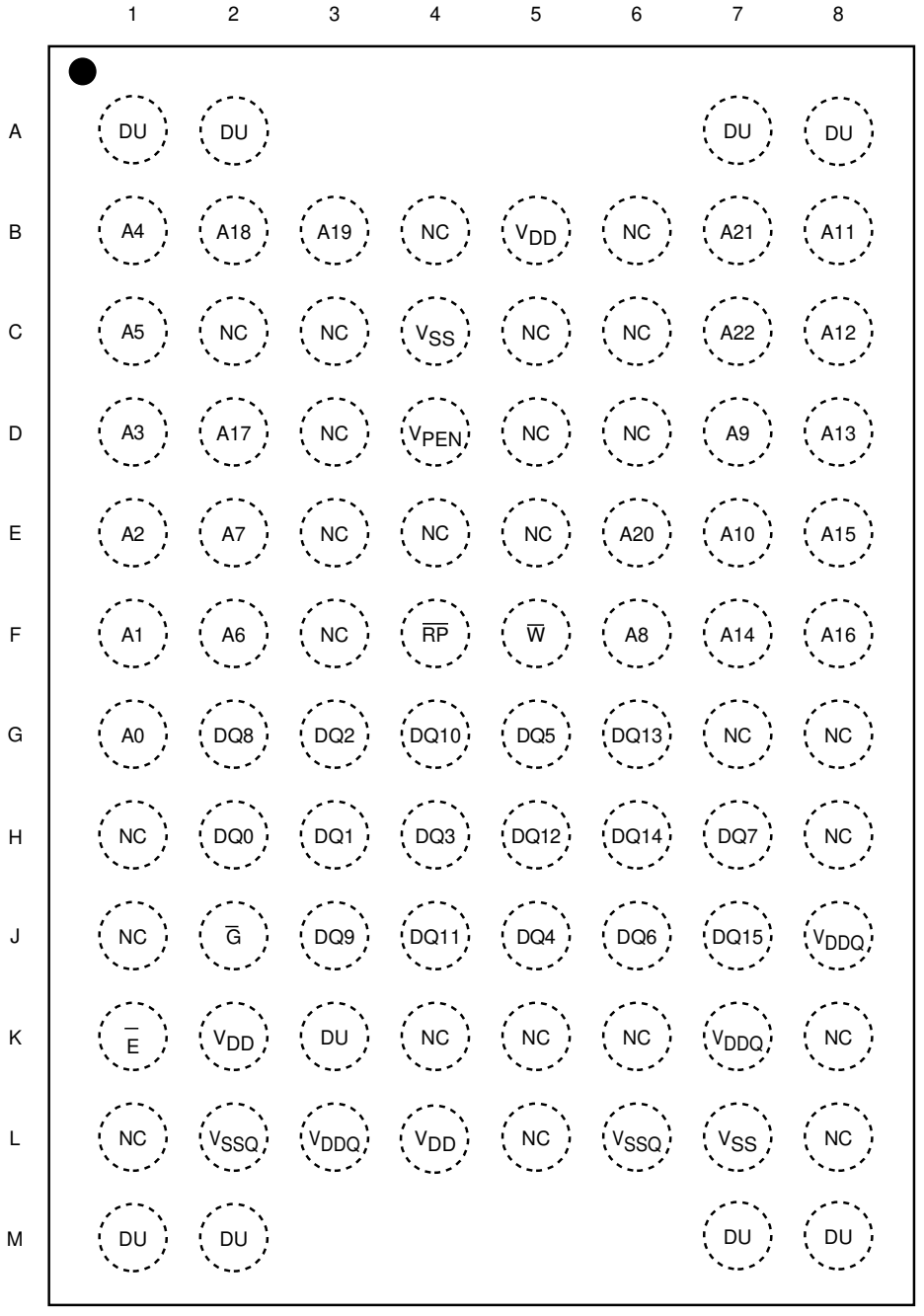
Figure 4. TBGA64 Connections (Top view through package)



AI07505

Note: Ball B8 (E1 for a single M58LW064D device) and ball H1(E2 for a single M58LW064D device) are NC (not connected). They should be tied to ground (V_{SS}) to assure compatibility with a single chip 128Mbit device.

Figure 5. LFBGA Connections (Top view through package)



Note: 1. $\overline{\text{BYTE}}$ and STS connections are not available with the LFBGA88 package.
2. Address Inputs are A0-A22 as only the x16 mode is supported in the LFBGA package. A0 is the least significant while A22 is the most significant address.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A23). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface.

The device must be enabled (refer to Table 3, M30LW128D Device Enable) when selecting the addresses. The address inputs are latched on the rising edge of Write Enable, $\overline{W}$, or Chip Enable, $\overline{E}$, whichever occurs first.

For the TSOP and TFBGA packages the address inputs are A0-A23. A0 is used to select the higher or lower byte in x8 mode; it's not used in x16 mode where A1 is the least significant address.

Address input A23 is used to select between the two internal memories. When it is High, V_{IH}, it selects the Upper Memory, when it is Low, V_{IL}, it selects the Lower Memory. Refer to Memory Enable section for more details.

As the LFBGA package only supports x16 mode this package has all the addresses shifted down by one with respect to the TSOP and TFBGA packages. So for the LFBGA package the address inputs are A0-A22 and address input A22 is used to select between the two internal memories. When it is High, V_{IH}, it selects the Upper Memory, when it is Low, V_{IL}, it selects the Lower Memory. Refer to Memory Enable section for more details.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, $\overline{E}$, whichever occurs first.

When the device is enabled and Output Enable is low, V_{IL}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the device is deselected, Output Enable is high, V_{IH}, or the Reset/Power-Down signal is low, V_{IL}. When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. The M30LW128D stacked memory uses the A23 (A22 for LFBGA package) address input and the external Chip Enable, $\overline{E}$, to select and enable the internal memories. Refer to Memory Enable section and Table 3, for more details.

When the Chip Enable deselects the memory, power consumption is reduced to the Standby level, I_{DD1}.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable.

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down signal can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. When Reset/Power-Down is Low, V_{IL}, the Status Register information is cleared and the power consumption is reduced to power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL},during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the STS pin stays low, V_{IL}, for a maximum timing of $t_{PLPH} + t_{PHBH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH}, the device will be ready for Bus Read and Bus Write operations after t_{PHQV}. Note that STS does not fall during a reset, see Ready/Busy Output section.

In an application, it is recommended to associate Reset/Power-Down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the device is performing an Erase or Program operation, the device may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Byte/Word Organization Select ($\overline{BYTE}$). The Byte/Word Organization Select signal is used to switch between the x8 and x16 bus widths of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

The Byte/Word Organization Select signal is not available with the LFBGA88 package.

Status/(Ready/Busy) (STS). The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

- Ready/Busy - the pin is Low, V_{OL}, during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
- Status - the pin gives a pulsing signal to indicate the end of a Program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several devices to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active.

The STS signal is not available with the LFBGA88 package.

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, V_{SS}, is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 10, AC Measurement Load Circuit.

MEMORY ENABLE

Each internal M58LW064D memory has 3 Chip Enable signals to allow up to 4 memories to be connected together without the use of additional glue logic, see Table 2, Single M58LW064D Device Enable. In this way the address space is contiguous and the microcontroller only requires one Chip Enable, $\overline{E}$, to control both memories.

Figure 6 shows how a 128Mbit Stacked Flash memory is created using two M58LW064D memories. One of the memories is located in the Upper Address space and is referred to as the Upper Memory, the other is located in the lower address space and is referred to as the Lower Memory, see Figure 7, Block Addresses.

The E0, E1 and E2 Chip Enables of each M58LW064D memory are connected internally, as shown in Figure 6.

The external signal A23 (A22 for LFBGA package) is used to select between the Upper and Lower memories. A23 (A22 for LFBGA) is connected to E2 of the Upper Memory and to E1 of the Lower Memory.

E1 of the Upper Memory is always connected to V_{DD} while E2 of the Lower Memory is always connected to V_{SS}.

The external Chip Enable, $\overline{E}$, is used to enable or disable the memory selected by A23 (A22 for LFBGA), see Table 3, M30LW128D Device Enable. $\overline{E}$ is connected to the E0 signal of both memories.

The M30LW128D (TSOP56 and TBGA64 packages only) supports both x8 and x16 bus widths. It is also possible to have a x32 bus width by connecting two x16 bus width M30LW128D devices together. Note that the two M30LW128D devices must use the same E0 as Chip Enable, as E1 and E2 are not connected internally.

Table 2. Single M58LW064D Device Enable, E2, E1 and E0

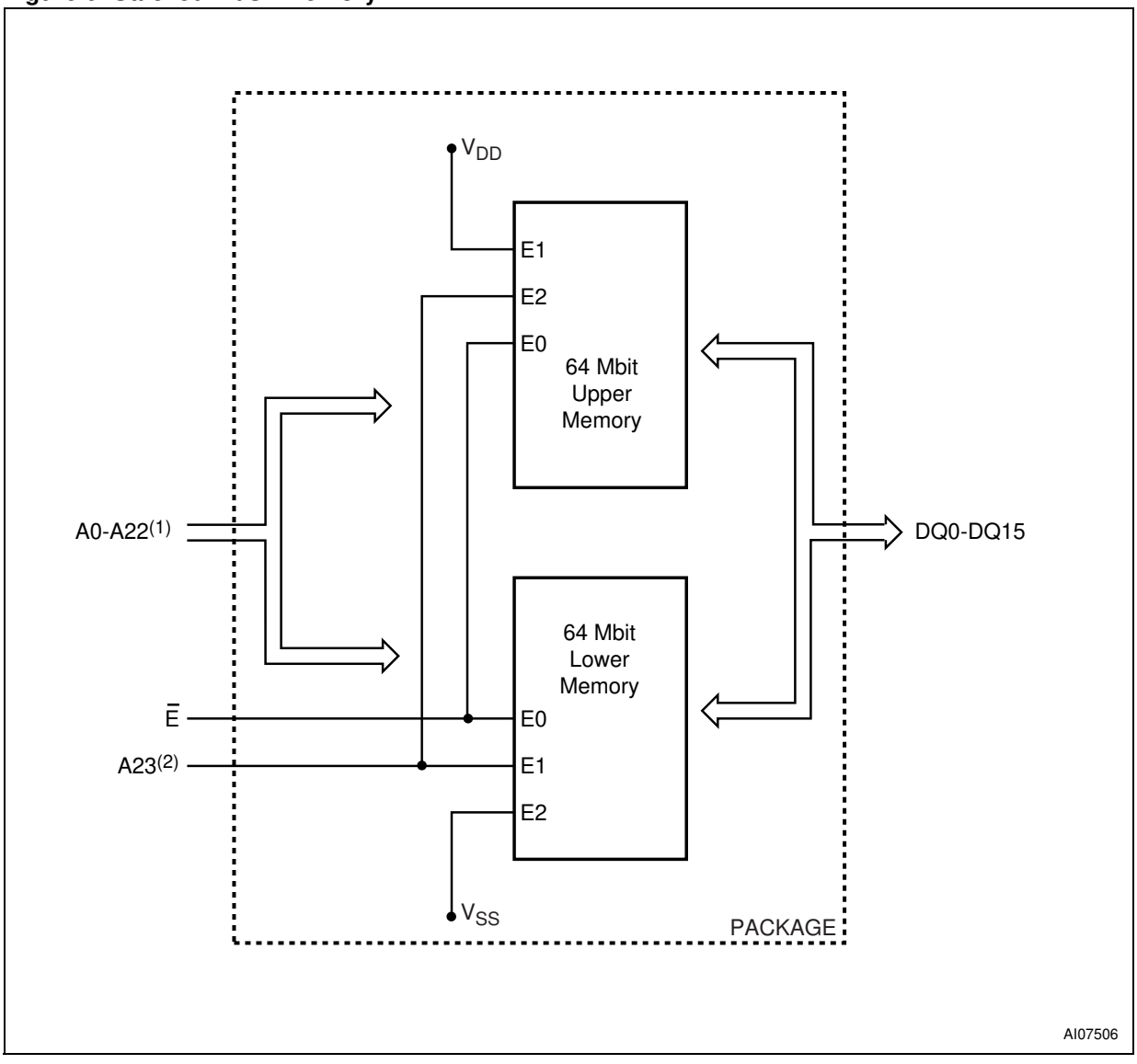
E2	E1	E0	Device
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

Table 3. M30LW128D Device Enable

A23(1)	Internal Signals		Chip Enable, $\overline{E}$	Upper Memory	Lower Memory
$E2_{UM} = E1_{LM}$ (1)	$E1_{UM}$ (1)	$E2_{LM}$ (1)	$E0_{UM} = E0_{LM}$ (1)		
V_{IL}	V_{DD} (V_{IH})	V_{SS} (V_{IL})	V_{IL}	Disabled	Enabled
V_{IL}			V_{IH}	Disabled	Disabled
V_{IH}			V_{IL}	Enabled	Disabled
V_{IH}			V_{IH}	Disabled	Disabled

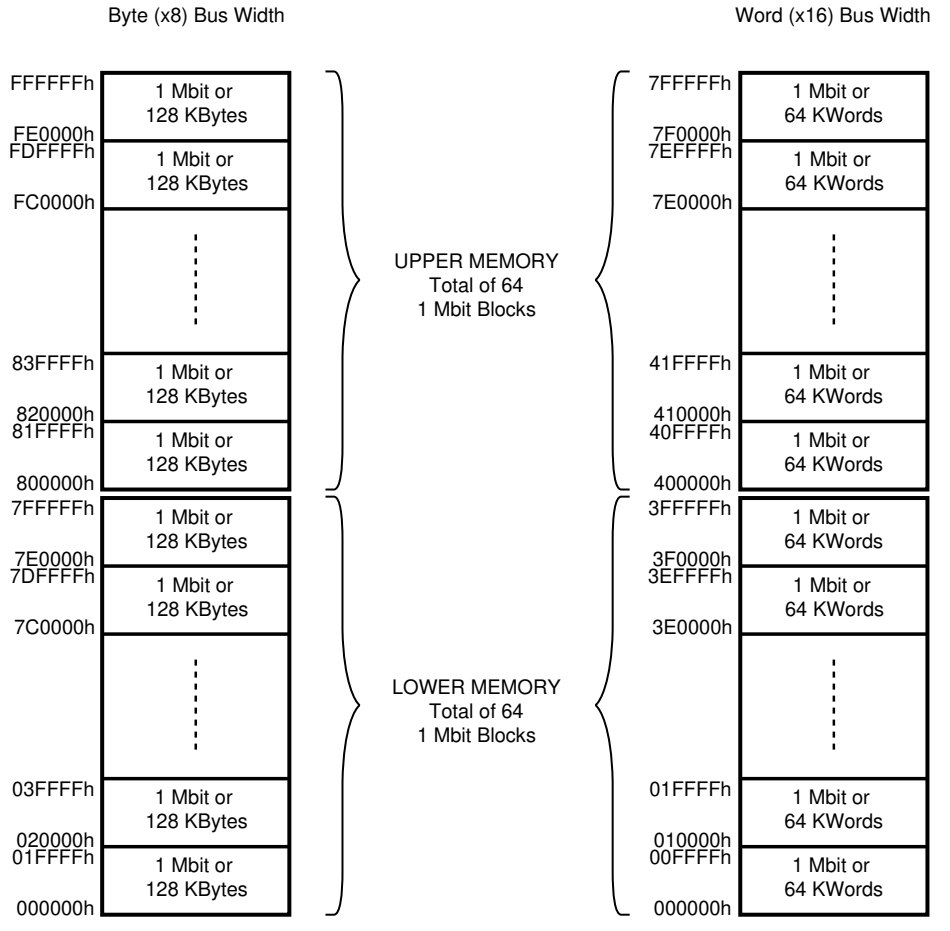
Note: 1. UM = Upper Memory, LM = Lower Memory.
2. A22 for LFBGA package.

Figure 6. Stacked Flash Memory



Note: 1. A0-A21 for LFBGA package.
2. A22 for LFBGA package.

Figure 7. Block Addresses



Note: Also see Appendix A, Table 25 for a full listing of the Block Addresses

BUS OPERATIONS

There are 6 bus operations that control each memory. Each of these is described in this section, see Tables 4, Bus Operations, for a summary.

On Power-up or after a Hardware Reset the device defaults to Read Array mode (Page Read).

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the device and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Status Register, CFI and Block Protection Status) in the Command Interface.

A valid bus operation involves setting the desired address on the Address inputs, enabling the device (refer to Table 3), applying a Low signal, V_{IL}, to Output Enable and keeping Write Enable High, V_{IH}.

The Data Inputs/Outputs will output the value, see Figure 11, Bus Read AC Waveforms, and Table 16, Bus Read AC Characteristics, for details of when the output becomes valid.

Page Read. Page Read operations are used to read from several addresses within the same memory page.

Each memory page is a 4 Words or 8 Bytes and has the same A3-A23 (A2-A22 for LFBGA package). In x8 mode only A0, A1 and A2 may change, in x16 mode only A1 and A2 (A0 and A1 for LFBGA package) may change.

Valid bus operations are the same as Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. See Figure 12, Page Read AC Waveforms and Table 17, Page Read AC Characteristics for details on when the outputs become valid.

Bus Write. Bus Write operations write to the Command Interface in order to send commands to the device or to latch addresses and input data to program.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address Inputs and enabling the device (refer to Chip Enable section).

Both the Address Inputs and Data Input/Outputs are latched by the Command Interface on the rising edge of Write Enable or Chip Enable, whichever occurs first.

Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 13, and 14, Write AC Waveforms, and Tables 18 and 19, Write and Chip Enable Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when the Output Enable is High.

Standby. When Chip Enable is High, V_{IH}, the device enters Standby mode and the Data Inputs/Outputs pins are placed in the high impedance state regardless of Output Enable or Write Enable. The Supply Current is reduced to the Standby Supply Current, I_{DD1}.

During Program or Erase operations the device will continue to use the Program/Erase Supply Current, I_{DD3}, for Program or Erase operations until the operation completes.

Automatic Low Power. If there is no change in the state of the bus for a short period of time during Asynchronous Bus Read operations the device enters Auto Low Power mode where the internal Supply Current is reduced to the Auto-Standby Supply Current, I_{DD5}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Power-Down. The device is in Power-Down mode when Reset/Power-Down, $\overline{RP}$, is Low. The power consumption is reduced to the Power-Down level, I_{DD2}, and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Table 4. Bus Operations

Bus Operation	Memory Enabled	A23[3]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	Address Inputs	DQ0-DQ15 (x16) DQ0-DQ7 (x8)[1]
Bus Read	Upper	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High	Address	Data Output
	Lower	V_{IL}						
Page Read	Upper	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High	Address	Data Output
	Lower	V_{IL}						
Bus Write	Upper	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High	Address	Data Input
	Lower	V_{IL}						
Output Disable	Output disabled	X	V_{IL}	V_{IH}	V_{IH}	High	X	High Z
Standby	Device disabled	X	V_{IH}	X	X	High	X	High Z
Power-Down	Device disabled	X	X	X	X	V_{IL}	X	High Z

Note: 1. DQ8-DQ15 are High Z in x8 mode.
2. X = Don't Care V_{IL} or V_{IH}. High = V_{IH} or V_{HH}.
3. A22 for LFBGA package.

COMMAND INTERFACE

All Bus Write operations to the device are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. As the device contains two internal memories care must be taken to issue the commands to the correct address. Commands issued with A23 (A22 for LFBGA package) High will be addressed to the Upper Memory, commands issued with A23 (A22 for LFBGA) Low will be addressed to the Lower Memory.

The Commands are summarized in Table 5, Commands. Refer to Table 5 in conjunction with the text descriptions below.

After power-up or a Reset operation the device enters Read mode.

Read Memory Array Command. The Read Memory Array command is used to return the addressed internal memory to Read mode.

One Bus Write cycle is required to issue the Read Memory Array command and return the addressed internal memory to Read mode. Once the command is issued the internal memory remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory arrays. After power-up or a reset the device (both internal memories) defaults to Read Array mode (Page Read).

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Blocks Unprotect or Protection Register Program operation the device will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status or the Protection Register until another command is issued. Refer to Table 7, Read Electronic Signature, Tables 8 and 9, Word and Byte-wide Read Protection Register and Figure 8, Protection Register Memory Map for information on the addresses.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Tables 26, 27, 28, 29, 30 and 31 for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. As the device contains two Status Registers (one for each internal memory) the command must be issued to the same address as the previous operation (Block Erase, Write to Buffer, Word Program etc.). Once the command is issued subsequent Bus Read operations to the same internal memory (A23 (A22 for LFBGA) Low or A23 (A22 for LFBGA) High depending on where the command was issued to) read the Status Register until another command is issued. If the Bus Read operation is issued to the other internal memory, then the other Status Register will be read, giving the status of the last command issued in the other internal memory.

The Status Register information is present on the output data bus (DQ1-DQ7) when the device is enabled and Output Enable is Low, V_{IL}.

See the section on the Status Register and Table 11 for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. The command must be issued to the same address as the previous operation (Block Erase, Write to Buffer, Word Program etc.).

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect, Block Unprotect or Protection Register Program command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During Erase, the device being erased will only accept the Read Status Register and Program/Erase

Suspend commands, ignoring all other commands. The device not being erased will accept any command. Typical Erase times are given in Table 10.

See Appendix C, Figure 21, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Word/Byte Program Command. The Word/Byte Program command is used to program a single Word or Byte in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array. If the command is issued with A23 (A22 for LFBGA) High the Upper Memory will be programmed, if the command is issued with A23 (A22 for LFBGA) Low the Lower Memory will be programmed.

Up to 16 Words/32 Bytes can be loaded into the Write Buffer and programmed into the memory array. Each Write Buffer has the same A5-A23 (A4-A22 for LFBGA) addresses. In Byte-wide mode only A0-A4 may change, in Word-wide mode only A1-A4 (A0-A3 for LFBGA package) may change.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words/Bytes to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. The addresses must have the same A5-A22.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See Appendix C, Figure 19, Write to Buffer and Program Flowchart and Pseudo Code, for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It can be issued at any time during an Erase operation but will only be accepted during a Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. The command must be issued to the same address as the current Program or Erase operation. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the device will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing, it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Word Program, Write to Buffer and Program, and Program Suspend commands will also be accepted.

When one of the devices is being Program or Erase Suspended, any command issued to the other internal Flash memory will be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix C, Figure 20, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 22, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. The command must be issued to the same address as the Program/Erase Suspend command. Once the command is issued subsequent Bus Read operations read the Status Register.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the device will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command.

See Appendix C, Figure 23, Block Protect Flowchart and Pseudo Code, for a suggested flowchart on using the Block Protect command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. To unprotect all of the blocks in both of the internal memories the command must be issued to both memories, that is first with A23 (A22 for LFBGA) Low and then with A23 (A22 for LFBGA) High.

Four Bus Write cycles are required to issue the Blocks Unprotect command; the first two are written with A23 (A22 for LFBGA) Low, the second two are written with A23 (A22 for LFBGA) High. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Blocks Unprotect operation the device will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

See Appendix C, Figure 24, Blocks Unprotect Flowchart and Pseudo Code, for a suggested flowchart on using the Blocks Unprotect command.

Protection Register Program Command.

The Protection Register Program command is used to Program the 64 bit user segment of the Protection Register. Only the lower address Protection Register is available to the customer (A23 or A22 Low), the other Protection Register is reserved.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to ‘0’ (see Table 8 and x for Word-wide and Byte-wide protection addressing). Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to ‘0’ in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see Figure 8, Protection Register Memory Map. Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See Appendix C, Figure 25, Protection Register Program Flowchart and Pseudo Code, for the flowchart for using the Protection Register Program command.

Configure STS Command.

The Configure STS command is used to configure the Status/(Ready/Busy) pin. It has to be configured for both internal memories, that is the command has to be issued first with A23 (A22 for LFBGA) Low and then with A23 (A22 for LFBGA) High. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS

command (refer to Status/(Ready/Busy) section for more details.

Four Bus Write cycles are required to issue the Configure STS command. The first two cycles must be written with A23 (A22 for LFBGA) Low and the second two with A23 (A22 for LFBGA) High.

- The first bus cycle sets up the Configure STS command. A23 (A22 for LFBGA) must be Low.
- The second Bus Write cycle specifies one of the four possible configurations, A23 (A22 for LFBGA) must be Low, (refer to Table 6, Configuration Codes):
  - Ready/Busy mode
  - Pulse on Erase complete mode
  - Pulse on Program complete mode
  - Pulse on Erase or Program complete mode
- The third Bus Write cycle re-sets up the Configure STS command. This time A23 (A22 for LFBGA) must be High.
- The fourth re-specifies the configuration code given in the second Bus Write cycle. A23 (A22 for LFBGA) must be High.

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

The Configure STS command is not available with the LFBGA88 package.

Table 5. Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			Subsequent			Final		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	2	Write	RA	FFh	Read	RA	RD						
Read Electronic Signature(2)	≥ 2	Write	PA/BA	90h	Read	IDA	IDD						
Read Status Register	2	Write	PA/BA	70h	Read	PA/BA	SRD						
Read Query(2)	≥ 2	Write	PA/BA	98h	Read	QA	QD						
Clear Status Register	1	Write	PA/BA	50h									
Block Erase	2	Write	BA	20h	Write	BA	D0						
Word/Byte Program	2	Write	PA	40h/ 10h	Write	PA	PD						
Write to Buffer and Program	4+N	Write	BA	E8h	Write	BA	N	Write	PA	PD	Write	BA	D0h
Program/Erase Suspend	1	Write	PA/BA	B0h									
Program/Erase Resume	1	Write	PA/BA	D0h									
Block Protect	2	Write	BA	60h	Write	BA	01h						
Blocks Unprotect	4	Write	000000h	60h	Write	000000h	D0h	Write	400000h	60h	Write	400000h	D0h
Protection Register Program	2	Write	PRA	C0h	Write	PRA	PRD						
Configure STS command(3)	4	Write	000000h	B8h	Write	000000h	CC	Write	400000h	B8h	Write	400000h	CC

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address, PD Program Data, QA Query Address, QD Query Data, BA Any address in Block, PRA Protection register address, PRD Protection Register Data, CC Configuration Code.

2. A23 (A22 for LFBGA) selects which internal memory will enter Read Query or Read Electronic signature mode. To verify the block protection in the CFI BA has to be in the internal memory selected by A23 (A22 for LFBGA). To verify the protection of all memory blocks the command has to be issued with A23 (A22 for LFBGA) both High and Low.

3. Not available with LFBGA88 package.

Table 6. Configuration Codes

Configuration Code	DQ1	DQ2	Mode	STS Pin	Description
00h	0	0	Ready/Busy	V_{OL} during P/E operations Hi-Z when the memory is ready	The STS pin is Low during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
01h	0	1	Pulse on Erase complete	Pulse Low then High when operation completed(2)	Supplies a system interrupt pulse at the end of a Block Erase operation.
02h	1	0	Pulse on Program complete		Supplies a system interrupt pulse at the end of a Program operation.
03h	1	1	Pulse on Erase or Program complete		Supplies a system interrupt pulse at the end of a Block Erase or Program operation.

Note: 1. DQ2-DQ7 are reserved
2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 7. Read Electronic Signature

Code	Bus Width	Address Inputs (3)	Data (DQ15-DQ0)
Manufacturer Code	x8	000000h	20h
	x16		0020h
Device Code	x8	000001h	17h
	x16		8817h
Block Protection Status	x8	SBA(1)+02h	00h (Block Unprotected) 01h (Block Protected)
	x16		0000h (Block Unprotected) 0001h (Block Protected)
Protection Register	x8, x16	000080h(2)	PRD(1)

Note: 1. SBA is the Start Base Address of each block, PRD is Protection Register Data.
2. Base Address, refer to Figure 8 and Tables 8 and 9 for more information. A23 (A22 for LFBGA) must be Low to address the customer's Protection Register. The other Protection Register is reserved.
3. A1-A23 for TFBGA and TSOP; A0-A22 for LFBGA.

Figure 8. Protection Register Memory Map

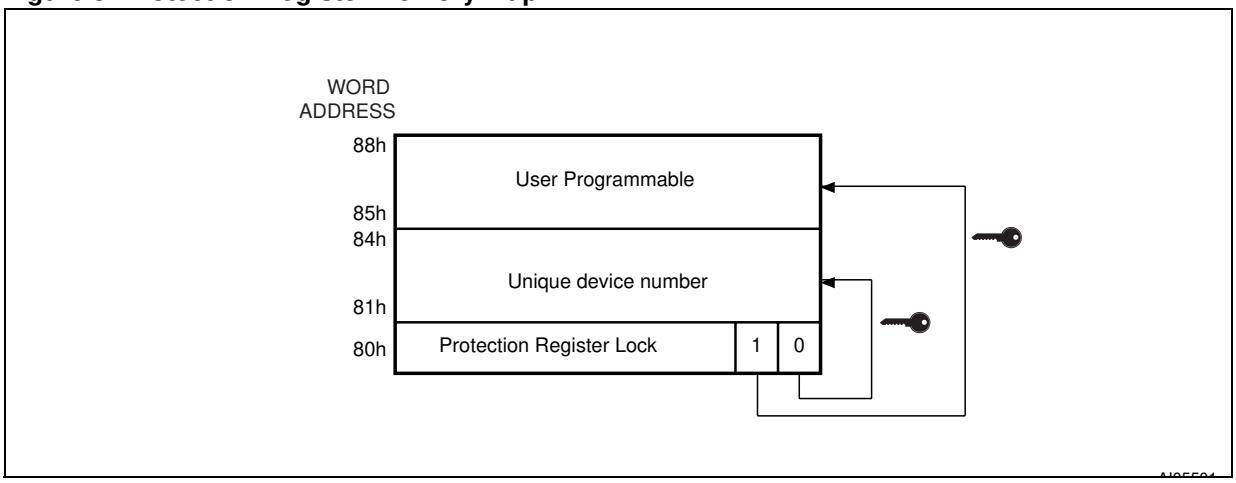


Table 8. Word-Wide Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	1	0
2	Factory (Unique ID)	1	0	0	0	0	0	1	1
3	Factory (Unique ID)	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Note: To read the Protection Register, A23 (A22 for LFBGA) must be V_{IL}.

Table 9. Byte-Wide Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	0	1
2	Factory (Unique ID)	1	0	0	0	0	0	1	0
3	Factory (Unique ID)	1	0	0	0	0	0	1	0
4	Factory (Unique ID)	1	0	0	0	0	0	1	1
5	Factory (Unique ID)	1	0	0	0	0	0	1	1
6	Factory (Unique ID)	1	0	0	0	0	1	0	0
7	Factory (Unique ID)	1	0	0	0	0	1	0	0
8	User	1	0	0	0	0	1	0	1
9	User	1	0	0	0	0	1	0	1
A	User	1	0	0	0	0	1	1	0
B	User	1	0	0	0	0	1	1	0
C	User	1	0	0	0	0	1	1	1
D	User	1	0	0	0	0	1	1	1
E	User	1	0	0	0	1	0	0	0
F	User	1	0	0	0	1	0	0	0

Note: To read the Protection Register, A23 must be V_{IL}.

Table 10. Program/Erase Times and Program/Erase Endurance Cycles

Parameters	M30LW128D			Unit
	Min	Typ(1,2)	Max(2)	
Block (1Mb) Erase		1.2	4.8(4)	s
Chip Program (Write to Buffer)		98	290(4)	s
Chip Erase Time		148	440 (4)	s
Program Write Buffer		192 (3)	576 (4)	µs
Word/Byte Program Time (Word/Byte Program command)		16	48 (4)	µs
Program Suspend Latency Time		1	20 (5)	µs
Erase Suspend Latency Time		1	25 (5)	µs
Block Protect Time		18	30 (5)	µs
Blocks Unprotect Time		0.75	1.2 (5)	s
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Effective byte programming time 6µs, effective word programming time 12µs.
4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.
5. Maximum value measured at worst case conditions for both temperature and V_{DD}.