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M34C02

2 Kbit Serial I²C Bus EEPROM For DIMM Serial Presence Detect

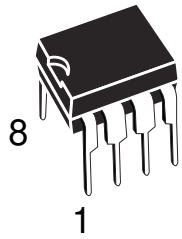
FEATURES SUMMARY

- Software Data Protection for lower 128 Bytes
- Two Wire I^2C Serial Interface
- 100kHz and 400kHz Transfer Rates
- Single Supply Voltage:
  - 2.5 to 5.5V up to 400kHz for M34C02-W
  - 2.2 to 5.5V up to 400kHz for M34C02-L
  - 1.8 to 5.5V up to 400kHz for M34C02-R
  - 1.7 to 3.6V up to 100kHz for M34C02-F
- BYTE and PAGE WRITE (up to 16 bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention
- Packages
  - ECOPACK® (RoHS compliant)

Table 1. Product List

Reference	Part Number
M34C02	M34C02-W
	M34C02-L
	M34C02-R
	M34C02-F

Figure 1. Packages



PDIP8 (BN)

TSSOP8 (DW)
169 mil width

TSSOP8 (DS)
3x3mm² body size (MSOP)

UFDFPN8 (MB)
2x3mm² (MLP)

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M34C02 is a 2Kbit serial EEPROM memory able to lock permanently the data in its first half (from location 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

This bottom half of the memory area can be write-protected using a specially designed software write protection mechanism. By sending the device a specific sequence, the first 128 Bytes of the memory become permanently write protected. Care must be taken when using this sequence as its effect cannot be reversed. In addition, the device allows the entire memory area to be write protected, using the $\overline{WC}$ input (for example by tieing this input to V_{CC}).

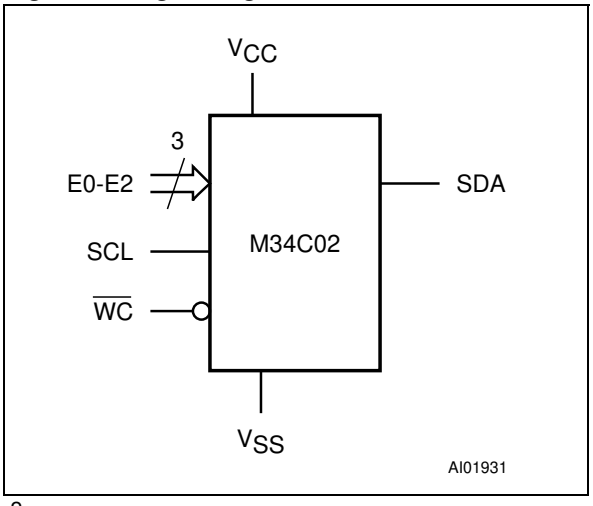
These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256x8 bits.

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.

ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. Logic Diagram

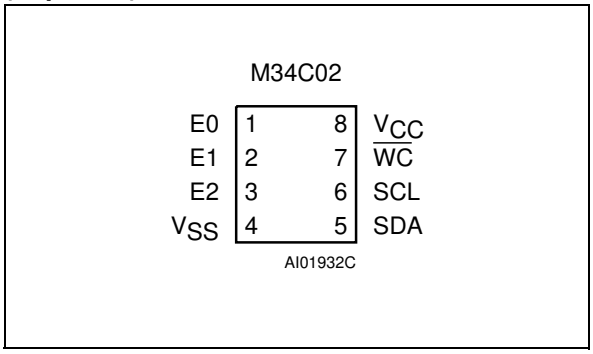


I^2C uses a two wire serial interface, comprising a bi-directional data line and a clock line. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition to access the memory area and a second Device Type Identifier Code (0110) to access the Protection Register. These codes are used together with three chip enable inputs (E2, E1, E0) so that up to eight 2Kbit devices may be attached to the I²C bus and selected individually.

The device behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R$\overline{W}$ bit (as described in Table 3.), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Figure 3. DIP, TSSOP and MLP Connections (Top View)



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

Table 2. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Device Internal Reset

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up (continuous rise up of VCC), the device will not respond to any instruction until the VCC has reached the Power On Reset threshold voltage (this threshold is lower than the minimum VCC operating voltage (as defined in Table 7. to Table 10.). When VCC has passed over the POR threshold, the device is reset and is in Standby Power mode.

Prior to selecting and issuing instructions to the memory, a valid and stable VCC voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At Power-down (continuous decay of VCC), as soon as VCC drops from the normal operating voltage, below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (Figure 5. indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

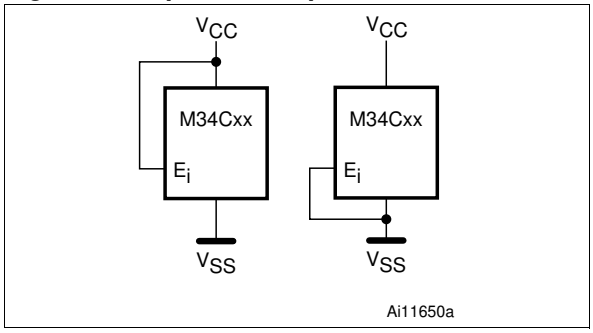
Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 5. indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS} to establish the Device Select Code.

Figure 4. Chip Enable input connection



Write Control ($\overline{WC}$)

This input signal is provided for protecting the contents of the whole memory from inadvertent write operations. Write Control ($\overline{WC}$) is used to enable (when driven Low) or disable (when driven High) write instructions to the entire memory area or to the Protection Register.

When Write Control ($\overline{WC}$) is tied Low or left unconnected, the write protection of the first half of the memory is determined by the status of the Protection Register.

Figure 5. Maximum RP Value versus Bus Parasitic Capacitance (C) for an I²C Bus

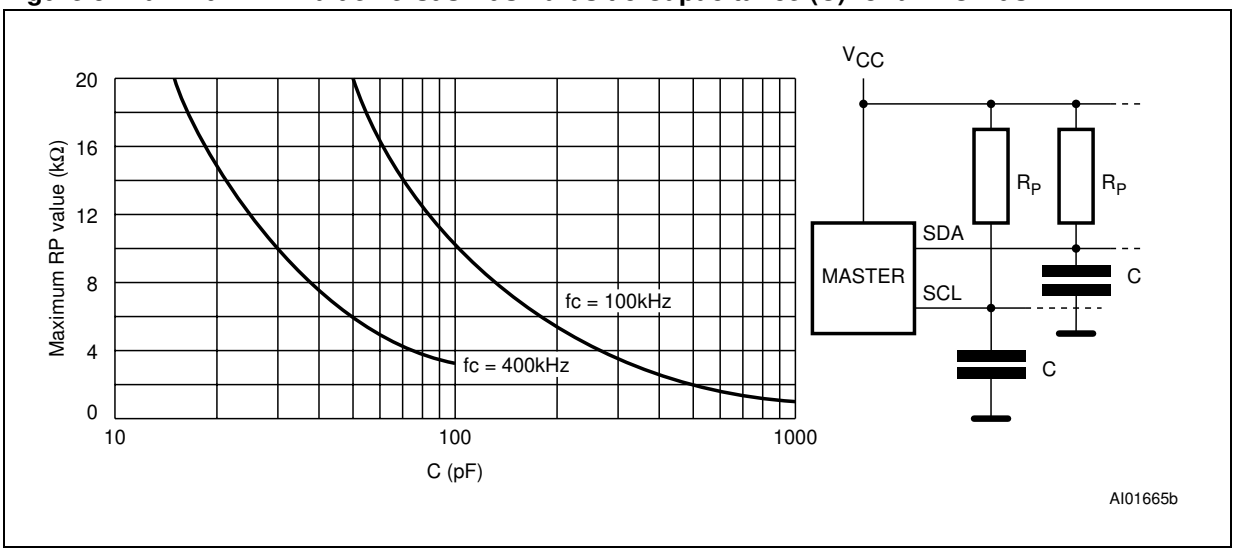


Figure 6. I²C Bus Protocol

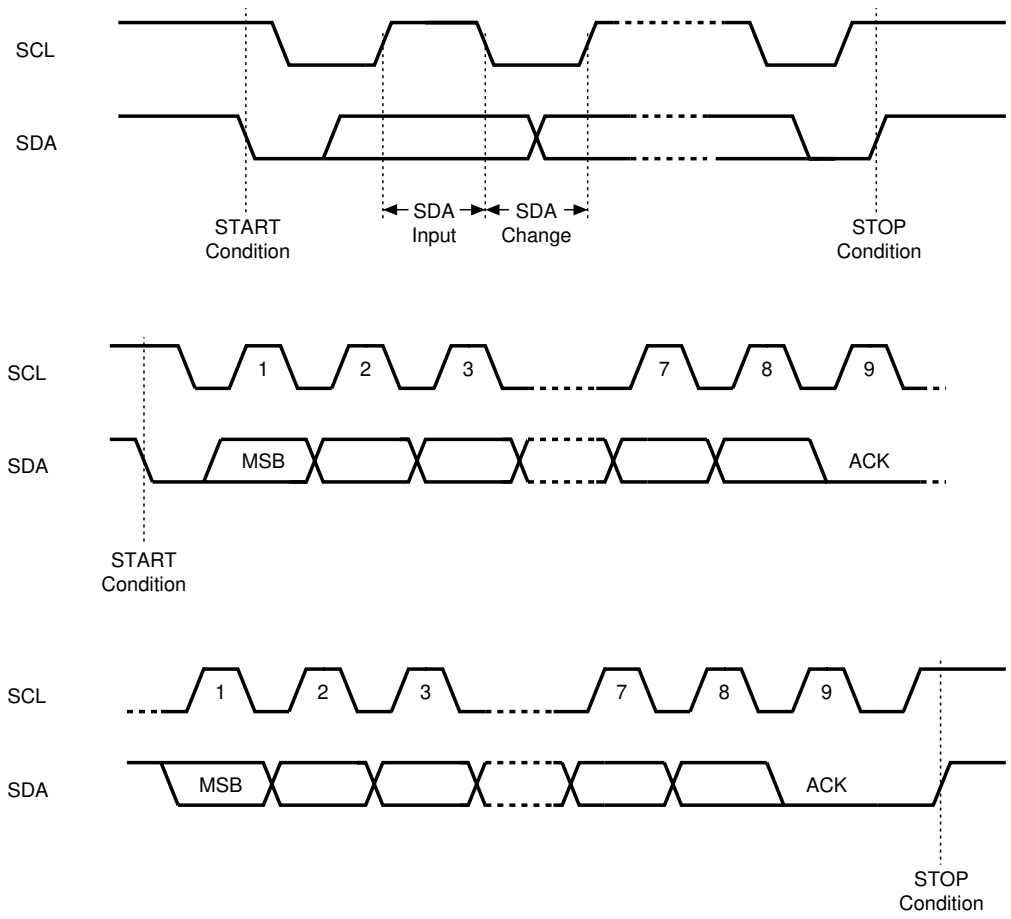


Table 3. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	R$\overline{W}$
Protection Register Select Code	0	1	1	0	E2	E1	E0	R$\overline{W}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

DEVICE OPERATION

The device supports the I^2C protocol. This is summarized in Figure 6.. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 3. (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to address the Protection Register, it is 0110b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

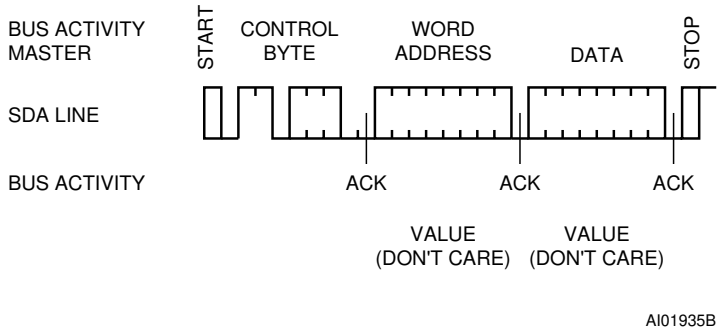
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	$\overline{WC}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, $R\overline{W}$ = 1
Random Address Read	0	X	1	START, Device Select, $R\overline{W}$ = 0, Address
	1	X		reSTART, Device Select, $R\overline{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $R\overline{W}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, $R\overline{W}$ = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 7. Setting the Write Protection Register ($\overline{WC}$ = 0)



Setting the Software Write-Protection

The M34C02 has a hardware write-protection feature, using the Write Control ($\overline{WC}$) signal. This signal can be driven High or Low, and must be held constant for the whole instruction sequence. When Write Control ($\overline{WC}$) is held Low, the whole memory array (addresses 00h to FFh) is write protected. When Write Control ($\overline{WC}$) is held High, the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 00h to 7Fh) to be permanently write protected irrespective of subsequent states of the Write Control ($\overline{WC}$) signal.

The write protection feature is activated by writing once to the Protection Register. The Protection Register is accessed with the device select code set to 0110b (as shown in Table 3.), and the E2, E1 and E0 bits set according to the states being applied on the E2, E1 and E0 signals. As for any other write command, Write Control ($\overline{WC}$) needs to be held Low. Address and data bytes must be sent with this command, but their values are all ignored, and are treated as Don't Care. Once the Protection Register has been written, the write protection of the first 128 Bytes of the memory is enabled, and it is not possible to unprotect these 128 Bytes, even if the device is powered off and on, and regardless the state of Write Control ($\overline{WC}$).

When the Protection Register has been written, the M34C02 no longer responds to the device type identifier 0110b in either read or write mode.

Figure 8. Result of Setting the Write Protection

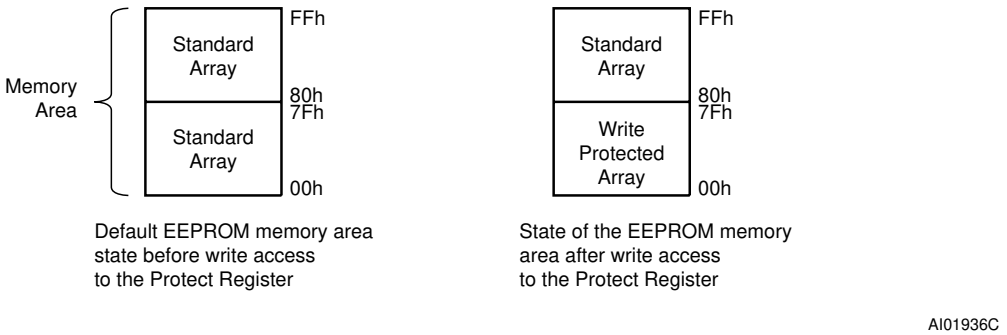
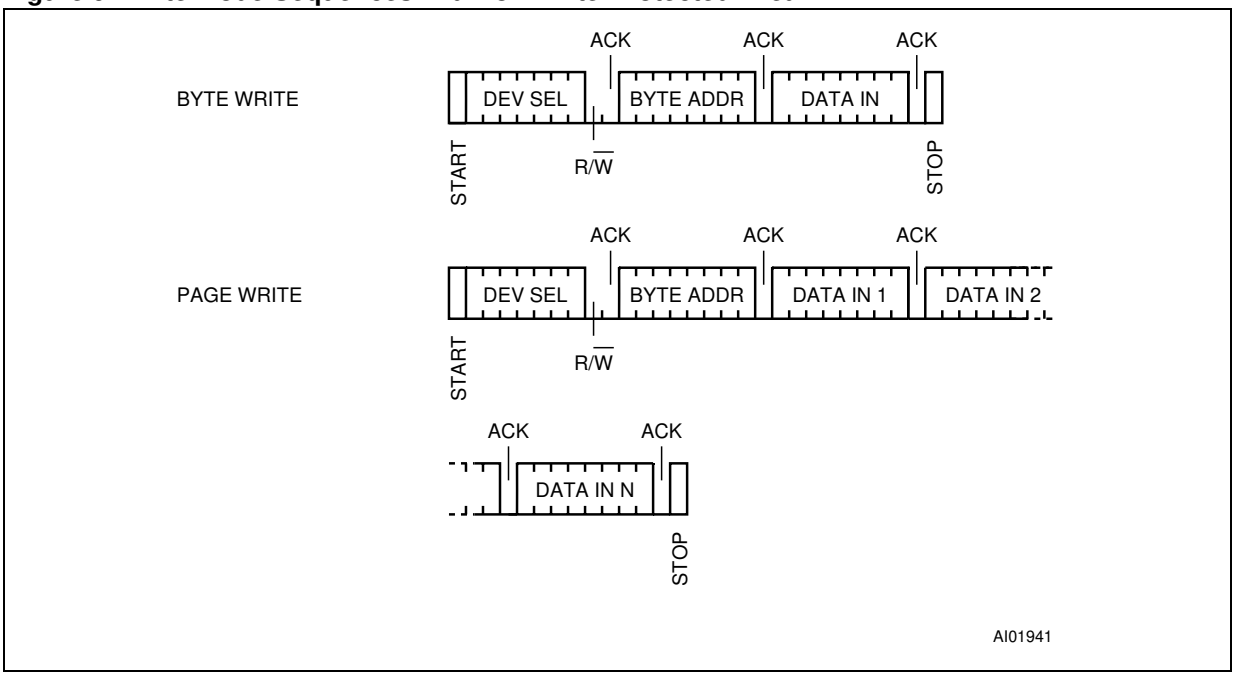


Figure 9. Write Mode Sequences in a Non Write-Protected Area



Write Operations

Following a Start condition the bus master sends a Device Select Code with the R$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 9., and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

Byte Write

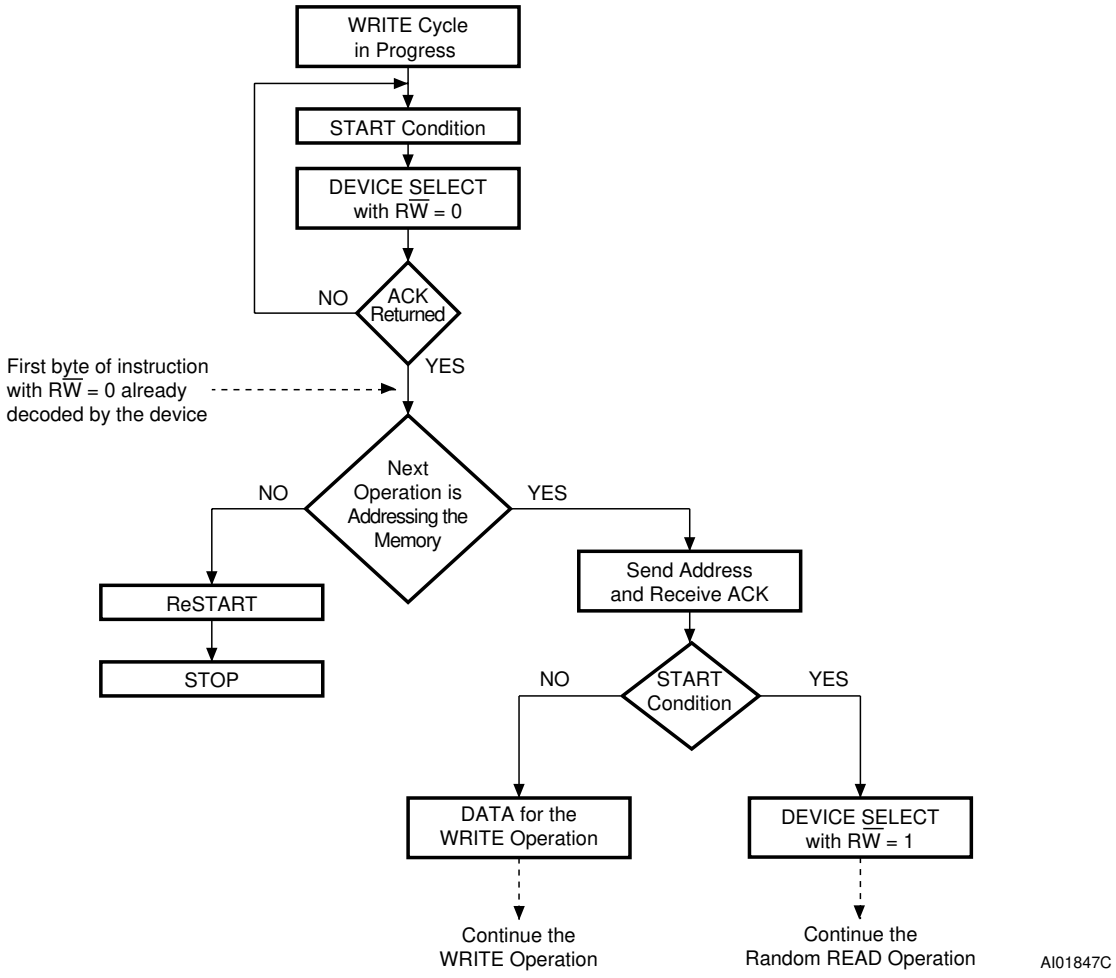
After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 9..

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 10. Write Cycle Polling Flowchart using ACK



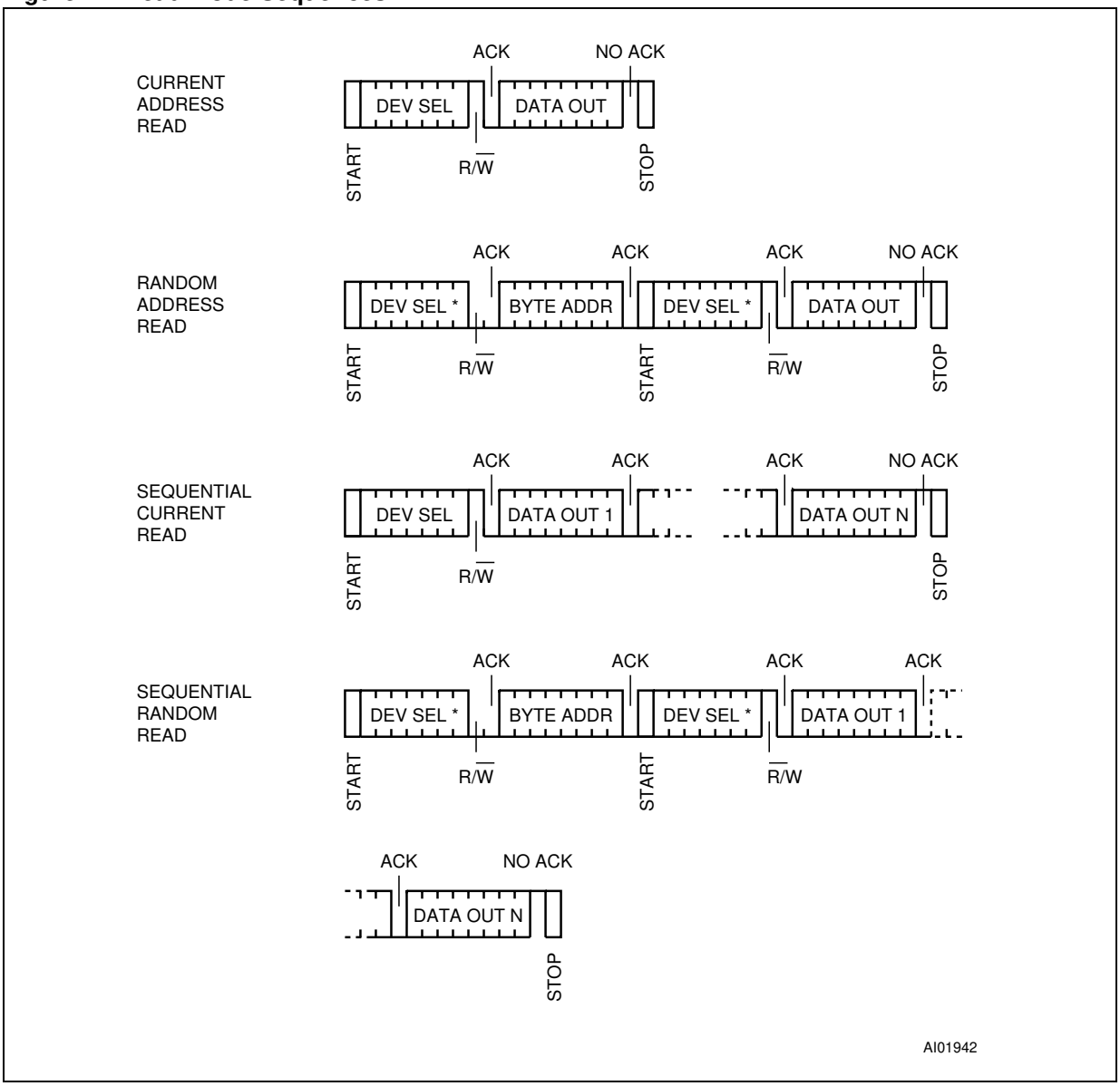
Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 17. and Table 18., but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 10., is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 11. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

Read Operations

Read operations are performed independently of whether hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 11.) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the RW bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 11., *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 11..

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

USE WITHIN A DRAM DIMM

In the application, the M34C02 is soldered directly in the printed circuit module. The 3 Chip Enable inputs (pins 1, 2 and 3) are wired at V_{CC} or V_{SS} through the DIMM socket (see Table 5.). The pull-up resistors needed for normal behavior of the I^2C bus are connected on the I^2C bus of the motherboard (as shown in Figure 12.).

The Write Control ($\overline{WC}$) of the M34C02 can be left unconnected. However, connecting it to V_{SS} is recommended, to maintain full read and write access.

Programming the M34C02

When the M34C02 is delivered, full read and write access is given to the whole memory array. It is recommended that the first step is to use the test equipment to write the module information (such as its access speed, its size, its organization) to the first half of the memory, starting from the first memory location. When the data has been validated, the test equipment can send a Write command to the Protection Register, using the device select code '01100000b' followed by an address and data byte (made up of Don't Care values) as shown in Figure 7.. The first 128 bytes of the memory area are then write-protected, and the M34C02 will no longer respond to the specific device select code '0110000xb'. It is not possible to reverse this sequence.

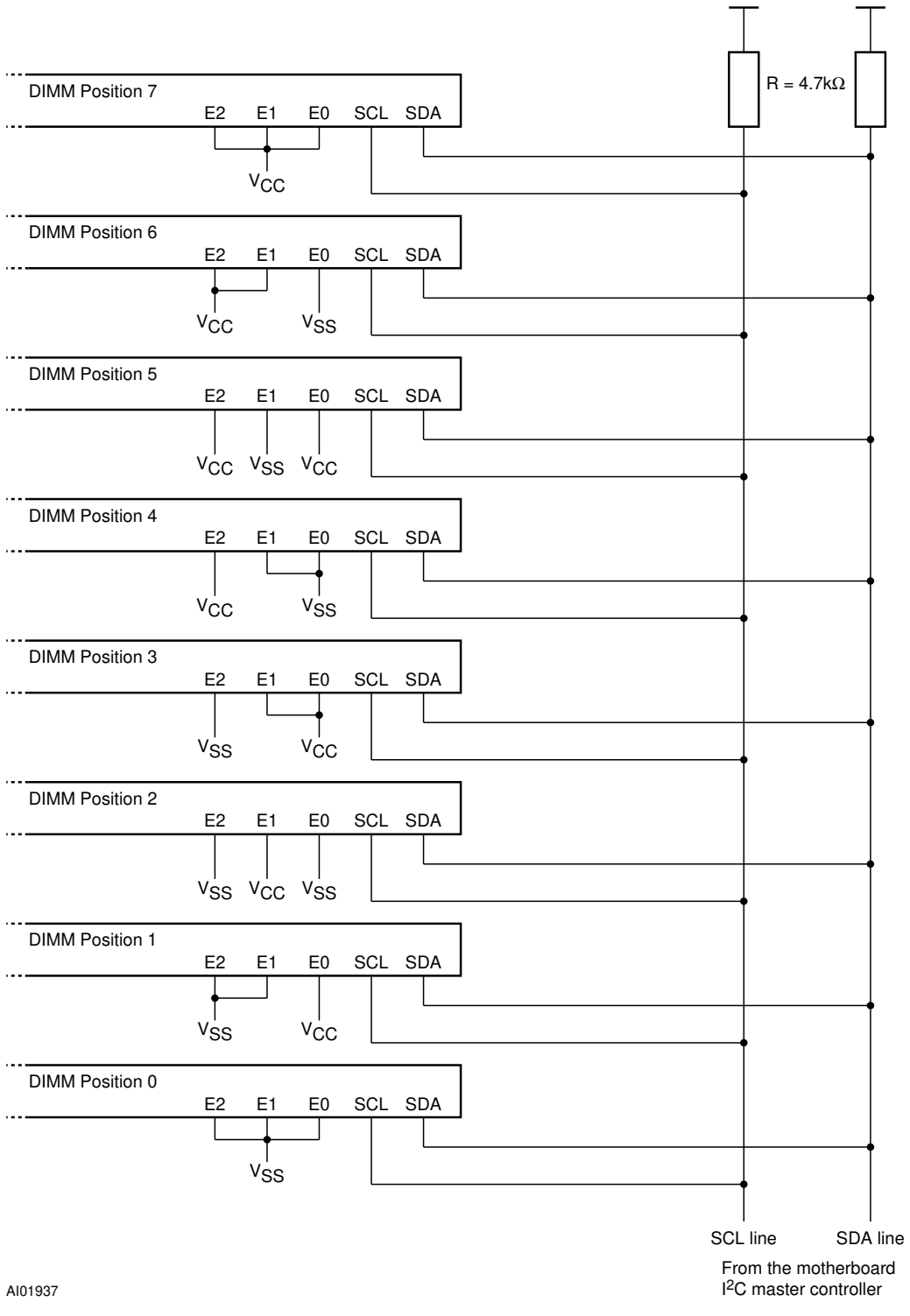
Table 5. DRAM DIMM Connections

DIMM Position	E2	E1	E0
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh).

Figure 12. Serial Presence Detect Block Diagram



Note: 1. E0, E1 and E2 are wired at each DIMM socket in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.
3. Pull-up resistors are required on all SDA and SCL bus lines (typically 4.7 kΩ) because these lines are open drain when used as outputs.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–40	90	°C
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering [1]	See Note: 1.		°C
V_{IO}	Input or Output Voltage	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–4000	4000	V

Note: 1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating Conditions (M34C02-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 8. Operating Conditions (M34C02-L)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.2	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 9. Operating Conditions (M34C02-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 10. Operating Conditions (M34C02-F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.7	3.6	V
T_A	Ambient Operating Temperature	0	70	°C

Table 11. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 13. AC Measurement I/O Waveform

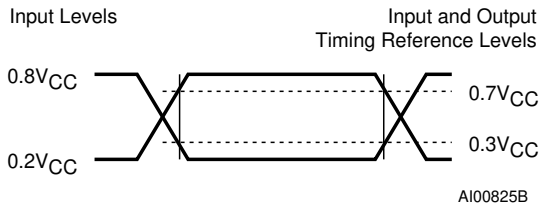


Table 12. Input Parameters

Symbol	Parameter[1,2]	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.3$ V	15	70	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. $T_A = 25°C$, f = 400kHz
2. Sampled only, not 100% tested.

Table 13. DC Characteristics (M34C02-W)

Symbol	Parameter	Test Condition (in addition to those in Table 7.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1,and E2)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		0.5	µA
V_{IL}	Input Low Voltage (1)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage (1)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Note: 1. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kOhm.

Table 14. DC Characteristics (M34C02-L)

Symbol	Parameter	Test Condition (in addition to those in Table 8.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		V_{CC} =2.2V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC} , 2.2V ≤ V_{CC} < 2.5V		0.5	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.3	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2.1mA, 2.2V ≤ V_{CC} < 2.5V		0.4	V

Table 15. DC Characteristics (M34C02-R)

Symbol	Parameter	Test Condition (in addition to those in Table 9.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1 and E2)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		V_{CC} =1.8V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC} , 1.8V ≤ V_{CC} < 2.5V		0.5	µA
V_{IL}	Input Low Voltage (1)	2.5V ≤ V_{CC} ≤ 5.5V	– 0.3	0.3 V_{CC}	V
		1.8V ≤ V_{CC} < 2.5V	– 0.3	0.25 V_{CC}	V
V_{IH}	Input High Voltage (1)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2.1mA, 2.2V ≤ V_{CC} < 2.5V		0.4	V
		I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Note: 1. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kOhm.

Table 16. DC Characteristics (M34C02-F)

Symbol	Parameter	Test Condition (in addition to those in Table 10.)	Min.[1]	Max.[1]	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1 and E2)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =1.7V, f_c=100kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 3.6V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC} , 1.7V ≤ V_{CC} < 2.5V		0.5	µA
V_{IL}	Input Low Voltage (2)	2.5V ≤ V_{CC} ≤ 3.6V	– 0.3	0.3 V_{CC}	V
		1.7V ≤ V_{CC} < 2.5V	– 0.3	0.25 V_{CC}	V
V_{IH}	Input High Voltage (2)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, 2.2V ≤ V_{CC} ≤ 3.6V		0.4	V
		I_{OL} = 0.15mA, V_{CC} = 1.7V		0.2	V

Note: 1. Preliminary Data.
2. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kOhm.

Table 17. AC Characteristics (M34C02-W, M34C02-L, M34C02-R)

Test conditions specified in Table 11. and Table 7. or Table 8.					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		10	ms

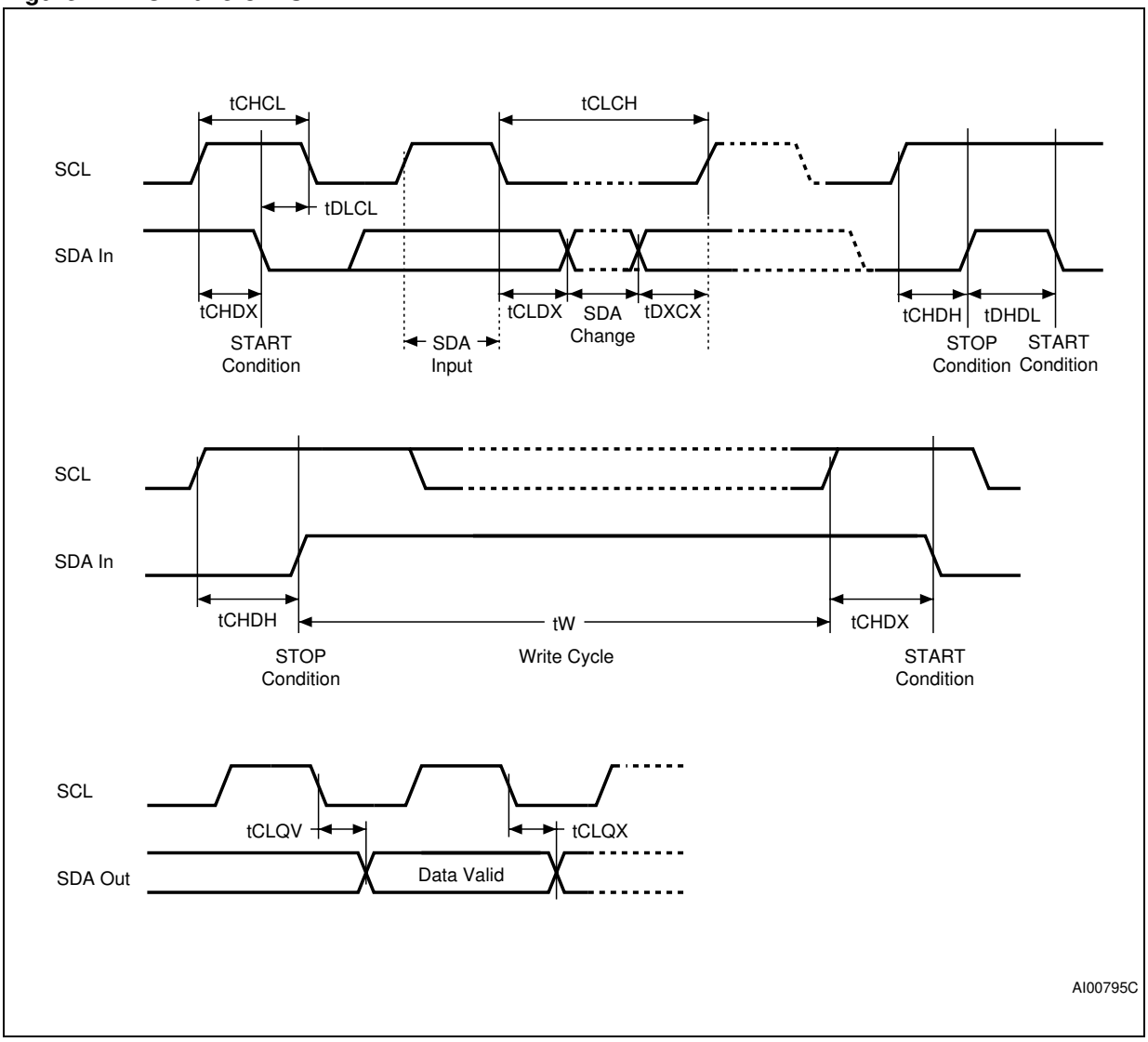
Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Table 18. AC Characteristics (M34C02-F)

Test conditions specified in Table 11. and Table 9. or Table 10.					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4000		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4700		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	250		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	3500	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	4700		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	4000		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	4000		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	4700		ns
t_W	t_{WR}	Write Time		10	ms

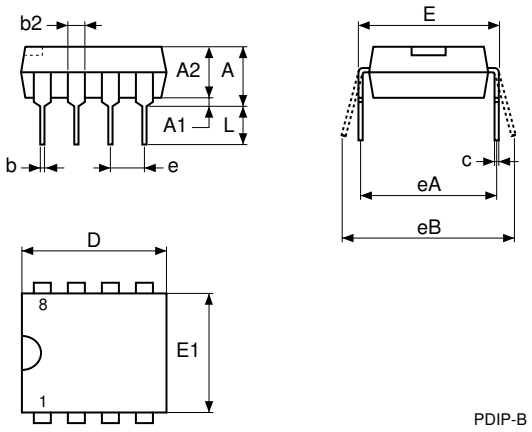
Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Figure 14. AC Waveforms



PACKAGE MECHANICAL

Figure 15. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline

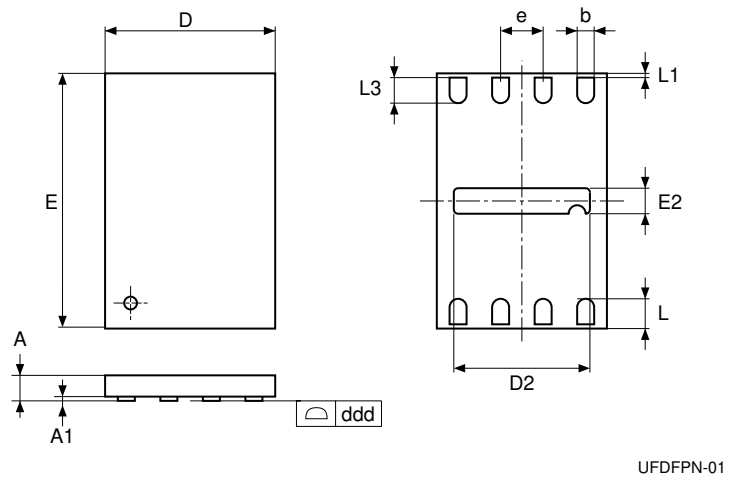


Note: Drawing is not to scale.

Table 19. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

Figure 16. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Package Outline

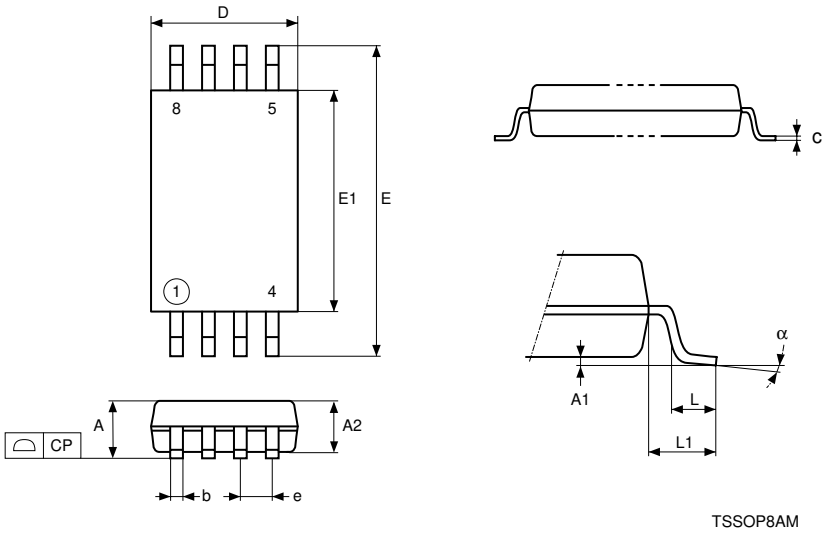


Note: 1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 20. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.55	0.50	0.60	0.022	0.020	0.024
A1		0.00	0.05		0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00			0.079		
D2		1.55	1.65		0.061	0.065
ddd			0.05			0.002
E	3.00			0.118		
E2		0.15	0.25		0.006	0.010
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	
N	8			8		

Figure 17. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline

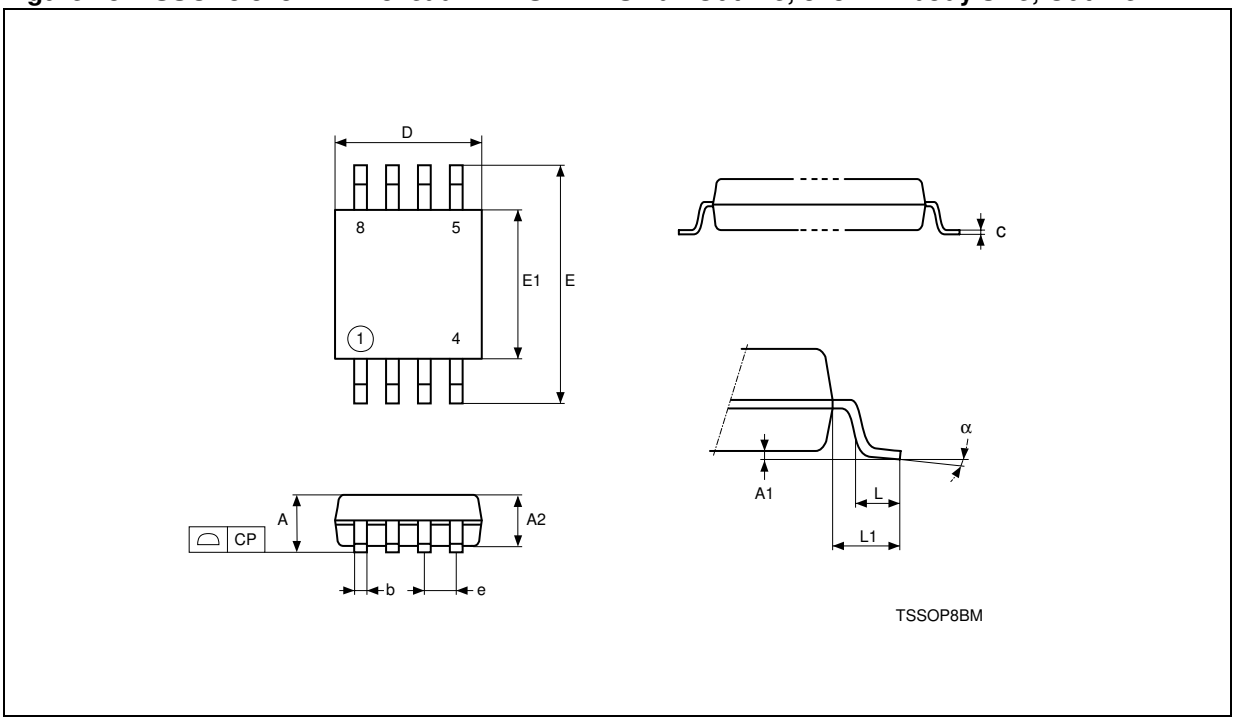


Note: Drawing is not to scale.

Table 21. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

Figure 18. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Outline



Note: Drawing is not to scale.

Table 22. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
CP			0.100			0.0039
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°