Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

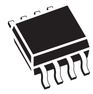
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

M34D64-W

64 Kbit serial I²C bus EEPROM with hardware write control on top quarter of memory

Features

- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltage:
  - 2.5 to 5.5 V for M34D64-W
- Hardware write control of the top quarter of memory
- byte and page write (up to 32 bytes)
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 000 000 Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)



SO8 (MN)
150 mil width

Contents

List of tables

List of figures

1 Description

The M34D64-W are I^2C-compatible electrically erasable programmable memory (EEPROM) devices organized as 8192 x 8 bits.

These devices are compatible with the I^2C memory protocol. This is a two-wire serial interface that uses a bidirectional databus and serial clock. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) (as described in *Table 2.: Device select code*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Figure 1. Logic diagram

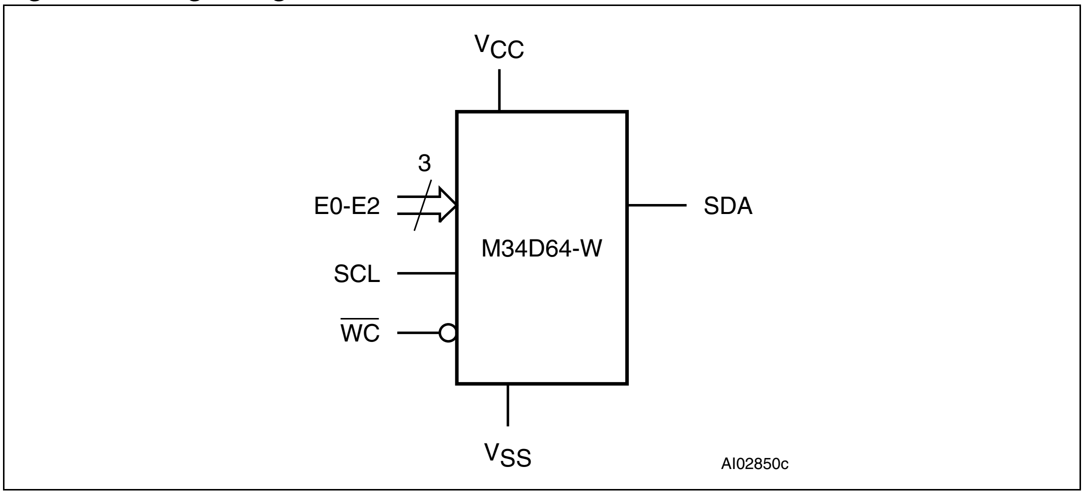
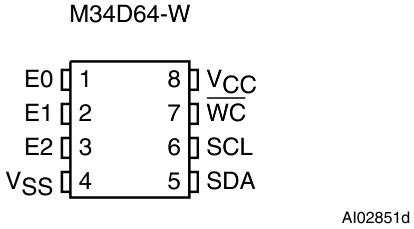


Table 1. Signal names

Signal name	Function	Direction
E0, E1, E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{\text{WC}}$	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. SO connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

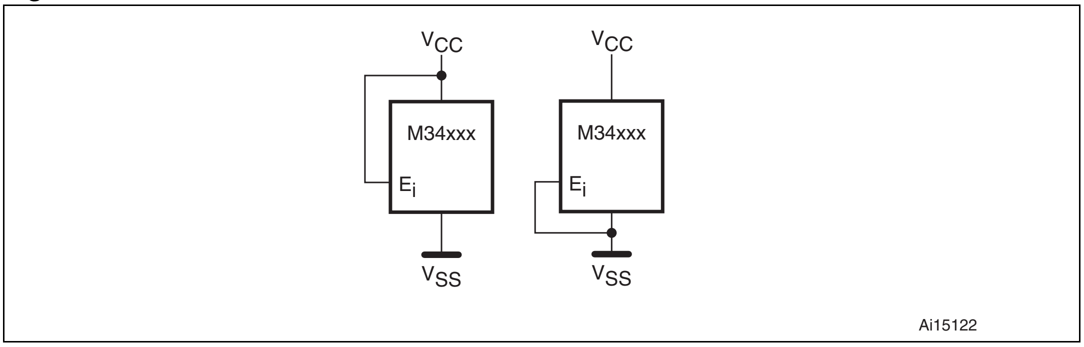
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0,0,0).

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the top quarter of the memory (as shown in *Figure 4*.) from inadvertent write. The Write Control signal is used to enable ($\overline{WC}$ = V_{IL}) or disable ($\overline{WC}$ = V_{IH}) write instructions to the top quarter of the memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 7*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}, the V_{CC} rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power-on-reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 7*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. It must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

Figure 4. Memory map showing write control area

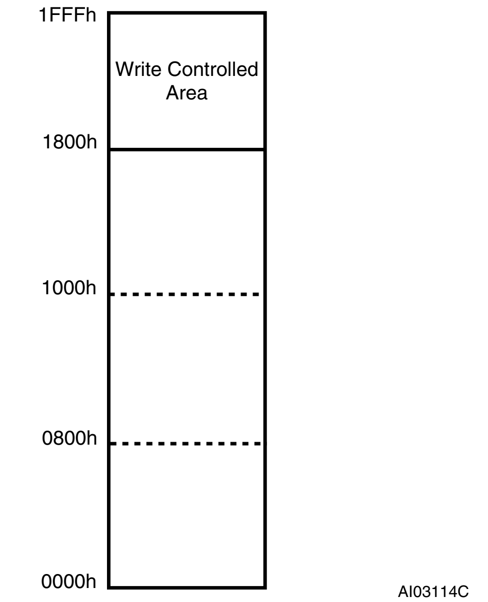


Figure 5. Maximum R_L value versus bus capacitance (C_{BUS}) for an I^2C bus

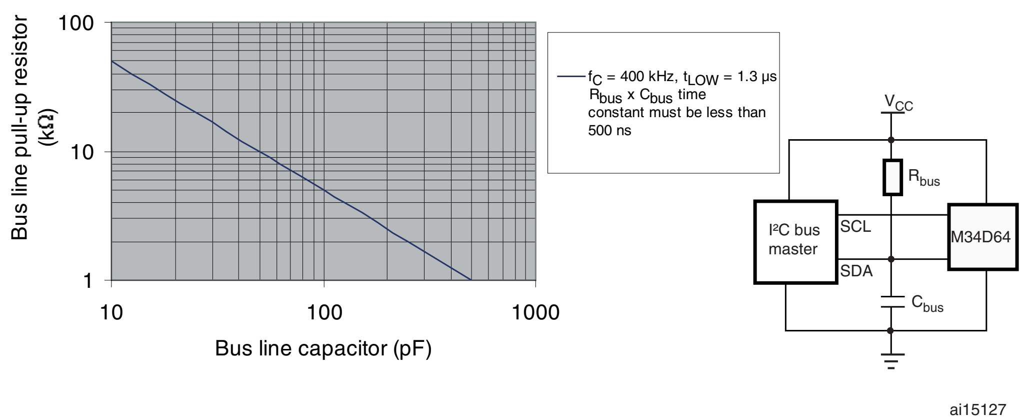


Figure 6. I^2C bus protocol

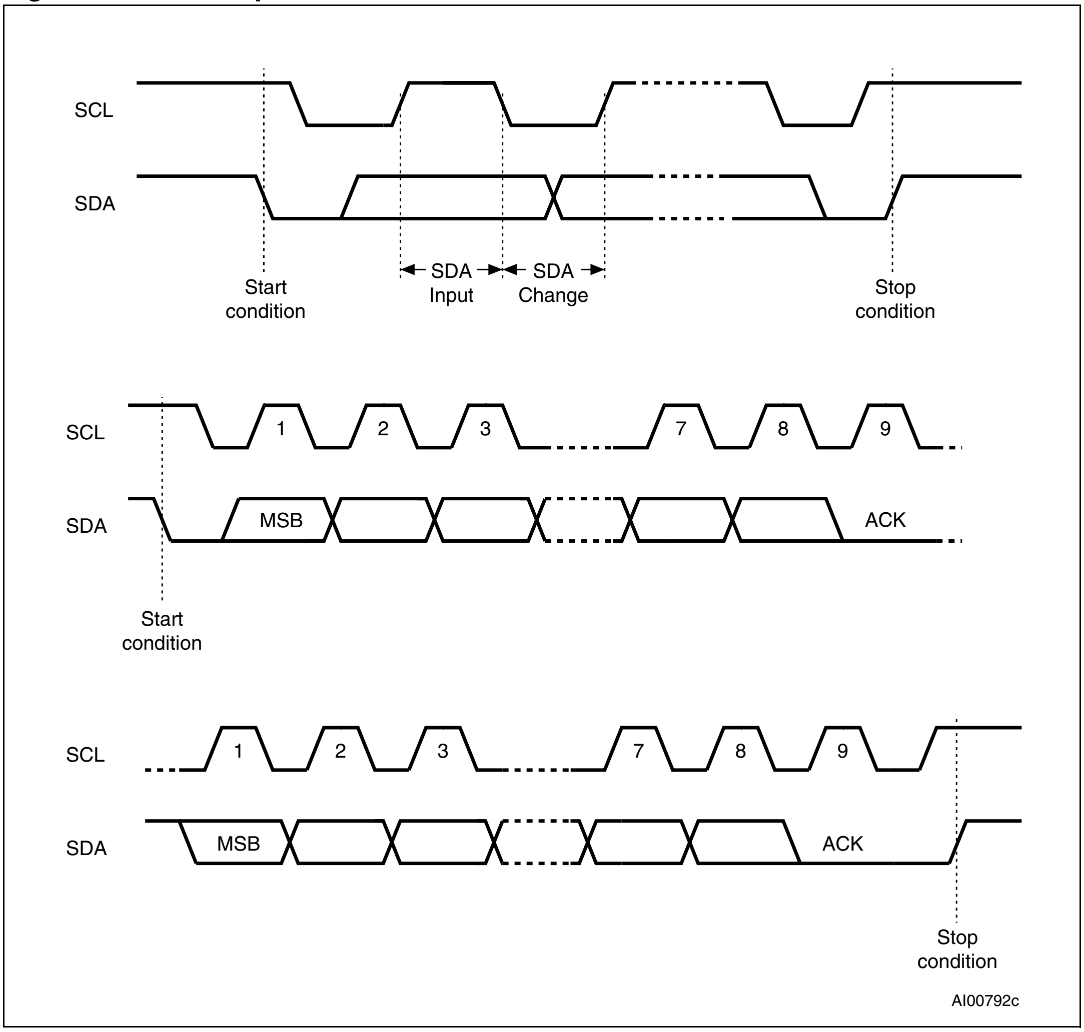


Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			RW̅
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	E0	RW̅

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 3. Most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 6.: I2C bus protocol*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M34D64-W device is always a slave in all communications.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in *Table 2.: Device select code* (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received on Serial Data (SDA), the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

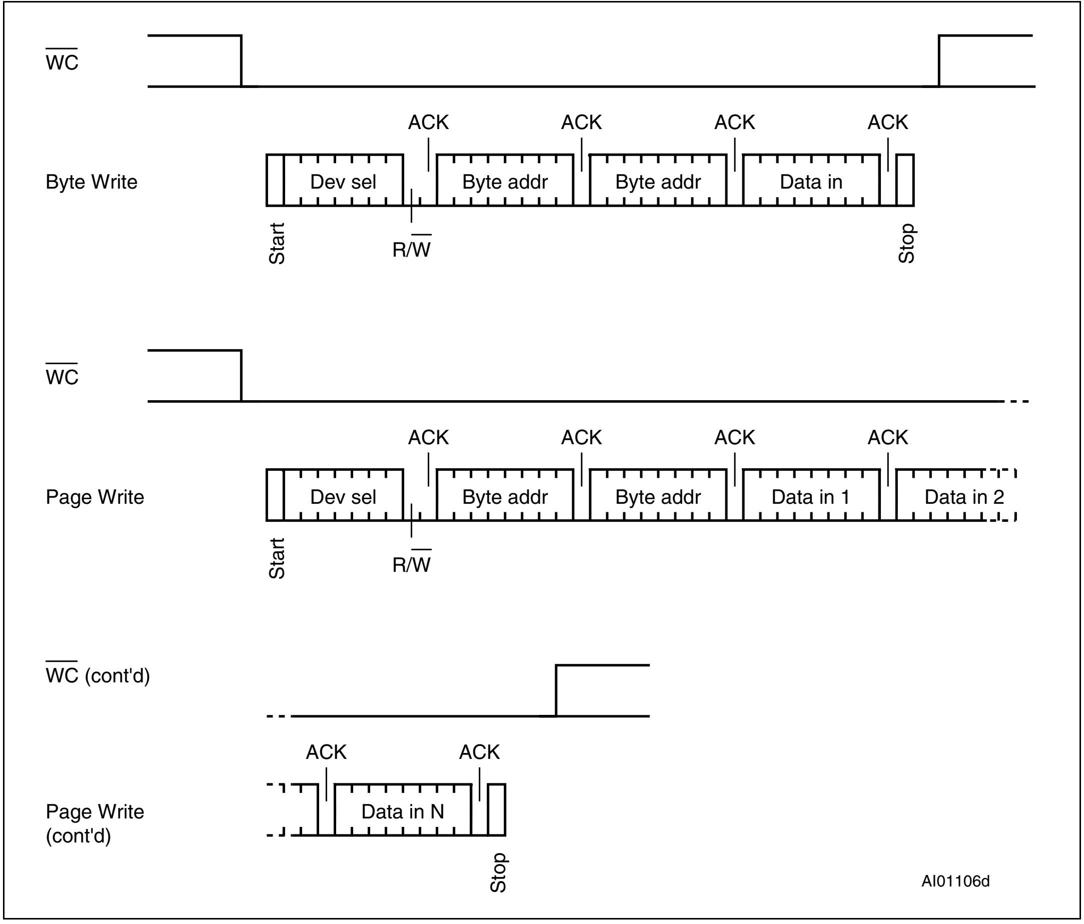
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Standby mode.

Table 5. Operating modes

Mode	$R\overline{W}$ bit	$\overline{WC}$ (1)	Bytes	Initial sequence
Current Address Read	1	X	1	Start, Device Select, $R\overline{W}$ = 1
Random Address Read	0	X	1	Start, Device Select, $R\overline{W}$ = 0, Address
	1	X		reStart, Device Select, $R\overline{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, Device Select, $R\overline{W}$ = 0
Page Write	0	V_{IL}	≤32	Start, Device Select, $R\overline{W}$ = 0

1. X = V_{IH} or V_{IL}.

Figure 7. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



3.6 Write operations

Following a Start condition the bus master sends a Device Select Code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) reset to 0. The device acknowledges this, as shown in *Figure 7.: Write mode sequences with WC = 0 (data write enabled)*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte(s).

Writing to the memory may be inhibited if Write Control ($\overline{\text{WC}}$) is driven high. Any Write instruction with Write Control ($\overline{\text{WC}}$) driven high (during a period of time from the Start condition until the end of the two address bytes) will not modify the contents of the top quarter of the memory.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 3.: Most significant byte*) is sent first, followed by the Least Significant Byte (*:*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal EEPROM Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

3.7 Byte Write

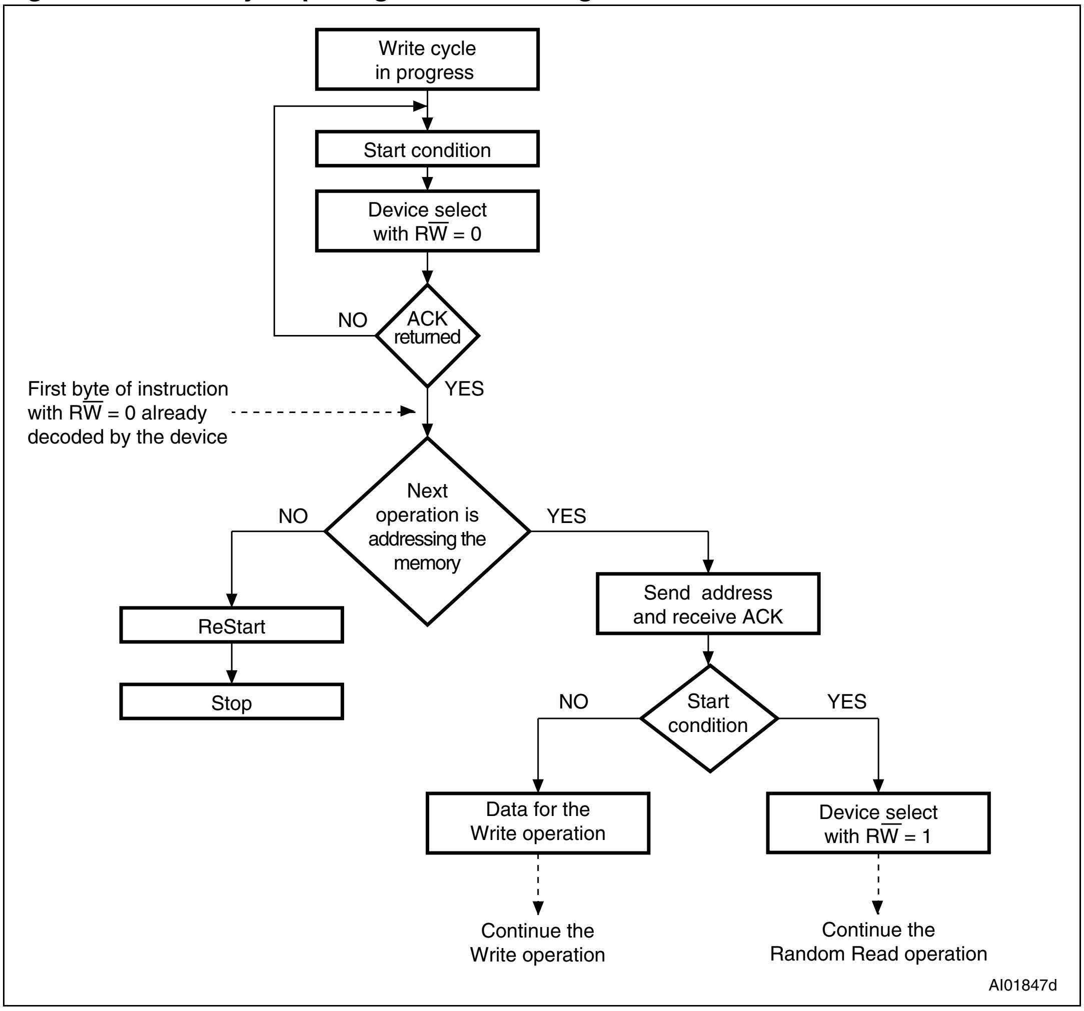
After the Device Select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected (top quarter of the memory), by Write Control ($\overline{WC}$) being driven high, the location is not modified. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7.: Write mode sequences with WC = 0 (data write enabled)*.

3.8 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b12-b5) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data. If Write Control ($\overline{WC}$) is high, the contents of the addressed top quarter of the memory location are not modified. After each byte is transferred, the internal byte address counter (the 5 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 8. Write cycle polling flowchart using ACK



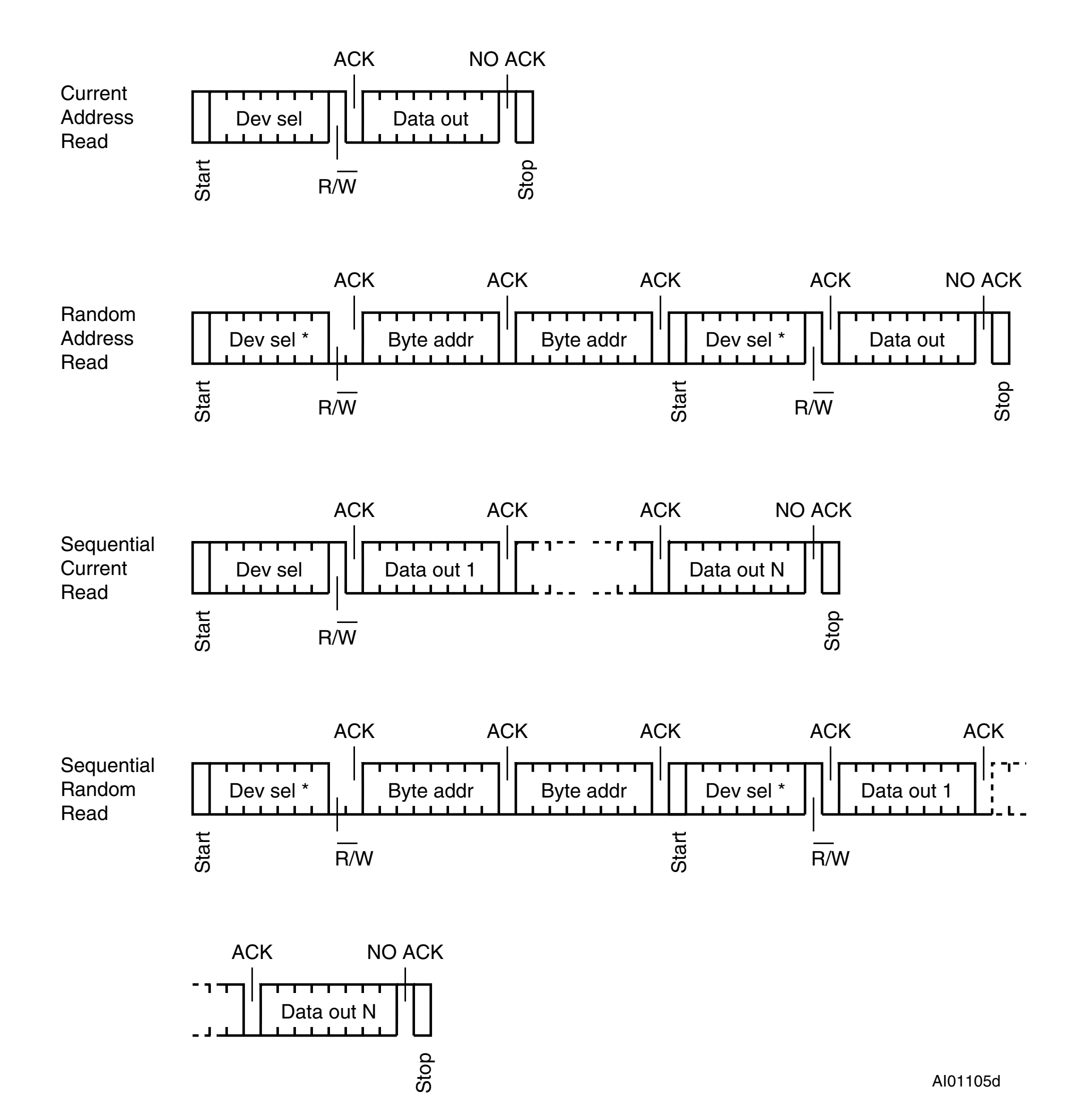
3.9 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 11.: AC characteristics*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8.: Write cycle polling flowchart using ACK*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Read mode sequences



1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

3.10 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

3.11 Random Address Read

A dummy Write is performed to load the address into the address counter (as shown in *Figure 9.: Read mode sequences*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the Read/$\overline{Write}$ bit (R$\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.12 Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9.: Read mode sequences*, *without* acknowledging the byte.

3.13 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9.: Read mode sequences*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.14 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9^{th} bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

4 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

5 Maximum rating

Stressing the device outside the ratings listed in *Table 6: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω)

6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC measurement I/O waveform

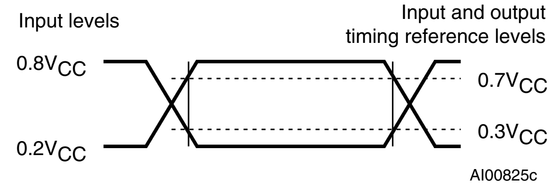


Table 9. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ input impedance	V_{IN} < 0.5 V	50	300	kΩ
Z_{WCH}	$\overline{WC}$ input impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (input filter on SCL and SDA)	Single glitch		100	ns

1. Sampled only, not 100% tested.

Table 10. DC characteristics

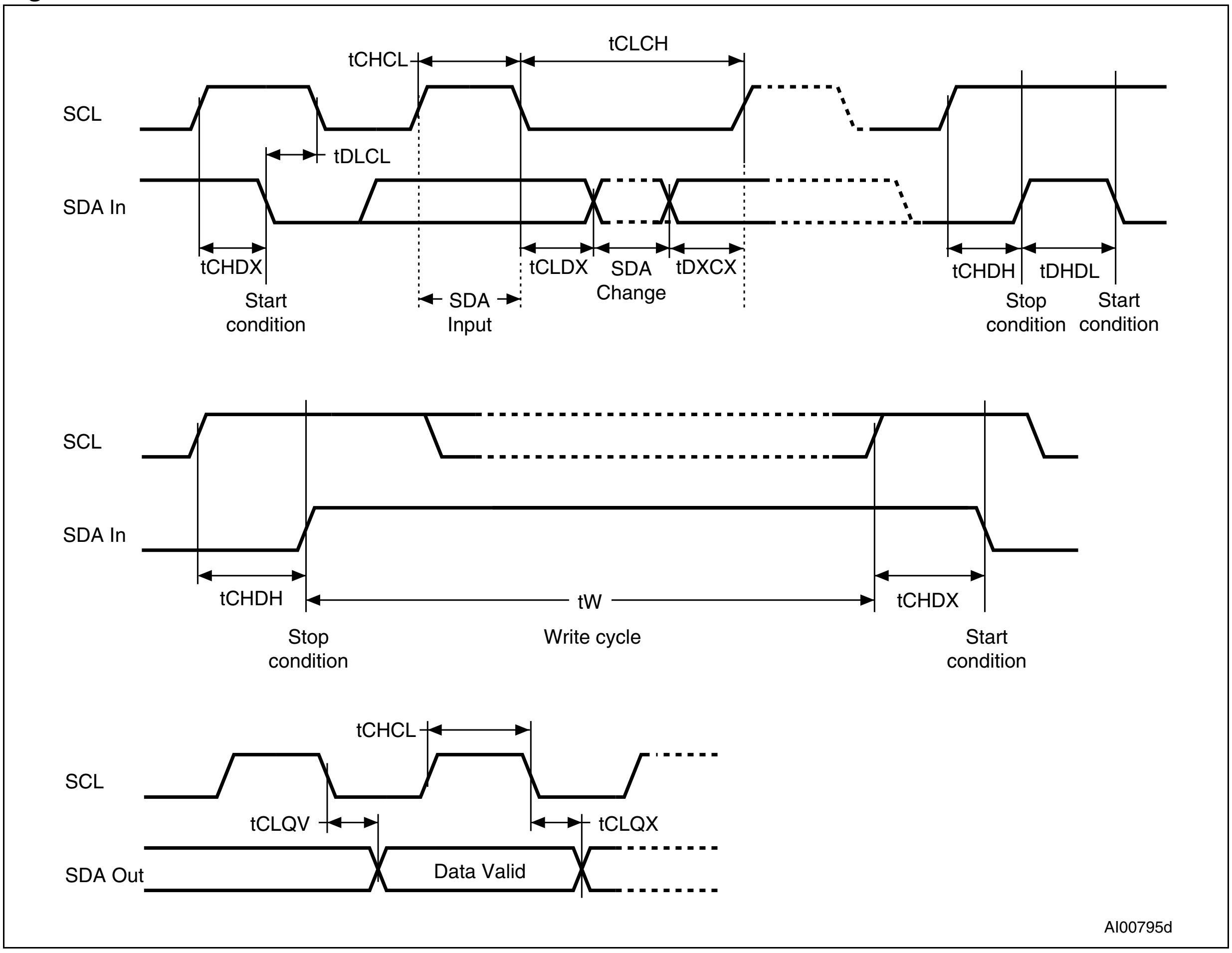
Symbol	Parameter	Test condition (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply current	$V_{CC} = 2.5$ V, $f_c = 400$ kHz (rise/fall time < 50 ns)		1	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} = 5$ V		10	µA
		$V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} = 2.5$ V		2	µA
V_{IL}	Input low voltage (E2, E1, E0, SCL, SDA)		–0.3	$0.3V_{CC}$	V
	Input low voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input high voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1$ mA, $V_{CC} = 2.5$ V		0.4	V

Table 11. AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
Test conditions specified in *Table 8.: AC measurement conditions* and *Table 7.: Operating conditions*					
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{CH1CH2}	t_R	Clock rise time		300	ns
t_{CL1CL2}	t_F	Clock fall time		300	ns
t_{DH1DH2}(1)	t_R	SDA rise time	20	300	ns
t_{DL1DL2}(1)	t_F	SDA fall time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}(2)	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDX}(3)	$t_{SU:STA}$	Start condition setup time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W	t_{WR}	Write time		5	ms

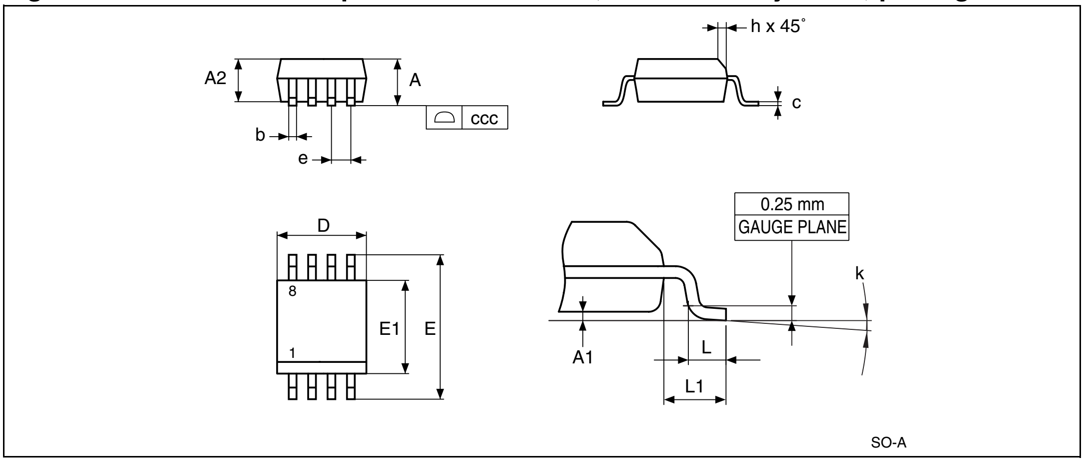
1. Sampled only, not 100% tested.
2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. For a reStart condition, or following a Write cycle.

Figure 11. AC waveforms



7 Package mechanical data

Figure 12. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 12. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Part numbering

Table 13. Ordering information scheme

Example:	M34D64	–	W	MN	6	T	P

Device type

M34 = I^2C application-specific standard product serial access EEPROM

Device function

64 = 64 Kbit (8192 × 8)

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

Package

MN = SO8 (150 mils width)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

P = ECOPACK® (RoHS compliant)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.