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M36W432T
M36W432B

32 Mbit (2Mb x16, Boot Block) Flash Memory and 4 Mbit (256K x16) SRAM, Multiple Memory Product

PRODUCT PREVIEW

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DDF} = 2.7V to 3.3V
  - V_{DDS} = V_{DDQF} = 2.7V to 3.3V
  - V_{PPF} = 12V for Fast Program (optional)
- ACCESS TIME: 70,85ns
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M36W432T: 88BAh
  - Bottom Device Code, M36W432B: 88BBh

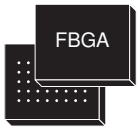
FLASH MEMORY

- 32 Mbit (2Mb x16) BOOT BLOCK
  - 8 x 4 KWord Parameter Blocks (Top or Bottom Location)
- PROGRAMMING TIME
  - 10µs typical
  - Double Word Programming Option
- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WPF}$ for Block Lock-Down
- AUTOMATIC STAND-BY MODE
- PROGRAM and ERASE SUSPEND
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- SECURITY
  - 64 bit user programmable OTP cells
  - 64 bit unique device identifier
  - One parameter block permanently lockable

SRAM

- 4 Mbit (256K x 16 bit)
- ACCESS TIME: 70ns
- LOW V_{DDS} DATA RETENTION: 1.5V
- POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS

Figure 1. Packages



Stacked LFBGA66 (ZA)
8 x 8 ball array

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SUMMARY DESCRIPTION

The M36W432 is a low voltage Multiple Memory Product which combines two memory devices; a 32 Mbit boot block Flash memory and a 4 Mbit SRAM. Recommended operating conditions do not allow both the Flash and the SRAM to be active at the same time.

The memory is offered in a Stacked LFBGA66 (0.8 mm pitch) package and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

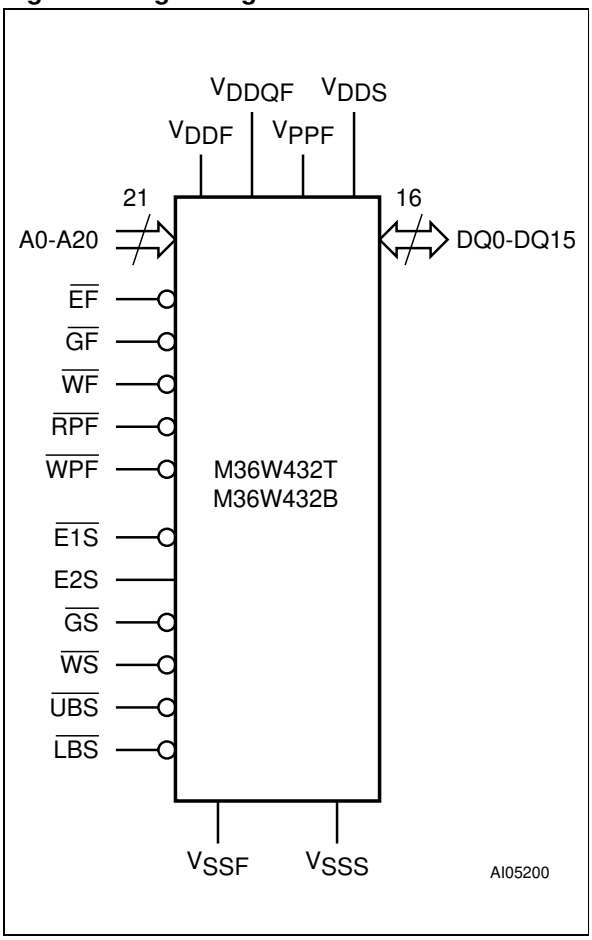
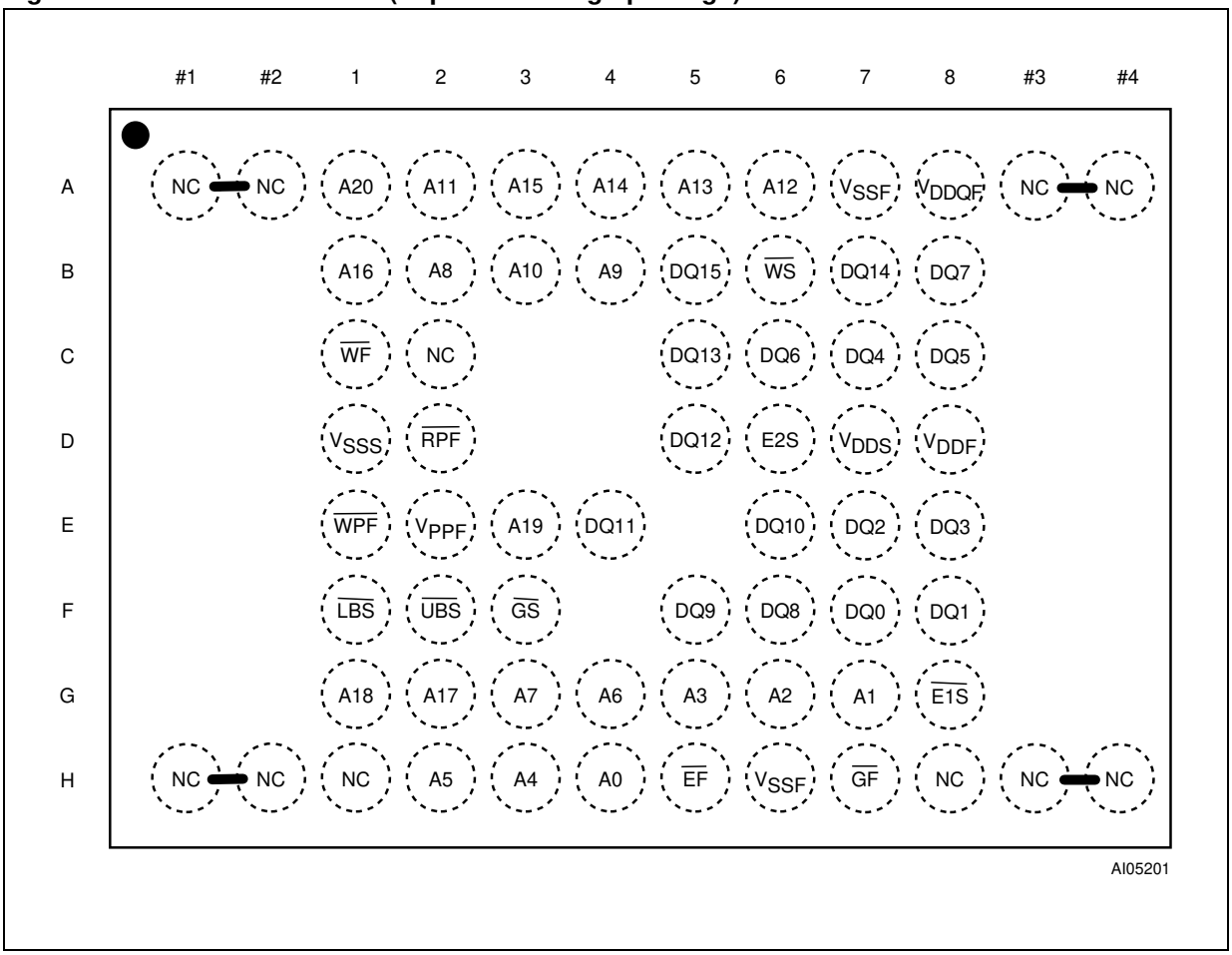


Table 1. Signal Names

A0-A17	Address Inputs
A18-A20	Address Inputs for Flash Chip only
DQ0-DQ15	Data Input/Output
V_{DDF}	Flash Power Supply
V_{DDQF}	Flash Power Supply for I/O Buffers
V_{PPF}	Flash Optional Supply Voltage for Fast Program & Erase
V_{SSF}	Flash Ground
V_{DDS}	SRAM Power Supply
V_{SSS}	SRAM Ground
NC	Not Connected Internally
Flash control functions	
$\overline{EF}$	Chip Enable input
$\overline{GF}$	Output Enable input
$\overline{WF}$	Write Enable input
$\overline{RPF}$	Reset input
$\overline{WPF}$	Write Protect input
SRAM control functions	
$\overline{E1S}$, E2S	Chip Enable inputs
$\overline{GS}$	Output Enable input
$\overline{WS}$	Write Enable input
$\overline{UBS}$	Upper Byte Enable input
$\overline{LBS}$	Lower Byte Enable input

Figure 3. LFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram and Table 1,Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A17). Addresses A0-A17 are common inputs for the Flash and the SRAM components. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable ($\overline{EF}$) and Write Enable ($\overline{WF}$) signals, while the SRAM is accessed through two Chip Enable signals ($\overline{E1S}$ and E2S) and the Write Enable signal ($\overline{WS}$).

Address Inputs (A18-A20). Addresses A18-A20 are inputs for the Flash component only. The Flash memory is accessed through the Chip Enable ($\overline{EF}$) and Write Enable ($\overline{WF}$) signals

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

Flash Chip Enable ($\overline{EF}$). The Chip Enable input activates the Flash memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

Flash Output Enable ($\overline{GF}$). The Output Enable controls the data outputs during the Bus Read operation of the Flash memory.

Flash Write Enable ($\overline{WF}$). The Write Enable controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable, $\overline{EF}$, or Write Enable, $\overline{WF}$, whichever occurs first.

Flash Write Protect ($\overline{WPF}$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the block cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the block can be locked or unlocked. (refer to Table 6, Read Protection Register and Protection Register Lock).

Flash Reset ($\overline{RPF}$). The Reset input provides a hardware reset of the Flash memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is minimized. After Reset all blocks are in the Locked state. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters read array mode, but a negative transition of Chip Enable or a change of the address is required to ensure valid data outputs.

SRAM Chip Enable (E1S, E2S). The Chip Enable inputs activate the SRAM memory control logic, input buffers and decoders. E1S at V_{IH} or E2S at V_{IL} deselects the memory and reduces the power consumption to the standby level. E1S and E2S can also be used to control writing to the SRAM memory array, while $\overline{WS}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL}, E1S at V_{IL} and E2S at V_{IH} at the same time.

SRAM Write Enable ($\overline{WS}$). The Write Enable input controls writing to the SRAM memory array. $\overline{WS}$ is active low.

SRAM Output Enable ($\overline{GS}$). The Output Enable gates the outputs through the data buffers during a read operation of the SRAM memory. $\overline{GS}$ is active low.

SRAM Upper Byte Enable ($\overline{UBS}$). The Upper Byte Enable enables the upper bytes for SRAM (DQ8-DQ15). $\overline{UBS}$ is active low.

SRAM Lower Byte Enable ($\overline{LBS}$). The Lower Byte Enable enables the lower bytes for SRAM (DQ0-DQ7). $\overline{LBS}$ is active low.

V_{DDF} Supply Voltage (2.7V to 3.3V). V_{DDF} provides the power supply to the internal core of the Flash Memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQF} and V_{DDS} Supply Voltage (2.7V to 3.3V). V_{DDQF} provides the power supply for the Flash memory I/O pins and V_{DDS} provides the power supply for the SRAM control pins. This allows all Outputs to be powered independently from the Flash core power supply, V_{DDF}. V_{DDQF} can be tied to V_{DDS}

V_{PPF} Program Supply Voltage. V_{PPF} is both a control input and a power supply pin for the Flash memory. The two functions are selected by the voltage range applied to the pin. The Supply Voltage V_{DDF} and the Program Supply Voltage V_{PPF} can be applied in any order.

If V_{PPF} is kept in a low voltage range (0V to 3.6V) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PPF} > V_{PPLK}$ enables these functions (see Table 14, DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range 11.4V to 12.6V it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed (see Table 16 and 17).

V_{SSF} and V_{SSS} Ground. V_{SSF} and V_{SSS} are the ground reference for all voltage measurements in the Flash and SRAM chips, respectively.

Note: Each device in a system should have V_{DDF}, V_{DDQF} and V_{PPF} decoupled with a 0.1µF capacitor close to the pin. See Figure 9, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The Flash and SRAM components have separate power supplies and grounds and are distinguished by three chip enable inputs: $\overline{E}$F for the Flash memory and, $\overline{E}$1S and E2S for the SRAM.

Recommended operating conditions do not allow both the Flash and the SRAM to be in active mode at the same time. The most common example is simultaneous read operations on the Flash and the SRAM which would result in a data bus contention. Therefore it is recommended to put the SRAM in the high impedance state when reading the Flash and vice versa (see Table 2 Main Operation Modes for details).

Figure 4. Functional Block Diagram

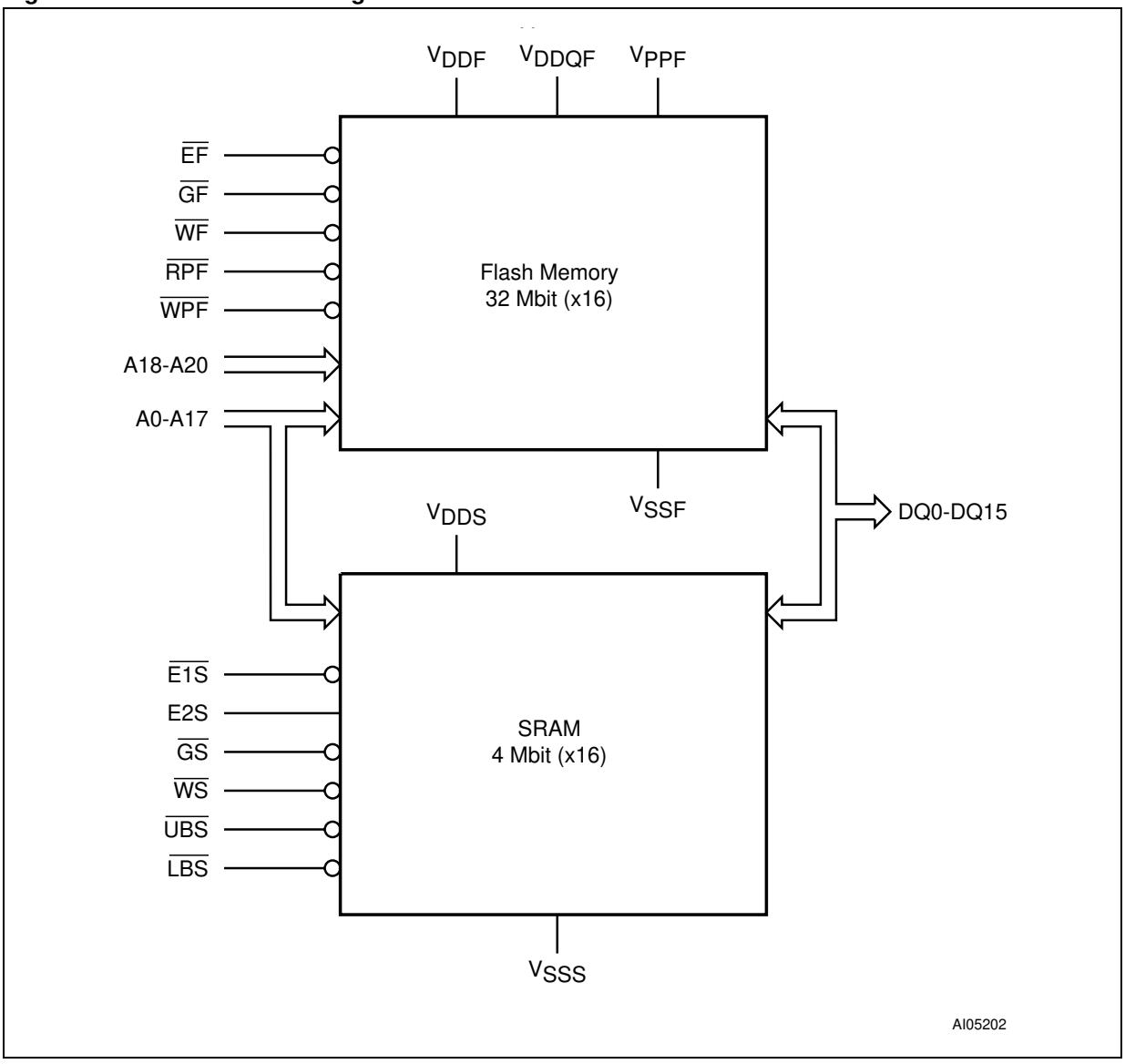


Table 2. Main Operation Modes

Operation Mode		$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	$\overline{RPF}$	$\overline{WPF}$	V_{PPF}	$\overline{E1S}$	E2S	$\overline{GS}$	$\overline{WS}$	$\overline{UBS}$, $\overline{LBS}$ (1)	DQ15-DQ0
Flash Memory	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Don't care	SRAM must be disabled					Data Output
	Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{DDF} or V_{PPFH}	SRAM must be disabled					Data Input
	Block Locking	V_{IL}	X	X	V_{IH}	V_{IL}	Don't care	SRAM must be disabled					X
	Standby	V_{IH}	X	X	V_{IH}	X	Don't care	Any SRAM mode is allowed					Hi-Z
	Reset	X	X	X	V_{IL}	X	Don't care	Any SRAM mode is allowed					Hi-Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Don't care	Any SRAM mode is allowed					Hi-Z
SRAM	Read	Flash must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data out Word Read
	Write	Flash must be disabled						V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data in Word Write
	Standby/ Power Down	Any Flash mode is allowable						V_{IH}	X	X	X	X	Hi-Z
								X	V_{IL}	X	X	X	Hi-Z
								X	X	X	X	V_{IH}	Hi-Z
	Data Retention	Any Flash mode is allowable						V_{IH}	X	X	X	X	Hi-Z
								X	V_{IL}	X	X	X	Hi-Z
								X	X	X	X	V_{IH}	Hi-Z
	Output Disable	Any Flash mode is allowable						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PPFH} = 12V ± 5%.

1. If $\overline{UBS}$ and $\overline{LBS}$ are tied together the bus is at 16 bit. For an 8 bit bus configuration use $\overline{UBS}$ and $\overline{LBS}$ separately.

Flash Memory Component

The Flash Memory is a 32 Mbit (2 Mbit x 16) device that can be erased electrically at the block level and programmed in-system on a Word-by-Word basis. These operations can be performed using a single low voltage (2.7 to 3.3V) supply and the V_{DDQF} for device I/0 operation feature the same voltage range. An optional 12V V_{PPF} power supply is provided to speed up customer programming.

The device features an asymmetrical blocked architecture with an array of 71 blocks: 8 Parameter Blocks of 4 KWord and 63 Main Blocks of 32 KWord. The M36W432T device has the Flash Memory Parameter Blocks at the top of the memory address space while the M36W432B device locates the Parameter Blocks starting from the bottom. The memory maps are shown in Figure 5, Block Addresses.

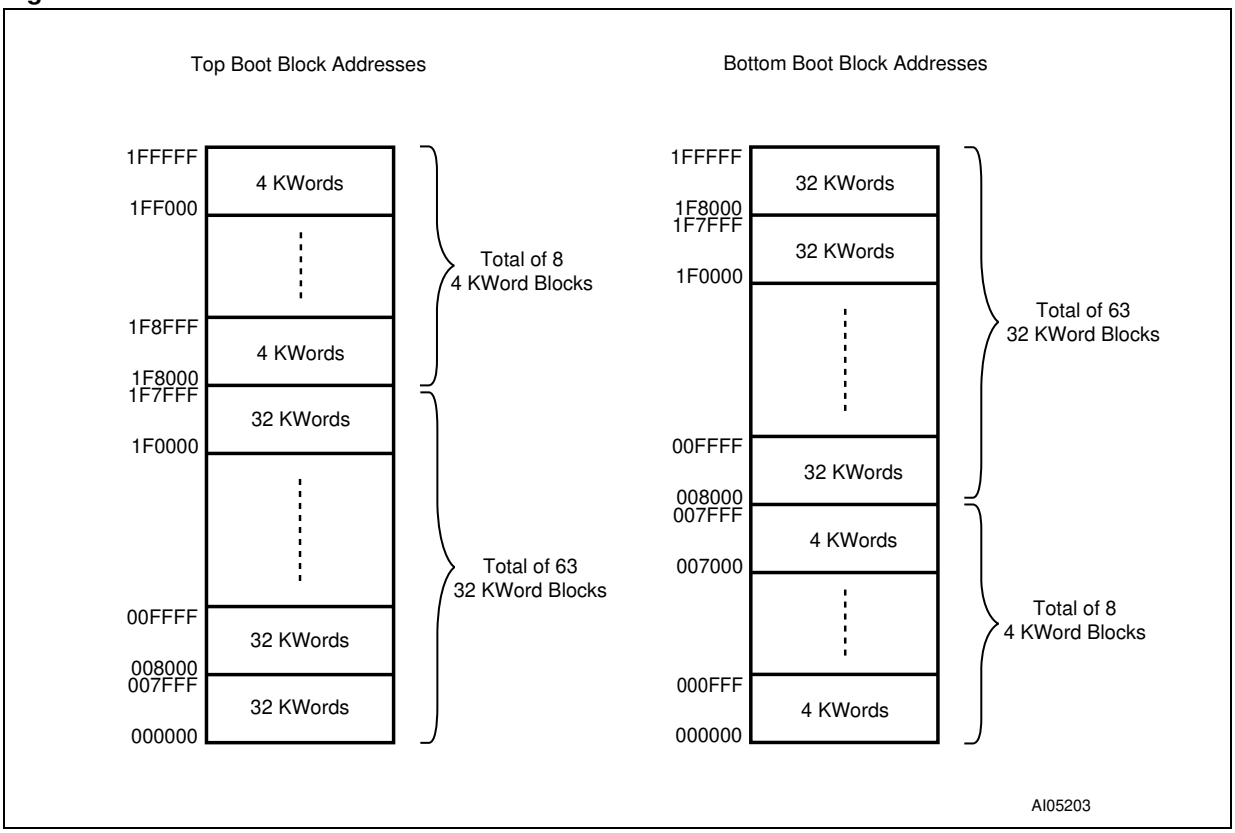
The Flash Memory features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PPF} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power Up.

Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The device includes a 128 bit Protection Register and a Security Block to increase the protection of a system design. The Protection Register is divided into two 64 bit segments, the first one contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user. Figure 6, shows the Flash Security Block Memory Map.

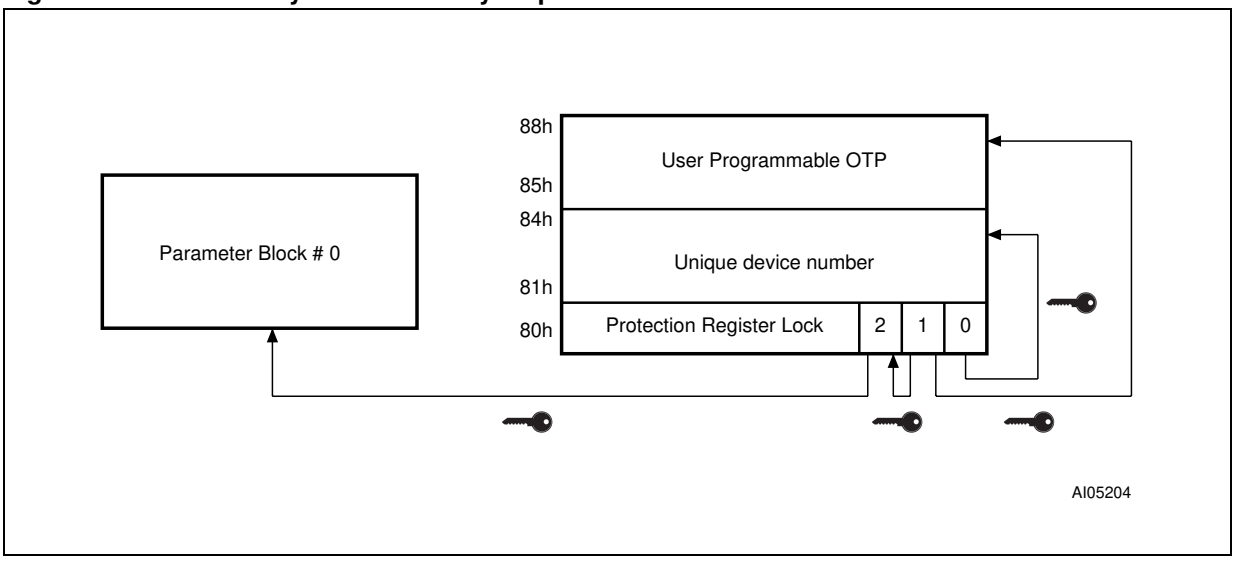
Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Figure 5. Flash Block Addresses



Note: Also see Appendix A, Tables 26 and 27 for a full listing of the Flash Block Addresses.

Figure 6. Flash Security Block Memory Map



SRAM Component

The SRAM is an 4 Mbit asynchronous random access memory which features a super low voltage operation and low current consumption with an access time of 70 ns in all conditions. The memory operations can be performed using a single low voltage supply, 2.7V to 3.3V, which is the same as the Flash voltage supply.

OPERATING MODES

Flash Bus Operations

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Reset. See Table 2, Main Operation Modes, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Read. Read Bus operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figure 9, Read Mode AC Waveforms, and Table 15, Flash Read AC Characteristics, for details of when the output becomes valid.

Read mode is the default state of the device when exiting Reset or after power-up.

Write. Bus Write operations write Commands to the memory or latch Input Data to be programmed. A write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

See Figures 10 and 11, Write AC Waveforms, and Tables 16 and 17, Flash Write AC Characteristics, for details of the timing requirements.

Output Disable. The data outputs are high impedance when the Output Enable is at V_{IH}.

Standby. Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable is at V_{IH} and the device is in read mode. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Automatic Standby. Automatic Standby provides a low power consumption state during Read mode. Following a read operation, the device enters Automatic Standby after 150ns of bus inactivity even if Chip Enable is Low, V_{IL}, and the supply current is reduced to I_{DD1}. The data Inputs/Outputs will still output data if a bus Read operation is in progress.

Reset. During Reset mode when Output Enable is Low, V_{IL}, the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL}. The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SSF} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Flash Command Interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time during, to monitor the progress of the operation, or the Program/Erase states. See Appendix 29, Table 34, Write State Machine Current/Next, for a summary of the Command Interface.

The Command Interface is reset to Read mode when power is first applied, when exiting from Reset or whenever V_{DDF} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode. Refer to Table 3, Commands, in conjunction with the text descriptions below.

Read Memory Array Command. The Read command returns the memory to its Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent read operations will read the addressed location and output the data. When a device Reset occurs, the memory defaults to Read mode.

Read Status Register Command. The Status Register indicates when a program or erase operation is complete and the success or failure of the operation itself. Issue a Read Status Register command to read the Status Register's contents. Subsequent Bus Read operations read the Status Register at any address, until another command is issued. See Table 10, Status Register Bits, for details on the definitions of the bits.

The Read Status Register command may be issued at any time, even during a Program/Erase operation. Any Read attempt during a Program/Erase operation will automatically output the content of the Status Register.

Read Electronic Signature Command. The Read Electronic Signature command reads the Manufacturer and Device Codes and the Block Locking Status, or the Protection Register.

The Read Electronic Signature command consists of one write cycle, a subsequent read will output the Manufacturer Code, the Device Code, the Block Lock and Lock-Down Status, or the Protection and Lock Register. See Tables 4, 5 and 6 for the valid address.

Read CFI Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area, allowing programming equipment or applications to automatically match their interface to the characteristics of the device. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Common Flash Interface, Tables 28, 29, 30, 31, 32 and 33 for details on the information contained in the Common Flash Interface memory area.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/ Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts.

Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

During Erase operations the memory will accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 7, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix C, Figure 28, Erase Flowchart and Pseudo Code, for a suggested flowchart for using the Erase command.

Program Command. The memory array can be programmed word-by-word. Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

During Program operations the memory will accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 7, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 25, Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

Double Word Program Command. This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel.The two words must differ only for the address A0. Programming should not be attempted when V_{PPF} is not at V_{PPH}. The command can be executed if V_{PPF} is below V_{PPH} but the result is not guaranteed.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 26, Double Word Program Flowchart and Pseudo Code, for the flowchart for using the Double Word Program command.

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One bus write cycle is required to issue the Clear Status Register command.

The bits in the Status Register do not automatically return to '0' when a new Program or Erase command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Program or Erase operation. One bus write cycle is required to issue the Program/Erase command and pause the Program/Erase controller.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array, Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Program, Block Lock, Block Lock-Down or Protection Program commands will also be accepted. The block being erased may be protected by issuing the Block Protect, Block Lock or Protection Program commands. When the Program/Erase Resume command is issued the operation will complete. Only the blocks not being erased may be read or programmed correctly.

During a Program/Erase Suspend, the device can be placed in a pseudo-standby mode by taking Chip Enable to V_{IH}. Program/Erase is aborted if Reset turns to V_{IL}.

See Appendix C, Figure 27, Program or Double Word Program Suspend & Resume Flowchart and Pseudo Code, and Figure 29, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the command. Once the command is issued subsequent Bus Read operations read the Status Register.

See Appendix C, Figure 27, Program or Double Word Program Suspend & Resume Flowchart and Pseudo Code, and Figure 29, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Resume command.

Protection Register Program Command. The Protection Register Program command is used to Program the 64 bit user One-Time-Programmable (OTP) segment of the Protection Register. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register. Bit 1 of the Protection Lock Register protects bit 2 of the Protection Lock Register. Programming bit 2 of the Protection Lock Register will result in a permanent protection of the Security Block (see Figure 6, Flash Security Block Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register and/or the Security Block is not reversible.

The Protection Register Program cannot be suspended.

Block Lock Command. The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The Lock Status can be monitored for each block using the Read Block Signature command. Table. 9 shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until reset or power-down/power-up. They are cleared by a Blocks Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Unlock Command. The Blocks Unlock command is used to unlock a block, allowing the block to be programmed or erased. Two Bus Write cycles are required to issue the Blocks Unlock command.

- The first bus cycle sets up the Block Unlock command.
- The second Bus Write cycle latches the block address.

The Lock Status can be monitored for each block using the Read Block Signature command. Table. 9 shows the Lock Status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Lock-Down Command. A locked block cannot be Programmed or Erased, or have its Lock status changed when $\overline{WP}$ is low, V_{IL}. When $\overline{WP}$ is high, V_{IH}, the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The Lock Status can be monitored for each block using the Read Block Signature command. Locked blocks revert to the protected (and not locked) state when the device is reset on power-down. Table. 9 shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation.

Table 3. Commands

Commands	No. of Cycles	Bus Write Operations								
		1st Cycle			2nd Cycle			3nd Cycle		
		Bus Op.	Addr	Data	Bus Op.	Addr	Data	Bus Op.	Addr	Data
Read Memory Array	1+	Write	X	FFh	Read	Read Addr	Data			
Read Status Register	1+	Write	X	70h	Read	X	Status Register			
Read Electronic Signature	1+	Write	X	90h	Read	Signature Addr (1)	Signature			
Read CFI Query	1+	Write	55h	98h	Read	CFI Addr	Query			
Erase	2	Write	X	20h	Write	Block Addr	D0h			
Program	2	Write	X	40h or 10h	Write	Addr	Data Input			
Double Word Program(2)	3	Write	X	30h	Write	Addr 1	Data Input	Write	Addr 2	Data Input
Clear Status Register	1	Write	X	50h						
Program/Erase Suspend	1	Write	X	B0h						
Program/Erase Resume	1	Write	X	D0h						
Block Lock	2	Write	X	60h	Write	Block Address	01h			
Block Unlock	2	Write	X	60h	Write	Block Address	D0h			
Block Lock-Down	2	Write	X	60h	Write	Block Address	2Fh			
Protection Register Program	2	Write	X	C0h	Write	Address	Data Input			

Note: X = Don't Care.

1. The signature addresses are listed in Tables 4, 5 and 6.
2. Addr 1 and Addr 2 must be consecutive Addresses differing only for A0.

Table 4. Read Electronic Signature

Code	Device	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A2-A7	A8-A11	A12-A20	DQ0-DQ7	DQ8-DQ15
Manufacture Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	Don't Care	Don't Care	20h	00h
Device Code	M36W432T	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	Don't Care	xxh	88h
	M36W432B	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	Don't Care	xxh	88h

Note: $\overline{RPF} = V_{IH}$.

Table 5. Read Block Signature

Block Status	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A2-A7	A8-A20	A12-A20	DQ0	DQ1	DQ2-DQ15
Locked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	1	0	00h
Unlocked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	0	0	00h
Locked-Down Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	X (1)	1	00h

Note: 1. A Locked Block can be protected "DQ0 = 1" or unprotected "DQ0 = 0"; see Block Locking section.

Table 6. Read Protection Register and Lock Register

Word	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0-A7	A8-A20	DQ0	DQ1	DQ2	DQ3-DQ7	DQ8-DQ15
Lock	V_{IL}	V_{IL}	V_{IH}	80h	Don't Care	0	OTP Prot. data	Security prot. data	00h	00h
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	81h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	82h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	83h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	84h	Don't Care	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	85h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	86h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	87h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	88h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data

Table 7. Program, Erase Times and Program/Erase Endurance Cycles

Parameter	Test Conditions	Flash Memory			Unit
		Min	Typ	Max	
Word Program	$V_{PPF} = V_{DDF}$		10	200	µs
Double Word Program	V_{PPF} = 12V ±5%		10	200	µs
Main Block Program	V_{PPF} = 12V ±5%		0.16	5	s
	$V_{PPF} = V_{DDF}$		0.32	5	s
Parameter Block Program	V_{PPF} = 12V ±5%		0.02	4	s
	$V_{PPF} = V_{DDF}$		0.04	4	s
Main Block Erase	V_{PPF} = 12V ±5%		1	10	s
	$V_{PPF} = V_{DDF}$		1	10	s
Parameter Block Erase	V_{PPF} = 12V ±5%		0.8	10	s
	$V_{PPF} = V_{DDF}$		0.8	10	s
Program/Erase Cycles (per Block)		100,000			cycles

Flash Block Locking

The Flash Memory features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has three levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.
- $V_{PPF} \leq V_{PPLK}$ - the third level offers a complete hardware protection against program and erase on all blocks.

The locking status of each block can be set to Locked, Unlocked, and Lock-Down. The following sections explain the operation of the locking system. Table 7, defines all of the possible locking states ($\overline{WP}$, DQ1, DQ0), and Appendix C, Figure 30, shows a flowchart for the locking operations.

Locked State. The default status of all blocks on power-up or reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will return an error in the Status Register. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

Unlocked State. Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state when the device is reset or powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

Lock-Down State. Blocks that are Locked-Down (state (0,1,1))are protected from program and erase operations (as for Locked blocks) but their Lock status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WPF}$ input pin. When $\overline{WPF}$=0 (V_{IL}), the blocks in the Lock-Down state (0,1,1) are protected from program, erase and lock status changes. When $\overline{WPF}$=1 (V_{IH}) the Lock-Down function is disabled (1,1,1) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-locked (1,1,1) and unlocked (1,1,0) as desired while $\overline{WPF}$ remains high. When $\overline{WPF}$ is low, blocks that were previously Locked-Down return to the Lock-Down state (0,1,1) regardless of any changes made while $\overline{WPF}$ was high. Device reset or power-down resets all blocks, including those in Lock-Down, to the Locked state.

Reading a Block's Lock Status. The lock status of every block can be read in the Read Electronic Signature mode of the device. To enter this mode write 90h to the device. Subsequent reads at Block Address 00002h will output the lock status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. it is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a device reset or power-down.

Locking Operations During Erase Suspend. Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Locking operations cannot be performed during a program suspend. Refer to Appendix D, Command Interface and Program/Erase Controller State, for detailed information on which commands are valid during erase suspend.

Table 8. Block Lock Status

Item	Address	Data
Block Lock Configuration	xx002	LOCK
Block is Unlocked		DQ0=0
Block is Locked		DQ0=1
Block is Locked-Down		DQ1=1

Table 9. Lock Status

Current Lock Status(1) (WPF, DQ1, DQ0)		Next Lock Status(1) (WPF, DQ1, DQ0)			
Current State	**Program/Erase Allowed**	**After Block Lock Command**	**After Block Unlock Command**	**After Block Lock-Down Command**	**After $\overline{WPF}$ transition**
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1(2)	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1(2)	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 (3)

Note: 1. The lock status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a locked block) as read in the Read Electronic Signature command with A1 = V_{IH} and A0 = V_{IL}.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to $\overline{WPF}$ status.
3. A $\overline{WPF}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

Flash Status Register

The Status Register provides information on the current or previous Program or Erase operation. The various bits convey information and errors on the operation. To read the Status register the Read Status Register command can be issued, refer to Read Status Register Command section. To output the contents, the Status Register is latched on the falling edge of the Chip Enable or Output Enable signals, and can be read until Chip Enable or Output Enable returns to V_{IH}. Either Chip Enable or Output Enable must be toggled to update the latched data.

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 10, Status Register Bits. Refer to Table 10 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low (set to '0'), the Program/Erase Controller is active; when the bit is High (set to '1'), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, operations the Program/Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PPF} Status and Block Lock Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended. When the Erase Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 7 is set within 30µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. When the Erase Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program failure. When the Program Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

V_{PPF} Status (Bit 3). The V_{PPF} Status bit can be used to identify an invalid voltage on the V_{PPF} pin during Program and Erase operations. The V_{PPF} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PPF} becomes invalid during an operation.

When the V_{PPF} Status bit is Low (set to '0'), the voltage on the V_{PPF} pin was sampled at a valid voltage; when the V_{PPF} Status bit is High (set to '1'), the V_{PPF} pin has a voltage that is below the V_{PPF} Lockout Voltage, V_{PPLK}, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PPF} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended. When the Program Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 2 is set within 5µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to '1'), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value must be masked.

Note: Refer to Appendix C, Flowcharts and Pseudo Codes, for using the Status Register.

Table 10. Status Register Bits

Bit	Name	Logic Level	Definition
7	P/E.C. Status	'1'	Ready
		'0'	Busy
6	Erase Suspend Status	'1'	Suspended
		'0'	In progress or Completed
5	Erase Status	'1'	Erase Error
		'0'	Erase Success
4	Program Status	'1'	Program Error
		'0'	Program Success
3	V_{PPF} Status	'1'	V_{PPF} Invalid, Abort
		'0'	V_{PPF} OK
2	Program Suspend Status	'1'	Suspended
		'0'	In Progress or Completed
1	Block Protection Status	'1'	Program/Erase on protected block, Abort
		'0'	No operation to protected blocks
0	Reserved		

Note: Logic level '1' is High, '0' is Low.

SRAM Operations

There are five standard operations that control the SRAM component. These are Bus Read, Bus Write, Standby/Power-down, Data Retention and Output Disable. A summary is shown in Table 2, Main Operation Modes

Read. Read operations are used to output the contents of the SRAM Array. The SRAM is in Read mode whenever Write Enable, $\overline{WS}$, is at V_{IH}, Output Enable, $\overline{GS}$, is at V_{IL}, Chip Enable, $\overline{E1S}$, is at V_{IL}, Chip Enable, E2S, is at V_{IH}, and Byte Enables, $\overline{UBS}$ and $\overline{LBS}$ are at V_{IL}.

Valid data will be available on the output pins after a time of t_{AVQV} after the last stable address. If the Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV} (see Table 19, Figures 13 and 14).

Write. Write operations are used to write data to the SRAM. The SRAM is in Write mode whenever $\overline{WS}$ and $\overline{E1S}$ are at V_{IL}, and E2S is at V_{IH}. Either the Chip Enable inputs, $\overline{E1S}$ and E2S, or the Write Enable input, $\overline{WS}$, must be deasserted during address transitions for subsequent write cycles.

A Write operation is initiated when $\overline{E1S}$ is at V_{IL}, E2S is at V_{IH} and $\overline{WS}$ is at V_{IL}. The data is latched on the falling edge of $\overline{E1S}$, the rising edge of E2S or the falling edge of $\overline{WS}$, whichever occurs last. The Write cycle is terminated on the rising edge of $\overline{E1S}$, the rising edge of $\overline{WS}$ or the falling edge of E2S, whichever occurs first.

If the Output is enabled ($\overline{E1S}$=V_{IL}, E2S=V_{IH} and $\overline{GS}$=V_{IL}), then $\overline{WS}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. The Data input must be valid for t_{DVWH} before the rising edge of Write Enable, for t_{DVE1H} before the rising edge of $\overline{E1S}$ or for t_{DVE2L} before the falling edge of E2S, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HAX} or t_{E2LAX} (see Table 20, Figure 16, 17, 18 and 19).

Standby/Power-Down. The SRAM component has a chip enabled power-down feature which invokes an automatic standby mode (see Table 19, Figure 15). The SRAM is in Standby mode whenever either Chip Enable is deasserted, $\overline{E1S}$ at V_{IH} or E2S at V_{IL}.

Data Retention. The SRAM data retention performances as V_{DDS} goes down to V_{DR} are described in Table 21 and Figure 20, 21. In $\overline{E1S}$ controlled data retention mode, the minimum standby current mode is entered when $\overline{E1S} \geq V_{DDS} - 0.2V$ and $E2S \leq 0.2V$ or $E2S \geq V_{DDS} - 0.2V$. In E2S controlled data retention mode, minimum standby current mode is entered when $E2S \leq 0.2V$.

Output Disable. The data outputs are high impedance when the Output Enable, $\overline{GS}$, is at V_{IH} with Write Enable, $\overline{WS}$, at V_{IH}.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature (1)	–40	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	155	°C
V_{IO}	Input or Output Voltage	–0.5	V_{DDQF} +0.3	V
V_{DDF}, V_{DDQF}	Flash Supply Voltage	–0.6	3.9	V
V_{PPF}	Program Voltage	–0.6	13	V
V_{DDS}	SRAM Supply Voltage	–0.5	3.9	V

Note: 1. Depends on range.

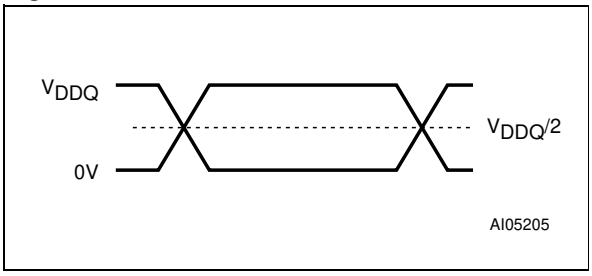
DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 12, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 12. Operating and AC Measurement Conditions

Parameter	SRAM		Flash Memory		Units
	70		70/85		
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	–	–	2.7	3.3	V
$V_{DDQ\ F\ =}$ V_{DDS} Supply Voltage	2.7	3.3	2.7	3.3	V
Ambient Operating Temperature	– 40	85	– 40	85	°C
Load Capacitance (C_L)	50		50		pF
Input Rise and Fall Times		5		5	ns
Input Pulse Voltages	0 to V_{DDQF}		0 to V_{DDQF}		V
Input and Output Timing Ref. Voltages	$V_{DDQF}/2$		$V_{DDQF}/2$		V

Figure 7. AC Measurement I/O Waveform



Note: V_{DDQ} means $V_{DDQF} = V_{DDS}$

Figure 8. AC Measurement Load Circuit

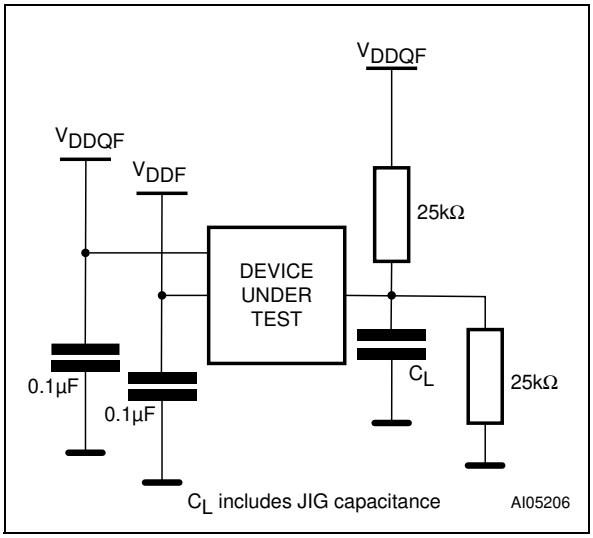


Table 13. Device Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f=1 MHz	12	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f=1 MHz	20	22	pF

Note: Sampled only, not 100% tested.

Table 14. DC Characteristics

Symbol	Parameter	Device	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	Flash & SRAM	$0V \le V_{IN} \le V_{DDQF}$			±2	µA
I_{LO}	Output Leakage Current	Flash & SRAM	$0V \le V_{OUT} \le V_{DDQF}$, SRAM Outputs Hi-Z			±10	µA
I_{DDS}	V_{DD} Standby Current	Flash	$\overline{EF} = V_{DDQF} \pm 0.2V$ $V_{DDQF} = V_{DDF}$ max		15	50	µA
		SRAM	$\overline{E1S} = E2S \ge V_{DDS} - 0.2V$ or $E2S \le 0.2V$		20	50	µA
I_{DDD}	Supply Current (Reset)	Flash	$\overline{RPF} = V_{SSF} \pm 0.2V$		15	50	µA
I_{DD}	Supply Current	SRAM	$V_{IN} \le V_{DDS} - 0.2V$ or $V_{IN} \le 0.2V$ I_{IO} = 0 mA, cycle time = 1µs		1	2	mA
			$V_{IN} \le V_{DDS} - 0.2V$ or $V_{IN} \le 0.2V$ I_{IO} = 0 mA, min cycle time		7	12	mA
I_{DDR}	Supply Current (Read)	Flash	$\overline{EF} = V_{IL}$, $\overline{GF} = V_{IH}$, f = 5 MHz		10	20	mA
I_{DDW}	Supply Current (Program)	Flash	Program in progress		10	20	mA
I_{DDE}	Supply Current (Erase)	Flash	Erase in progress		5	20	mA
I_{DDES}	Supply Current (Erase Suspend)	Flash	Erase Suspend in progress			50	µA
I_{DDWS}	Supply Current (Program Suspend)	Flash	Program Suspend in progress			50	µA
I_{PPS}	Program Current (Standby)	Flash	$V_{PPF} \le V_{DDQF}$		0.2	5	µA
			$V_{PPF} > V_{DDF}$		100	400	µA
I_{PPR}	Program Current (Read)	Flash	$V_{PPF} \le V_{DDQF}$		0.2	5	µA
			$V_{PPF} = V_{DDF}$		100	400	µA
I_{PPW}	Program Current (Program)	Flash	$V_{PPF} = 12V \pm 0.6V$ Program in progress		5	10	mA
I_{PPE}	Program Current (Erase)	Flash	$V_{PPF} = 12V \pm 0.6V$ Program in progress		5	10	mA
V_{IL}	Input Low Voltage	Flash & SRAM	$V_{DDQF} = V_{DDS} \ge 2.7V$	– 0.3		0.8	V
V_{IH}	Input High Voltage	Flash & SRAM	$V_{DDQF} = V_{DDS} \ge 2.7V$	2.2		V_{DDQF} +0.3	V
V_{OL}	Output Low Voltage	Flash & SRAM	$V_{DDQF} = V_{DDS} = V_{DD}$ min I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	Flash & SRAM	$V_{DDQF} = V_{DDS} = V_{DD}$ min I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PPL}	Program Voltage (Program or Erase operations)	Flash		2.7		3.3	V

Symbol	Parameter	Device	Test Condition	Min	Typ	Max	Unit
V_{PPH}	Program Voltage (Program or Erase operations)	Flash		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)	Flash				1	V
V_{LKO}	V_{DDF} Supply Voltage (Program and Erase lock-out)	Flash				2	V

Figure 9. Flash Read AC Waveforms

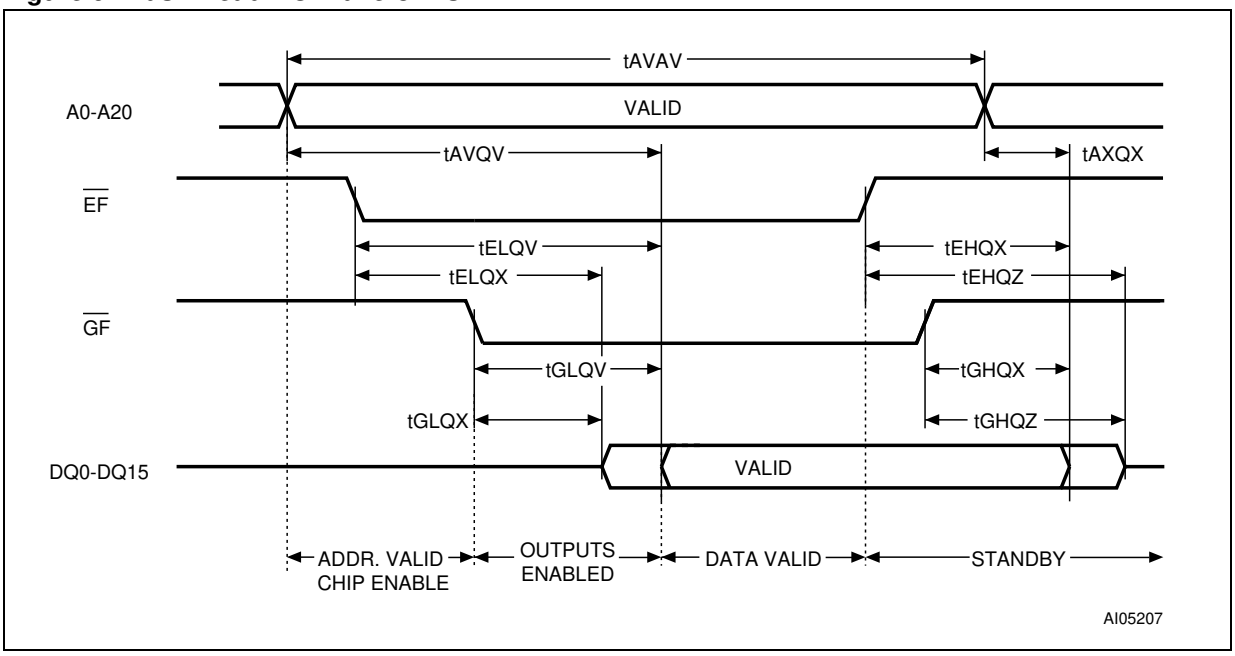


Table 15. Flash Read AC Characteristics

Symbol	Alt	Parameter		Flash		Unit
				70	85	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	70	85	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	Max	70	85	ns
t_{AXQX} (1)	t_{OH}	Address Transition to Output Transition	Min	0	0	ns
t_{EHQX} (1)	t_{OH}	Chip Enable High to Output Transition	Min	0	0	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	20	20	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	Max	70	85	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	ns
t_{GHQX} (1)	t_{OH}	Output Enable High to Output Transition	Min	0	0	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	Max	20	20	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	20	20	ns

Symbol	Alt	Parameter		Flash		Unit
				70	85	
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{GF}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EF}$ without increasing t_{ELQV}.