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3858 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0139-0111
Rev.1.11
Dec 18, 2008

DESCRIPTION

The 3858 group is the 8-bit microcomputer based on the 740 family core technology.
The 3858 group is designed for the household products and office automation equipment and includes serial interface functions, 8-bit timer, 16-bit timer, and A/D converter.

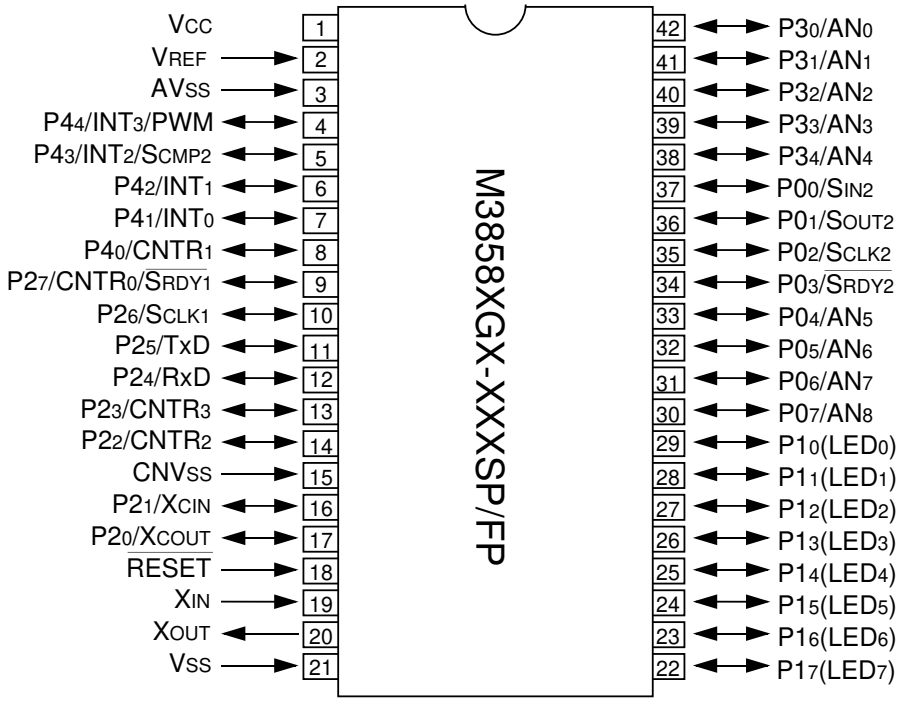
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.32 µs
  (at 12.5 MHz oscillation frequency)
- Memory size
  - ROM ..... 48 K bytes
  - RAM ..... 1.5 K bytes
- Programmable input/output ports 34
- On-chip software pull-up resistor ..... Built-in
- Interrupts ..... 19 sources, 16 vectors
  (external 8, internal 10, software 1)
- Timers ..... 8-bit × 4
  ..... 16-bit × 2
- Serial interface
  - Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
  - Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- PWM ..... 8-bit × 1
- A/D converter ..... 8-bit × 9 channels
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V
    (at 12.5 MHz oscillation frequency)
  - In high-speed mode ..... 2.7 to 5.5 V
    (at 6 MHz oscillation frequency)
  - In middle-speed mode ..... 2.7 to 5.5 V
    (at 12.5 MHz oscillation frequency, at middle-speed mode)
  - In low-speed mode ..... 2.7 to 5.5 V
    (at 32 kHz oscillation frequency)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Office automation equipment, Factory automation equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : PRDP0042BA-A (42P4B)
PRSP0042GA-A/B (42P2R-A/E)

Fig. 1 Pin configuration of M3858XGX-XXXSP/FP

FUNCTIONAL BLOCK DIAGRAM

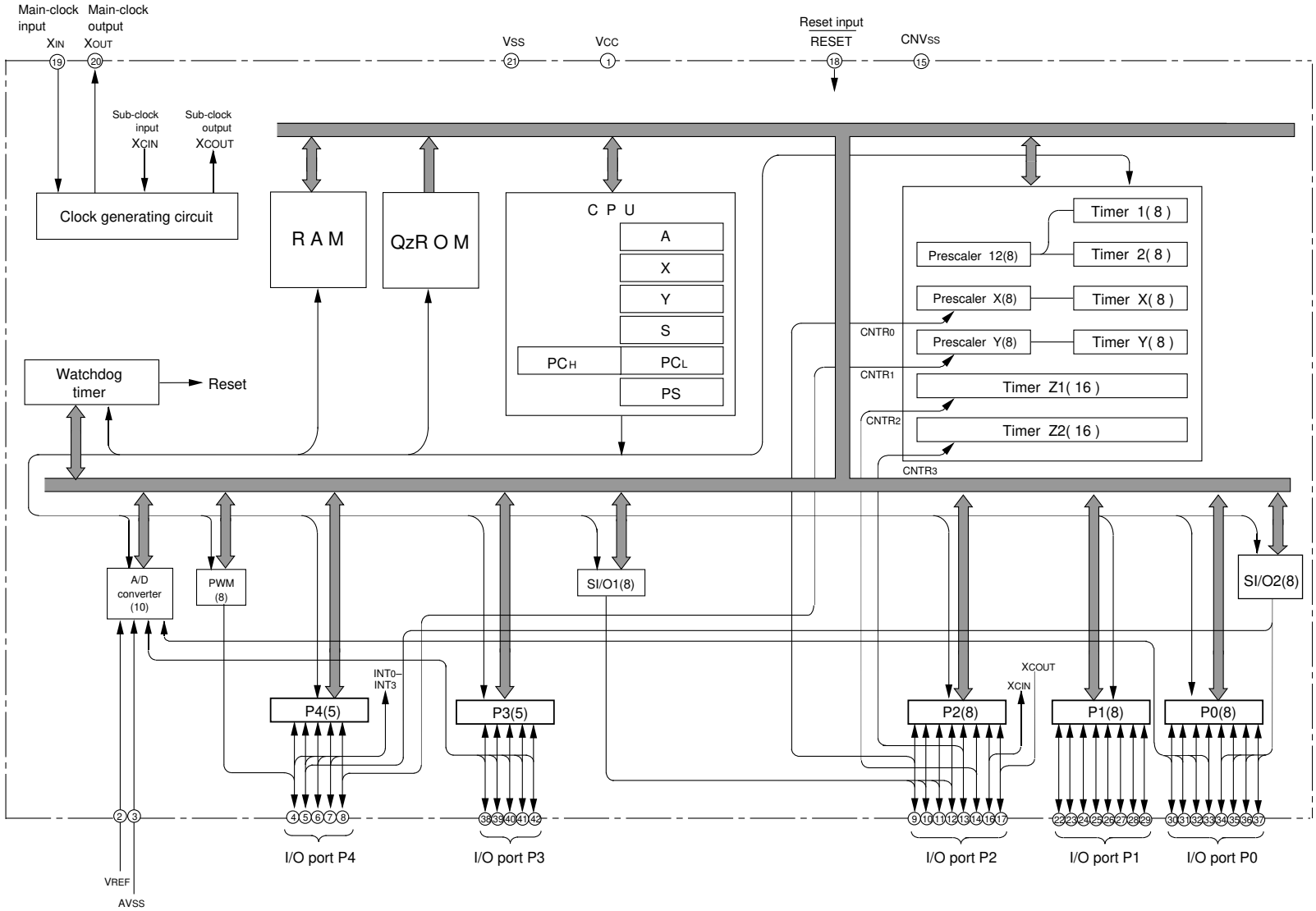


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip and is shared with the VPP pin which is the power source input pin for programming the built-in QzROM. •Normally connected to VSS.	
VREF	Reference voltage	•Reference voltage input pin for A/D converter.	
AVss	Analog power source	•Analog power source input pin for A/D converter. •Connect to Vss.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/$\overline{\text{SRDY2}}$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	• Serial I/O2 function pin
P04/AN5–P07/AN8			• A/D converter input pin
P10–P17	I/O port P1	•P10 to P17 (8 bits) are enabled to output large current for LED drive.	
P20/XCOUT P21/XCIN	I/O port P2	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS3-state output structure. •Pull-up control is enabled in a bit unit.	• Sub-clock generating circuit I/O pins (connect a resonator)
P22/CNTR2			• Timer Z1 function pin
P23/CNTR3			• Timer Z2 function pin
P24/RxD P25/TxD P26/SCLK1			• Serial I/O1 function pin
P27/CNTR0/$\overline{\text{SRDY1}}$			• Timer X function pin/ Serial I/O1 function pin
P30/AN0– P34/AN4	I/O port P3	•5-bit I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	• A/D converter input pin
P40/CNTR1	I/O port P4	•5-bit I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled in a bit unit.	• Timer Y function pin
P41/INT0 P42/INT1			• Interrupt input pins
P43/INT2/SCMP2			• Interrupt input pin • SCMP2 output pin
P44/INT3/PWM			• Interrupt input pin • PWM output pin

PART NUMBERING

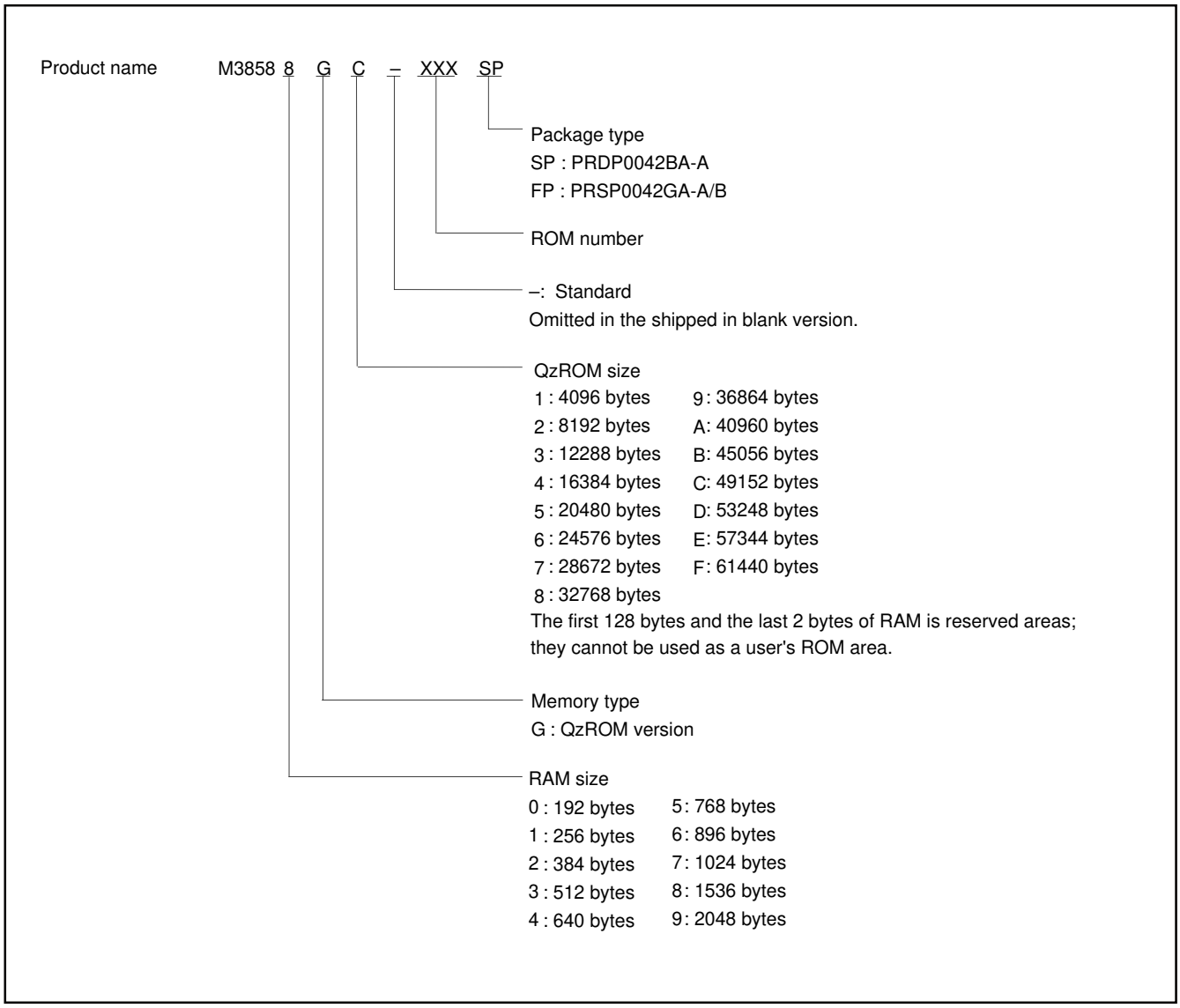


Fig. 3 Part numbering

GROUP EXPANSION

Renesas Technology plans to expand the 3858 group as follows.

Memory Type

Support for QzROM version.

Memory Size

QzROM size ..... 48 K bytes
RAM size ..... 1.5 K bytes

Packages

PRDP0042BA-A ..... 42-pin shrink plastic-molded SDIP
PRSP0042GA-A/B ..... 42-pin plastic-molded SSOP

Memory Expansion Plan

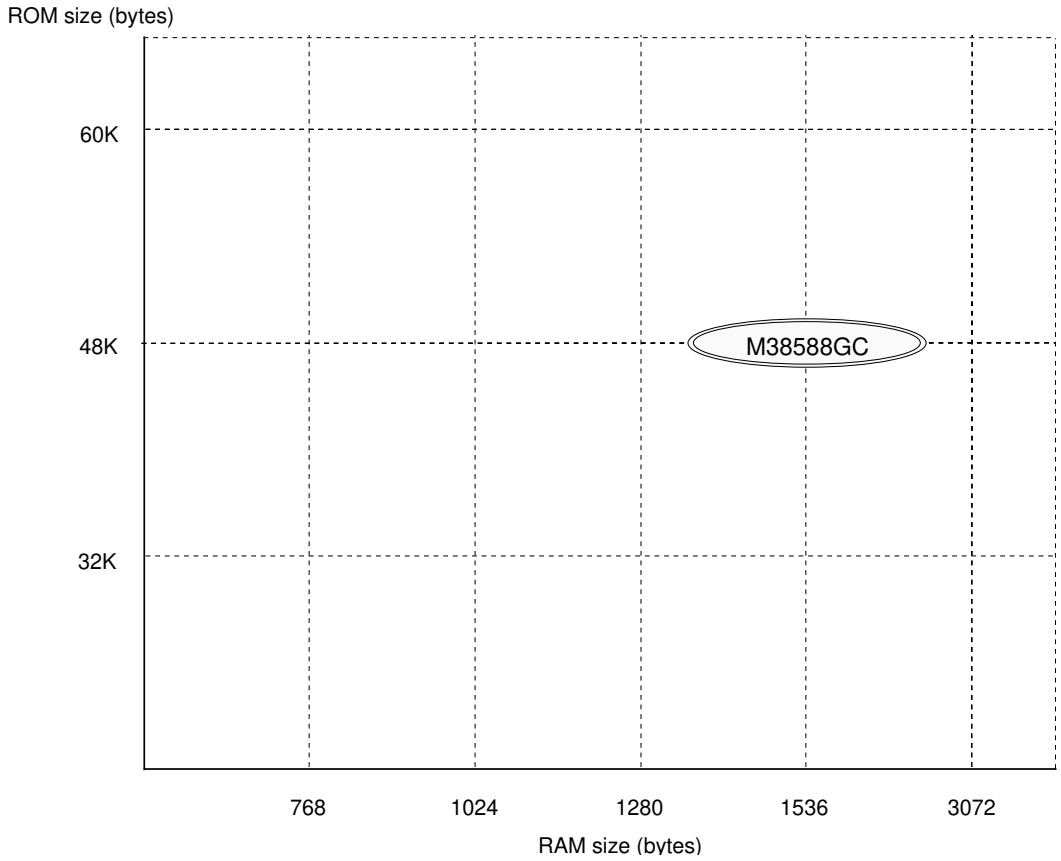


Fig. 4 Memory expansion plan

Table 2 List of products

Part number	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38588GC-XXXSP	49152 (49021)	1536	PRDP0042BA-A	
M38588GC-XXXFP			PRSP0042GA-A/B	
M38588GCSP	49152 (49021)	1536	PRDP0042BA-A	Blank
M38588GCFP			PRSP0042GA-A/B	

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3858 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls (see Table 3).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

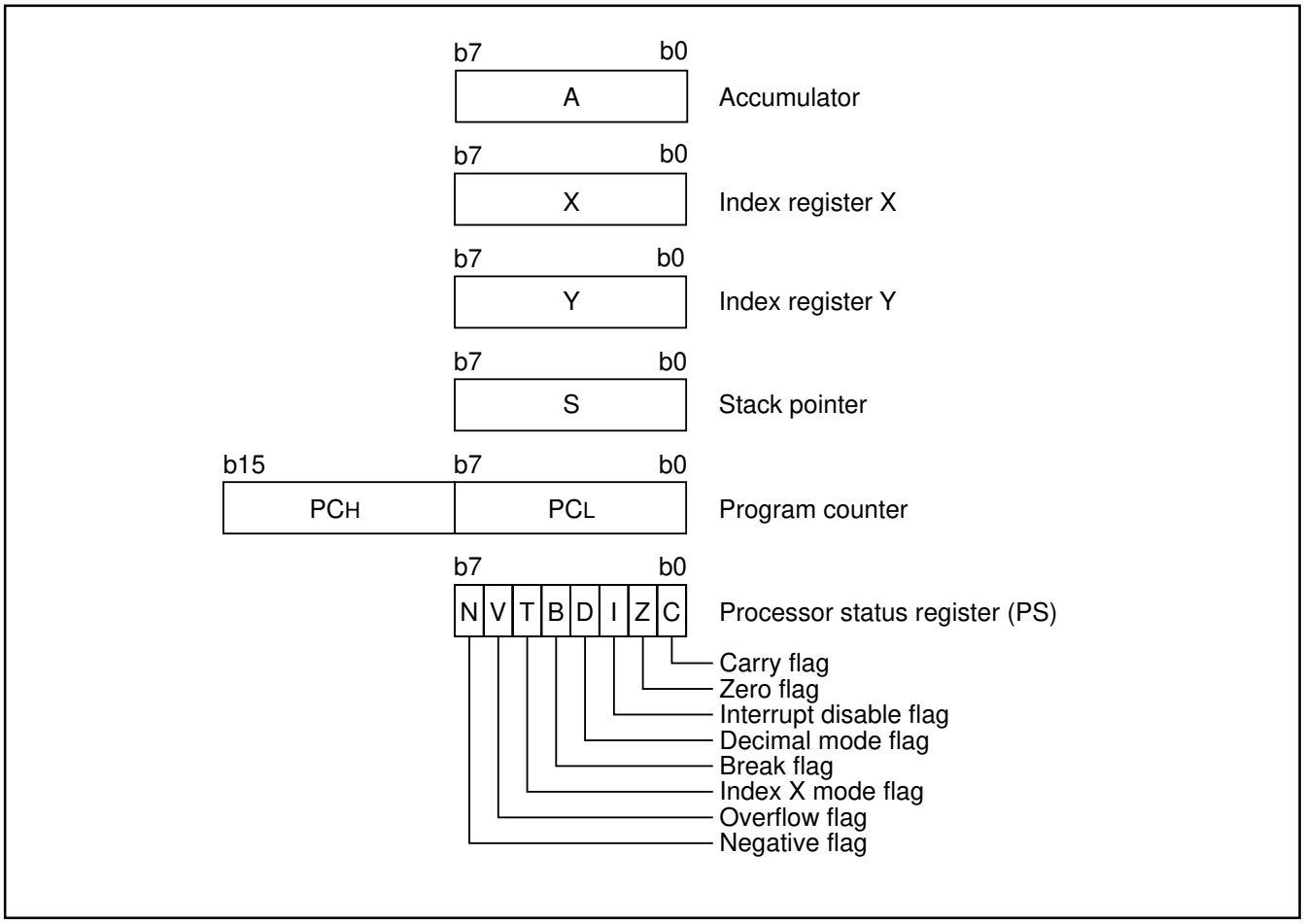


Fig. 5 740 Family CPU register structure

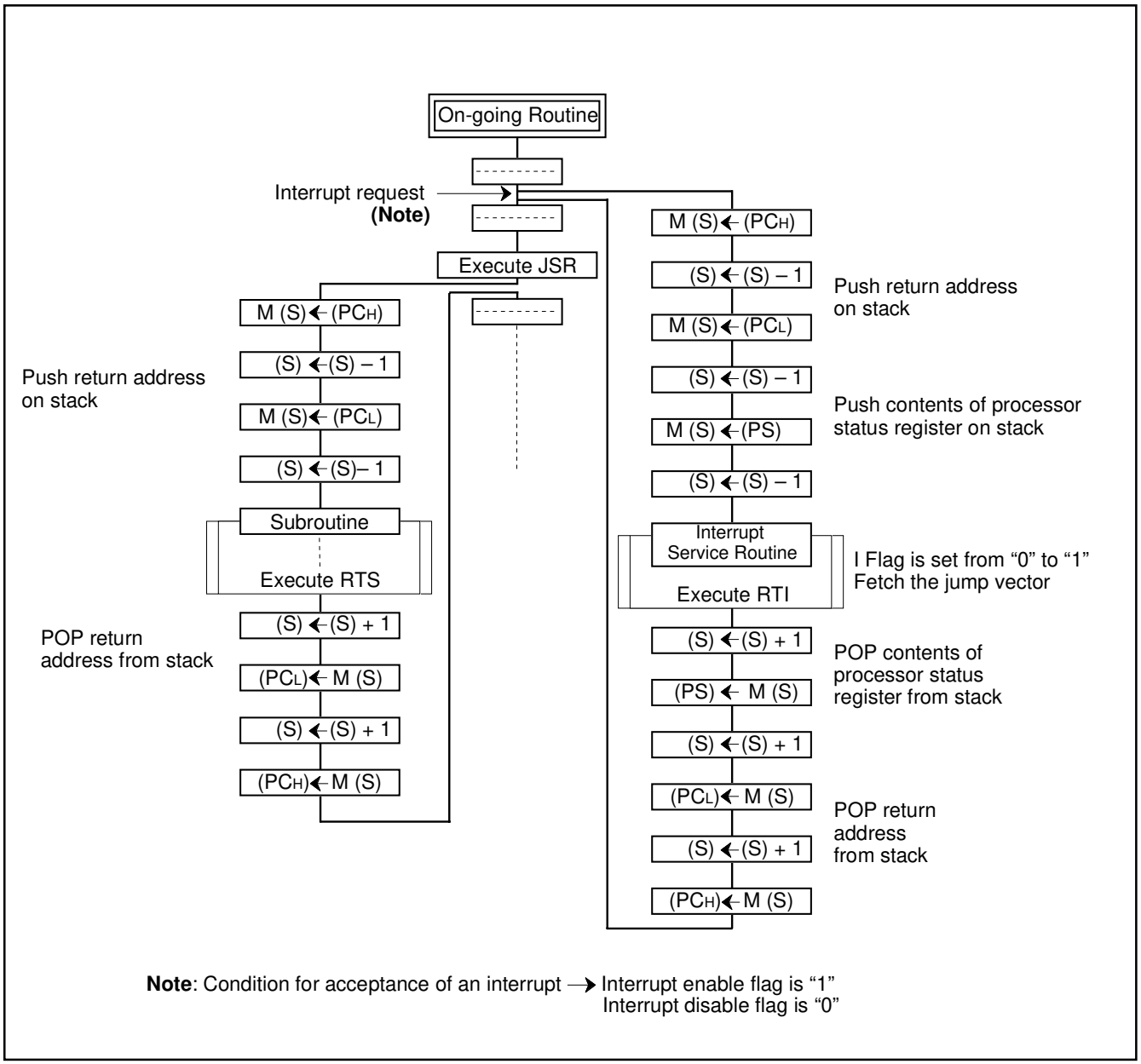


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address 003B16.

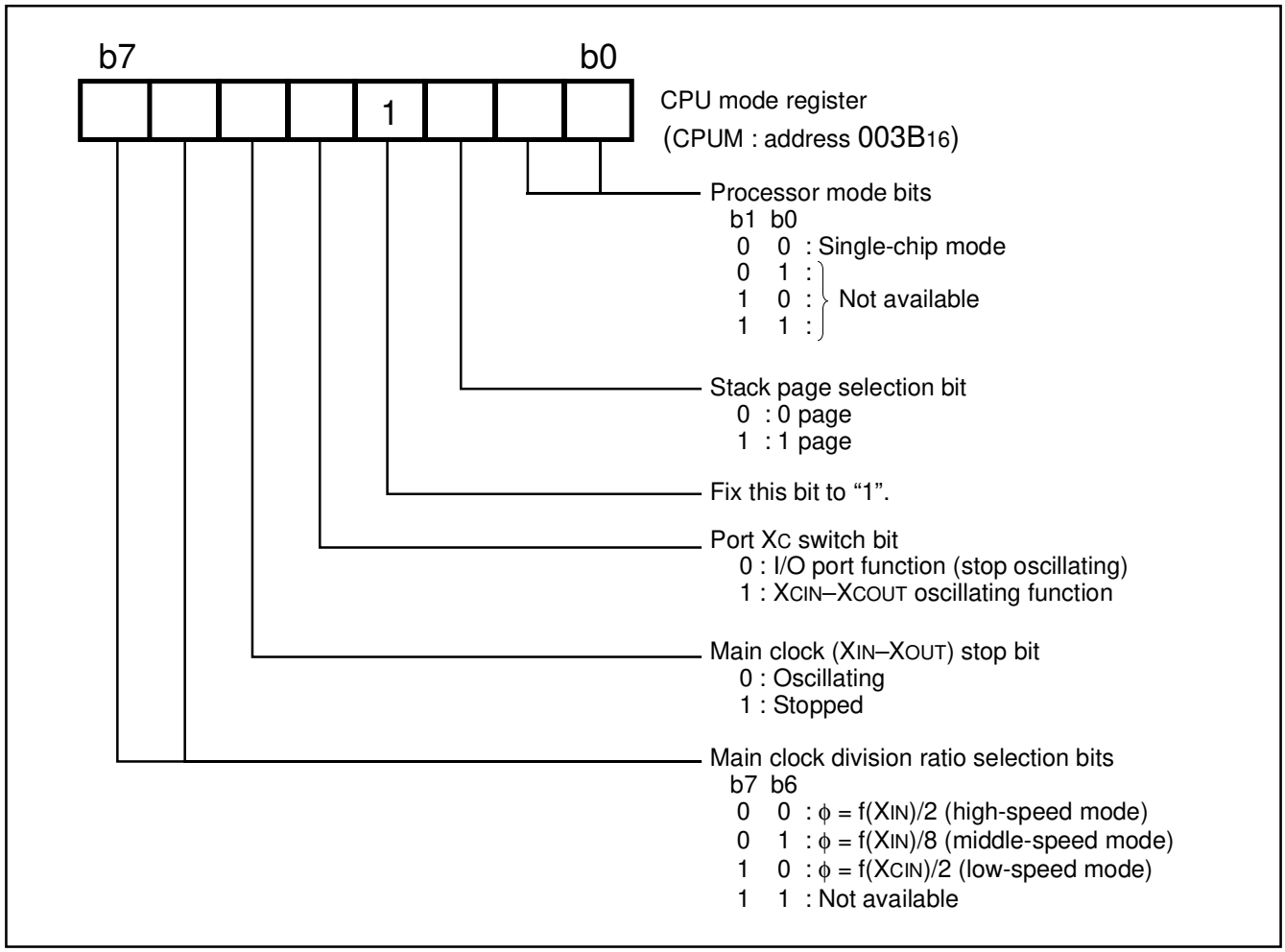


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address (address FFDB16)

Address FFDB16, which is the reserved ROM area of QzROM, is the ROM code protect address. "0016" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "0016" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "0016" (protect enabled) or "FF16" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "0016" or "FF16" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

■ Notes

Because the contents of RAM are indefinite at reset, set initial values before using.

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016

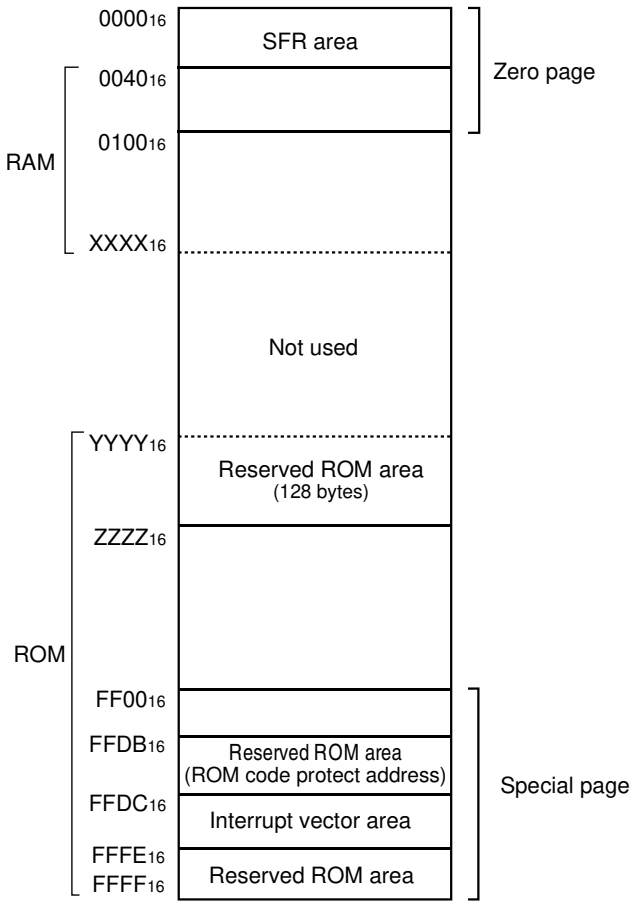


Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	
$000B_{16}$	
$000C_{16}$	
$000D_{16}$	
$000E_{16}$	
$000F_{16}$	
0010_{16}	Port P0 pull-up control register (PULL0)
0011_{16}	Port P1 pull-up control register (PULL1)
0012_{16}	Port P2 pull-up control register (PULL2)
0013_{16}	Port P3 pull-up control register (PULL3)
0014_{16}	Port P4 pull-up control register (PULL4)
0015_{16}	Serial I/O2 control register 1 (SIO2CON1)
0016_{16}	Serial I/O2 control register 2 (SIO2CON2)
0017_{16}	Serial I/O2 register (SIO2)
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O1 status register (SIOSTS)
$001A_{16}$	Serial I/O1 control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	PWM control register (PWMCON)
$001E_{16}$	PWM prescaler (PREPWM)
$001F_{16}$	PWM register (PWM)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Timer Z1 mode register (TZ1M)
0029_{16}	Timer Z1 low-order (TZ1L)
$002A_{16}$	Timer Z1 high-order (TZ1H)
$002B_{16}$	Timer Z2 mode register (TZ2M)
$002C_{16}$	Timer Z2 low-order (TZ2L)
$002D_{16}$	Timer Z2 high-order (TZ2H)
$002E_{16}$	Timer 12, X count source selection register (T12XCSS)
$002F_{16}$	Timer Y, Z1 count source selection register (TYZ1CSS)
0030_{16}	Timer Z2 count source selection register (TZ2CSS)
0031_{16}	
0032_{16}	
0033_{16}	
0034_{16}	AD control register (ADCON)
0035_{16}	AD conversion register (AD)
0036_{16}	Interrupt source selection register (INTSEL)
0037_{16}	Reserved ✻
0038_{16}	MISRG
0039_{16}	Watchdog timer control register (WDTCON)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

✻ Reserved : Do not write any data to this addresses, because these areas are reserved.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

By setting the port P0 pull-up control register (address 0010_{16}), the port P1 pull-up control register (address 0011_{16}), the port P2 pull-up control register (address 0012_{16}), the port P3 pull-up control register (address 0013_{16}), or the port P4 pull-up control register (address 0014_{16}), ports can control pull-up with a program. However, the contents of these registers do not affect ports programmed as the output ports.

Table 5 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
$P0_0$/S_{IN2} $P0_1$/S_{OUT2} $P0_2$/S_{CLK2} $P0_3$/$\overline{S_{RDY2}}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
$P0_4$/AN_5–$P0_7$/AN_8				A/D converter input	AD control register AD input selection register	(13)
$P1_0$–$P1_7$	Port P1					(5)
$P2_0$/X_{COUT} $P2_1$/X_{CIN}	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
$P2_2$/$CNTR_2$				Timer Z1 function I/O	Timer Z1 mode register	(8)
$P2_3$/$CNTR_3$				Timer Z2 function I/O	Timer Z2 mode register	(8)
$P2_4$/RxD $P2_5$/TxD $P2_6$/S_{CLK1}				Serial I/O1 function I/O	Serial I/O1 control register	(9) (10) (11)
$P2_7$/$CNTR_0$/$\overline{S_{RDY1}}$				Timer X function I/O Serial I/O1 function I/O	Timer XY mode register Serial I/O1 control register	(12)
$P3_0$/AN_0– $P3_4$/AN_4	Port P3 **(Note)**			A/D converter input	AD control register AD input selection register	(13)
$P4_0$/$CNTR_1$	Port P4 **(Note)**			Timer Y function I/O	Timer XY mode register	(14)
$P4_1$/INT_0 $P4_2$/INT_1				External interrupt input	Interrupt edge selection register	(15)
$P4_3$/INT_2/S_{CMP2}				External interrupt input S_{CMP2} output	Interrupt edge selection register Serial I/O2 control register	(16)
$P4_4$/INT_3/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(17)

Note: When bits 5 to 7 of Ports P3 and P4 are read out, the contents are undefined.

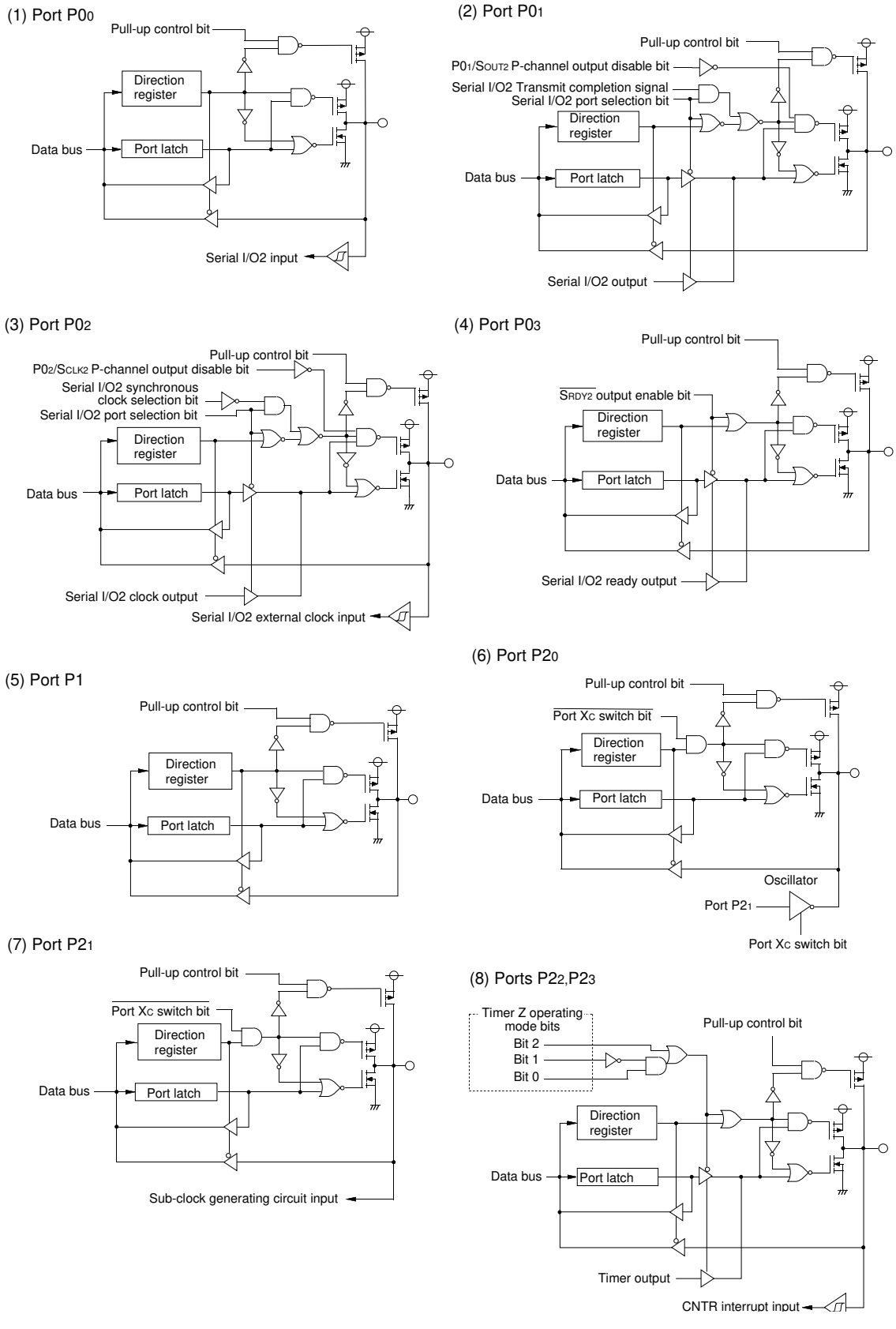


Fig. 10 Port block diagram (1)

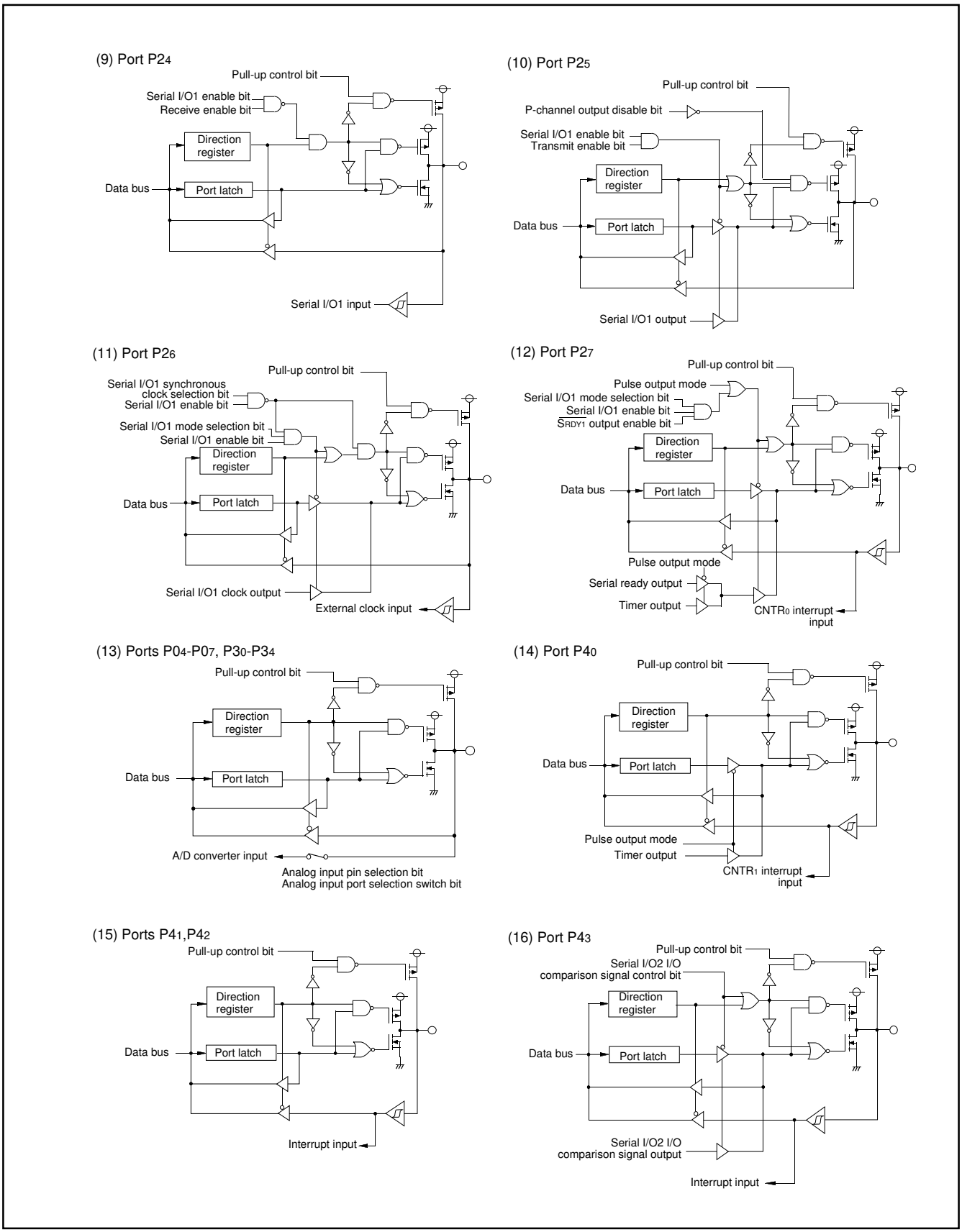


Fig. 11 Port block diagram (2)

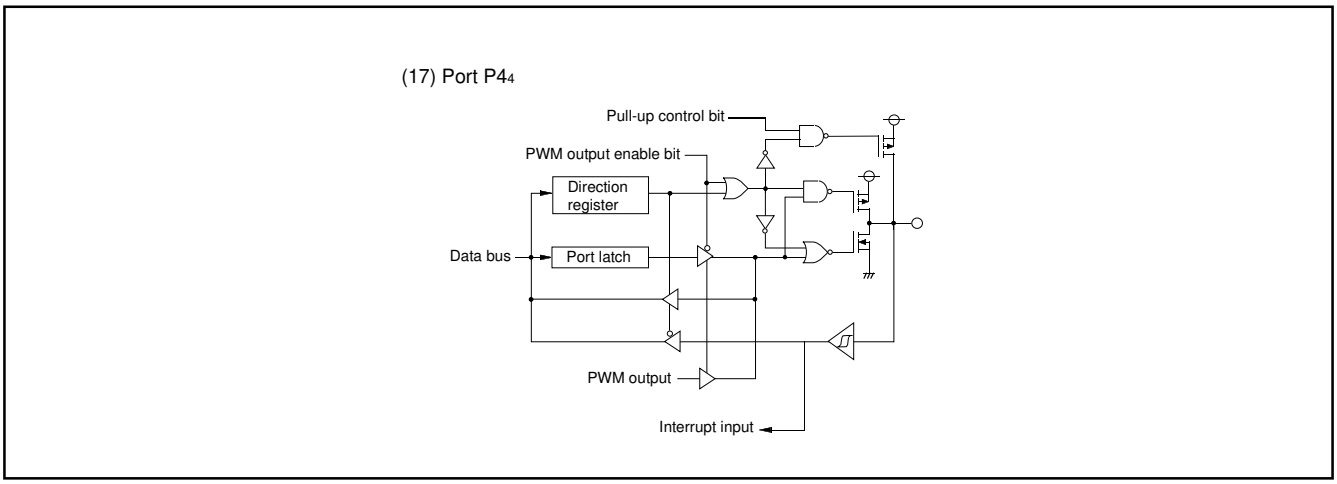
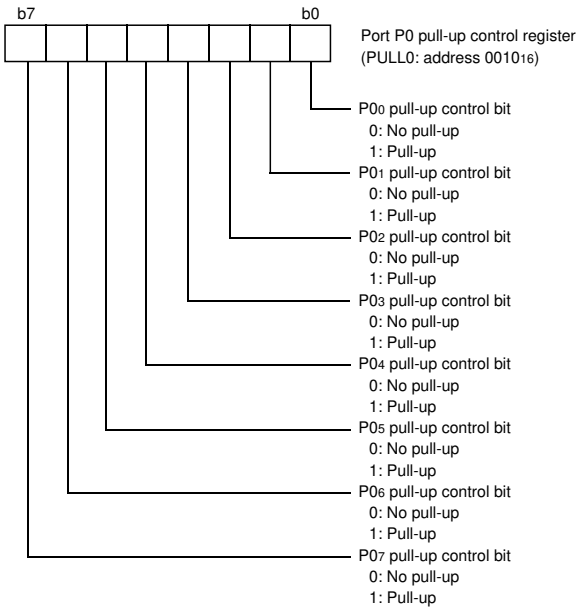
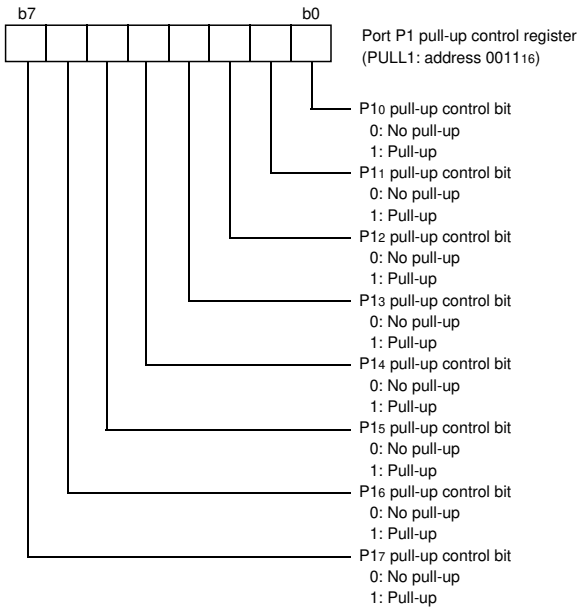


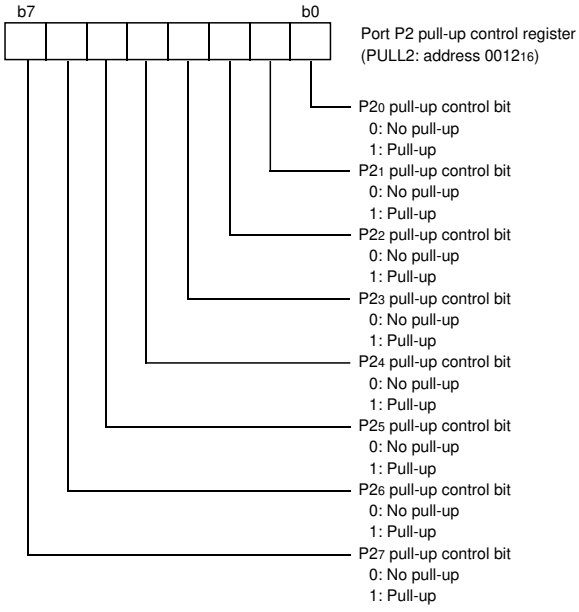
Fig. 12 Port block diagram (3)



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

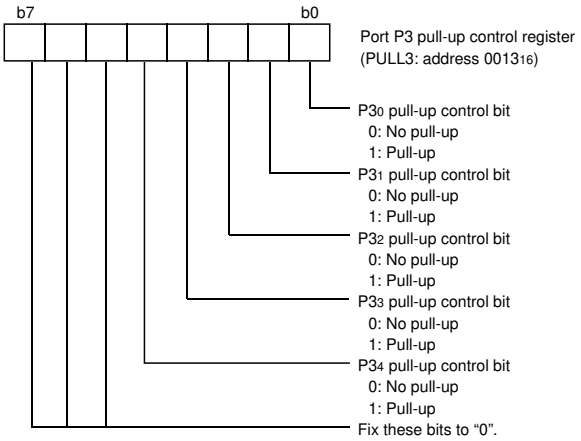


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

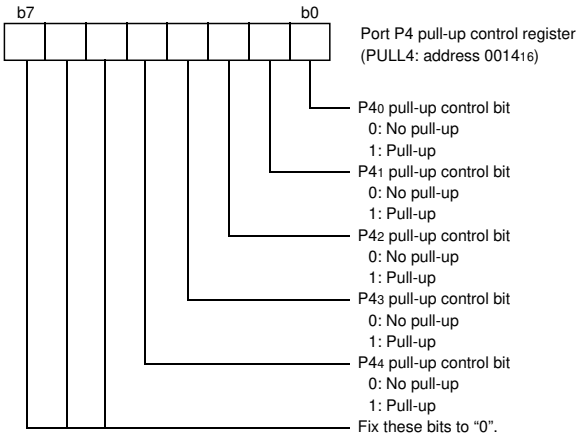


Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 13 Structure of port registers (1)



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.



Note: Pull-up control is valid when the corresponding bit of the port direction register is "0" (input).
When that bit is "1" (output), pull-up cannot be set to the port of which pull-up is selected.

Fig. 14 Structure of port registers (2)

INTERRUPTS

The 3858 group's interrupts are a type of vector and occur by 16 sources among 19 sources: eight external, ten internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Interrupt Source Selection

Which of each combination of the following interrupt sources can be selected by the interrupt source selection register (address 0039_{16}).

1. INT_3 or Serial I/O2
2. Timer Z1 or $CNTR_2$
3. Timer Z2 or $CNTR_3$
4. $CNTR_0$ or $CNTR_2$
5. $CNTR_1$ or $CNTR_3$

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Timer Z1	3	FFF916	FFF816	At timer Z1 underflow	
CNTR2				At detection of either rising or falling edge of CNTR2 input	External interrupt (active edge selectable)
INT1	4	FFF716	FFF616	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	5	FFF516	FFF416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	6	FFF316	FFF216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
Serial I/O2				At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Timer Z2	7	FFF116	FFF016	At timer Z2 underflow	
CNTR3				At detection of either rising or falling edge of CNTR3 input	External interrupt (active edge selectable)
Timer X	8	FFEF16	FFEE16	At timer X underflow	
Timer Y	9	FFED16	FFEC16	At timer Y underflow	
Timer 1	10	FFEB16	FFEA16	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE916	FFE816	At timer 2 underflow	
Serial I/O1 reception	12	FFE716	FFE616	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	13	FFE516	FFE416	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
CNTR0	14	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR2				At detection of either rising or falling edge of CNTR2 input	
CNTR1	15	FFE116	FFE016	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
CNTR3				At detection of either rising or falling edge of CNTR3 input	
A/D converter	16	FFDF16	FFDE16	At completion of A/D conversion	
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

■ Notes

When setting the followings, the interrupt request bit may be set to "1".

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address 003A16)
Timer XY mode register (address 002316)
Timer Z1 mode register (address 002816)
Timer Z2 mode register (address 002B16)

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt source selection register (address 003616)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to "0" (disabled).
②Set the interrupt edge select bit or the interrupt source select bit to "1".
③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to "1" (enabled).

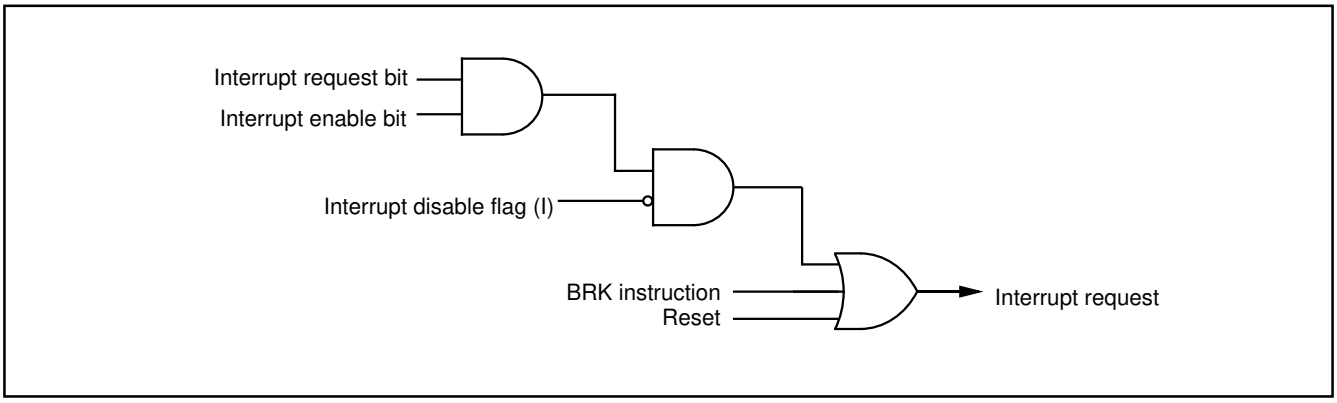


Fig. 15 Interrupt control

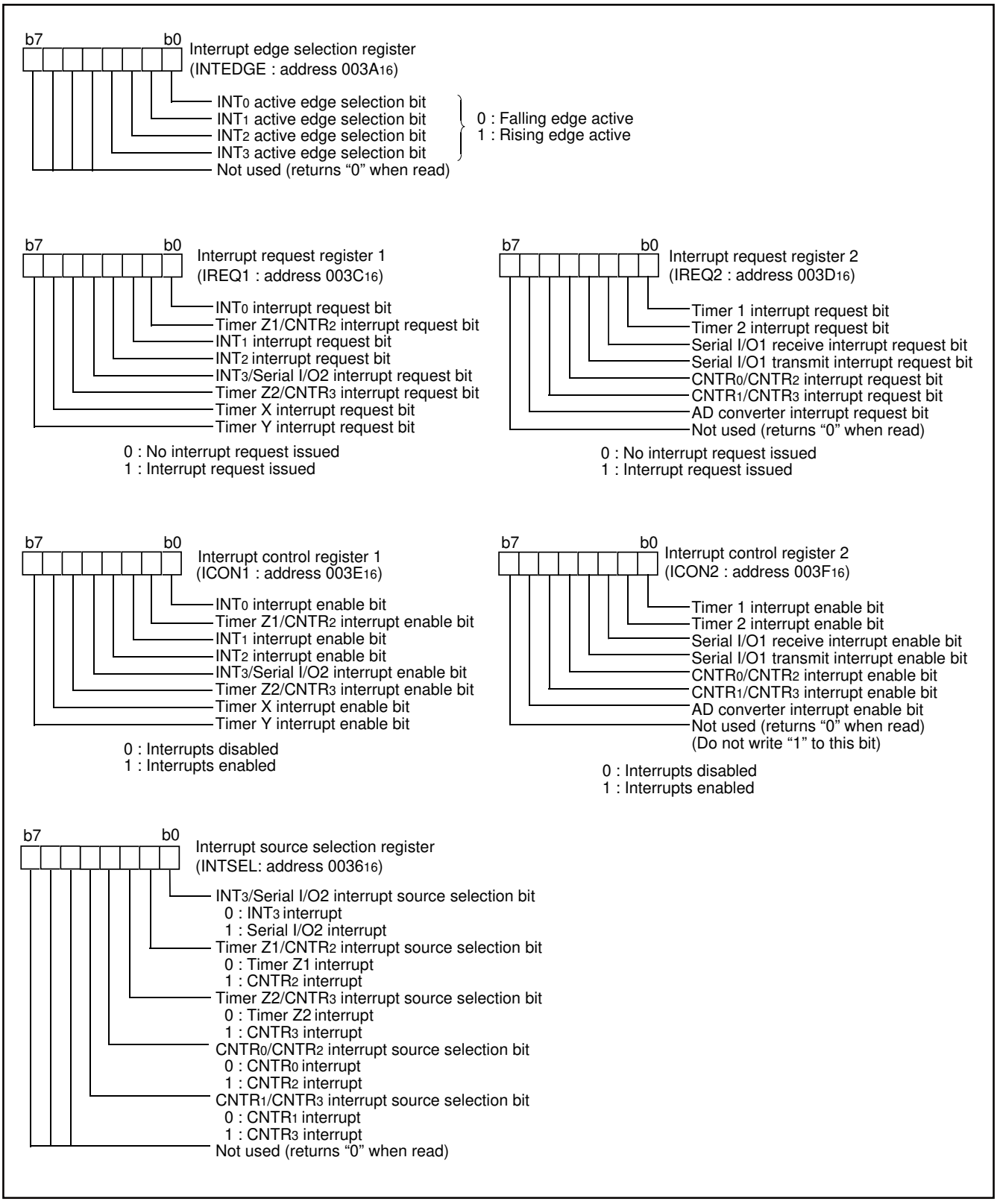


Fig. 16 Structure of interrupt-related registers

TIMERS

●8-bit Timers

The 3858 group has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are down-counters. When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

●Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B$_{16}$). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are "10" (low-speed mode), X_{CIN} is selected.

●Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register (address 002E$_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of f(X_{IN}) or f(X_{CIN}).

Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

●Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or f(X_{CIN}). The count source is selected by the timer 12, X count source selection register (address 002E$_{16}$) and the timer Y, Z1 count source selection register (address 002F$_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of f(X_{IN}) or f(X_{CIN}); and f(X_{CIN}).

Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023$_{16}$).

(1) Timer mode

●Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

●Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023$_{16}$).

When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse output mode

●Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from $CNTR_0$/$CNTR_1$ pin. Regardless of the timer counting or not the output of $CNTR_0$/$CNTR_1$ pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the $CNTR_0$ active edge switch bit (bit 2) and the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023$_{16}$) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

Switching the $CNTR_0$ or $CNTR_1$ active edge switch bit will reverse the output level of the corresponding $CNTR_0$ or CNTR1 pin.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P2_7$/$P4_0$ to output in this mode.

(3) Event counter mode

●Mode selection

This mode can be selected by setting “10” to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

The operation is the same as the timer mode’s except that the timer counts signals input from the $CNTR_0$ or $CNTR_1$ pin. The valid edge for the count operation depends on the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}). When it is “0”, the rising edge is valid. When it is “1”, the falling edge is valid.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P2_7$/$P4_0$ to input in this mode.

(4) Pulse width measurement mode

●Mode selection

This mode can be selected by setting “11” to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023_{16}).

●Explanation of operation

When the $CNTR_0$ active edge switch bit (bit 2) or the $CNTR_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023_{16}) is “1”, the timer counts during the term of one falling edge of $CNTR_0$/$CNTR_1$ pin input until the next rising edge of input (“L” term). When it is “0”, the timer counts during the term of one rising edge input until the next falling edge input (“H” term).

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin and port $P2_7$/$P4_0$ to input in this mode.

The count operation can be stopped by setting “1” to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023_{16}). The interrupt request bit is set to “1” each time the timer underflows.

•Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.