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Mach® 4 CPLD Device Datasheet

June 2010

Select Devices Discontinued!

Product Change Notifications (PCNs) have been issued to convert or discontinue select devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
M4-32/32	M4-32/32-7JC	Converted to M4A5	Contact pcn@latticesemi.com for more info.
	M4-32/32-10JC		
	M4-32/32-12JC		
	M4-32/32-15JC		
	M4-32/32-10JI		
	M4-32/32-12JI		
	M4-32/32-14JI		
	M4-32/32-18JI		
	M4-32/32-7VC		
	M4-32/32-10VC		
	M4-32/32-12VC		
	M4-32/32-15VC		
	M4-32/32-10VI		
	M4-32/32-12VI		
	M4-32/32-14VI		
	M4-32/32-18VI		
	M4-32/32-7VC48		
	M4-32/32-10VC48		
	M4-32/32-12VC48		
	M4-32/32-15VC48		
	M4-32/32-10VI48		
	M4-32/32-12VI48		
	M4-32/32-14VI48		
	M4-32/32-18VI48		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4-64/32	M4-64/32-7JC	Converted to M4A5	Contact pcn@latticesemi.com for more info.
	M4-64/32-10JC		
	M4-64/32-12JC		
	M4-64/32-15JC		
	M4-64/32-10JI		
	M4-64/32-12JI		
	M4-64/32-14JI		
	M4-64/32-18JI		
	M4-64/32-7VC		
	M4-64/32-10VC		
	M4-64/32-12VC		
	M4-64/32-15VC		
	M4-64/32-10VI		
	M4-64/32-12VI		
	M4-64/32-14VI		
	M4-64/32-18VI		
	M4-64/32-7VC48		
	M4-64/32-10VC48		
	M4-64/32-12VC48		
	M4-64/32-15VC48		
	M4-64/32-10VI48		
	M4-64/32-12VI48		
	M4-64/32-14VI48		
	M4-64/32-18VI48		
M4-96/48	M4-96/48-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-96/48-10VC		
	M4-96/48-12VC		
	M4-96/48-15VC		
	M4-96/48-10VI		
	M4-96/48-12VI		
	M4-96/48-14VI		
	M4-96/48-18VI		
M4-128/64	M4-128/64-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10YC		
	M4-128/64-12YC		
	M4-128/64-15YC		
	M4-128/64-10YI		
	M4-128/64-12YI		
	M4-128/64-14YI		
	M4-128/64-18YI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4-128/64 (Cont'd)	M4-128/64-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10VC		
	M4-128/64-12VC		
	M4-128/64-15VC		
	M4-128/64-10VI		
	M4-128/64-12VI		
	M4-128/64-14VI		
	M4-128/64-18VI		
M4-128N/64	M4-128N/64-7JC	Active / Orderable	
	M4-128N/64-10JC		
	M4-128N/64-12JC		
	M4-128N/64-15JC		
	M4-128N/64-10JI		
	M4-128N/64-12JI		
	M4-128N/64-14JI		
	M4-128N/64-18JI		
M4-192/96	M4-192/96-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-192/96-10VC		
	M4-192/96-12VC		
	M4-192/96-15VC		
	M4-192/96-10VI		
	M4-192/96-12VI		
	M4-192/96-14VI		
	M4-192/96-18VI		
M4-256/128	M4-256/128-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-256/128-10YC		
	M4-256/128-12YC		
	M4-256/128-15YC		
	M4-256/128-10YI		
	M4-256/128-12YI		
	M4-256/128-14YI		
	M4-256/128-18YI		
M4LV-32/32	M4LV-32/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10JC		
	M4LV-32/32-12JC		
	M4LV-32/32-15JC		
	M4LV-32/32-10JI		
	M4LV-32/32-12JI		
	M4LV-32/32-14JI		
	M4LV-32/32-18JI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-32/32 (Cont'd)	M4LV-32/32-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10VC		
	M4LV-32/32-12VC		
	M4LV-32/32-15VC		
	M4LV-32/32-10VI		
	M4LV-32/32-12VI		
	M4LV-32/32-14VI		
	M4LV-32/32-18VI		
	M4LV-32/32-7VC48		
	M4LV-32/32-10VC48		
	M4LV-32/32-12VC48		
	M4LV-32/32-15VC48		
	M4LV-32/32-10VI48		
	M4LV-32/32-12VI48		
	M4LV-32/32-14VI48		
	M4LV-32/32-18VI48		
M4LV-64/32	M4LV-64/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-64/32-10JC		
	M4LV-64/32-12JC		
	M4LV-64/32-15JC		
	M4LV-64/32-10JI		
	M4LV-64/32-12JI		
	M4LV-64/32-14JI		
	M4LV-64/32-18JI		
	M4LV-64/32-7VC		
	M4LV-64/32-10VC		
	M4LV-64/32-12VC		
	M4LV-64/32-15VC		
	M4LV-64/32-10VI		
	M4LV-64/32-12VI		
	M4LV-64/32-14VI		
	M4LV-64/32-18VI		
	M4LV-64/32-7VC48		
	M4LV-64/32-10VC48		
	M4LV-64/32-12VC48		
	M4LV-64/32-15VC48		
	M4LV-64/32-10VI48		
	M4LV-64/32-12VI48		
	M4LV-64/32-14VI48		
	M4LV-64/32-18VI48		

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-96/48	M4LV-96/48-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-96/48-10VC		
	M4LV-96/48-12VC		
	M4LV-96/48-15VC		
	M4LV-96/48-10VI		
	M4LV-96/48-12VI		
	M4LV-96/48-14VI		
	M4LV-96/48-18VI		
M4LV-128/64	M4LV-128/64-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10YC		
	M4LV-128/64-12YC		
	M4LV-128/64-15YC		
	M4LV-128/64-10YI		
	M4LV-128/64-12YI		
	M4LV-128/64-14YI		
	M4LV-128/64-18YI		
	M4LV-128/64-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10VC		
	M4LV-128/64-12VC		
	M4LV-128/64-15VC		
	M4LV-128/64-10VI		
	M4LV-128/64-12VI		
	M4LV-128/64-14VI		
	M4LV-128/64-18VI		
M4LV-128N/64	M4LV-128N/64-7JC	**Discontinued**	PCN#09-10
	M4LV-128N/64-10JC		
	M4LV-128N/64-12JC		
	M4LV-128N/64-15JC		
	M4LV-128N/64-10JI		
	M4LV-128N/64-12JI		
	M4LV-128N/64-14JI		
	M4LV-128N/64-18JI		
M4LV-192/96	M4LV-192/96-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-192/96-10VC		
	M4LV-192/96-12VC		
	M4LV-192/96-15VC		
	M4LV-192/96-10VI		
	M4LV-192/96-12VI		
	M4LV-192/96-14VI		
	M4LV-192/96-18VI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-256/128	M4LV-256/128-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-256/128-10YC		
	M4LV-256/128-12YC		
	M4LV-256/128-15YC		
	M4LV-256/128-10YI		
	M4LV-256/128-12YI		
	M4LV-256/128-14YI		
	M4LV-256/128-18YI		
	M4LV-256/128-7AC		
	M4LV-256/128-10AC		
	M4LV-256/128-12AC		
	M4LV-256/128-15AC		
	M4LV-256/128-10AI		
	M4LV-256/128-12AI		
	M4LV-256/128-14AI		
	M4LV-256/128-18AI		

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MACH 4 CPLD Family

High Performance E^{2}CMOS® In-System Programmable Logic

FEATURES

- **High-performance, E^{2}CMOS 3.3-V & 5-V CPLD families**
- **Flexible architecture for rapid logic designs**
  - — Excellent First-Time-Fit™ and refit feature
  - — SpeedLocking™ performance for guaranteed fixed timing
  - — Central, input and output switch matrices for 100% routability and 100% pin-out retention
- **High speed**
  - — 7.5ns t_{PD} Commercial and 10ns t_{PD} Industrial
  - — 111.1MHz f_{CNT}
- **32 to 256 macrocells; 32 to 384 registers**
- **44 to 256 pins in PLCC, PQFP, TQFP and BGA packages**
- **Flexible architecture for a wide range of design styles**
  - — D/T registers and latches
  - — Synchronous or asynchronous mode
  - — Dedicated input registers
  - — Programmable polarity
  - — Reset/ preset swapping
- **Advanced capabilities for easy system integration**
  - — 3.3-V & 5-V JEDEC-compliant operations
  - — JTAG (IEEE 1149.1) compliant for boundary scan testing
  - — 3.3-V & 5-V JTAG in-system programming
  - — PCI compliant (-7/-10/-12 speed grades)
  - — Safe for mixed supply voltage system designs
  - — Bus-Friendly™ inputs and I/Os
  - — Programmable security bit
  - — Individual output slew rate control
- **Advanced E^{2}CMOS process provides high-performance, cost-effective solutions**
- **Supported by ispDesignEXPERT™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for MACH 4
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Lattice and third-party hardware programming support**
  - — LatticePRO™ software for in-system programmability support on PCs and automated test equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

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Table 1. MACH 4 Device Features[1, 2]

Feature	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4-256/128 M4LV-256/128
Macrocells	32	64	96	128	128	192	256
Maximum User I/O Pins	32	32	48	64	64	96	128
t_{PD} (ns)	7.5	7.5	7.5	7.5	7.5	7.5	7.5
f_{CNT} (MHz)	111	111	111	111	111	111	111
t_{COS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
t_{SS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Static Power (mA)	25	25	50	70	70	85	100
JTAG Compliant	Yes	Yes	Yes	Yes	No	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. *For information on the M4-96/96 device, please refer to the M4-96/96 data sheet at www.latticesemi.com.*
2. *"M4-xxx" is for 5-V devices. "M4LV-xxx" is for 3.3-V devices.*

GENERAL DESCRIPTION

The MACH® 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-18
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	I
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	I
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	I
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	I
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	I
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	I
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	I

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. MACH 4 Package and I/O Options (Number of I/Os and dedicated inputs in Table)

Package	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4LV-256/128
44-pin PLCC	32+2	32+2					
44-pin TQFP	32+2	32+2					
48-pin TQFP	32+2	32+2					
84-pin PLCC					64+6		
100-pin TQFP			48+8	64+6			
100-pin PQFP				64+6			
144-pin TQFP						96+16	
208-pin PQFP							128+14
256-ball BGA							128+14

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4 architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

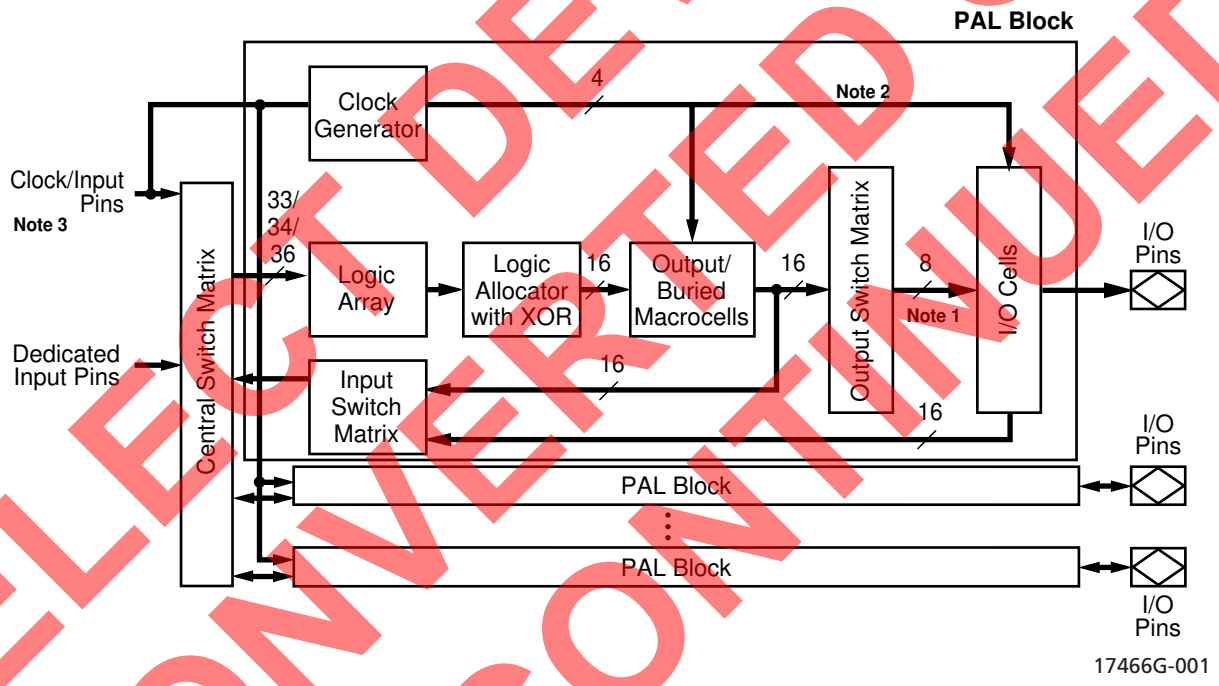


Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for MACH 4 devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32.*
3. *M4(LV)-192/96 and M4(LV)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

Table 4. Architectural Summary of MACH 4 devices

	MACH 4 Devices	
	M4-64/32, M4LV-64/32 M4-96/48, M4LV-96/48 M4-128/64, M4LV-128/64 M4-128N/64, M4LV-128N/64 M4-192/96, M4LV-192/96 M4-256/128, M4LV-256/128	M4-32/32 M4LV-32/32
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4-32/32 and M4LV-32/32	33
M4-64/32 and M4LV-64/32	33
M4-96/48 and M4LV-96/48	33
M4-128/64 and M4LV-128/64	33
M4-128N/64 and M4LV-128N/64	33
M4-192/96 and M4LV-192/96	34
M4-256/128 and M4LV-256/128	34

Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

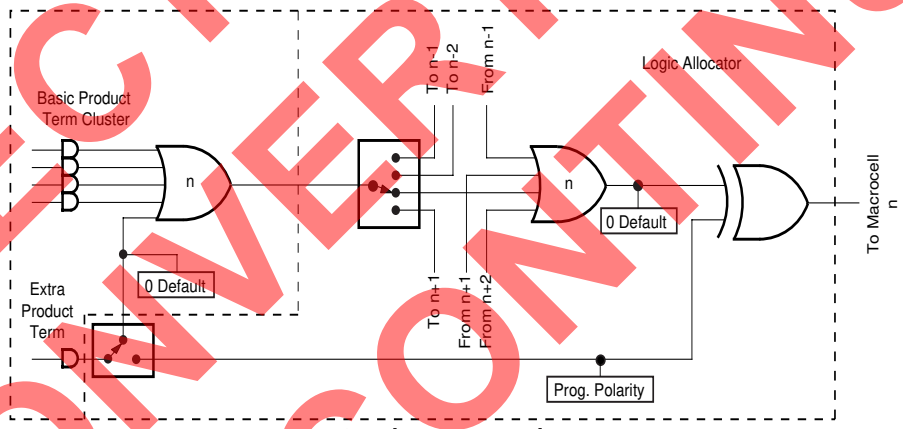
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

Table 6. Logic Allocator for All MACH 4 Devices (except M4(LV)-32/32)

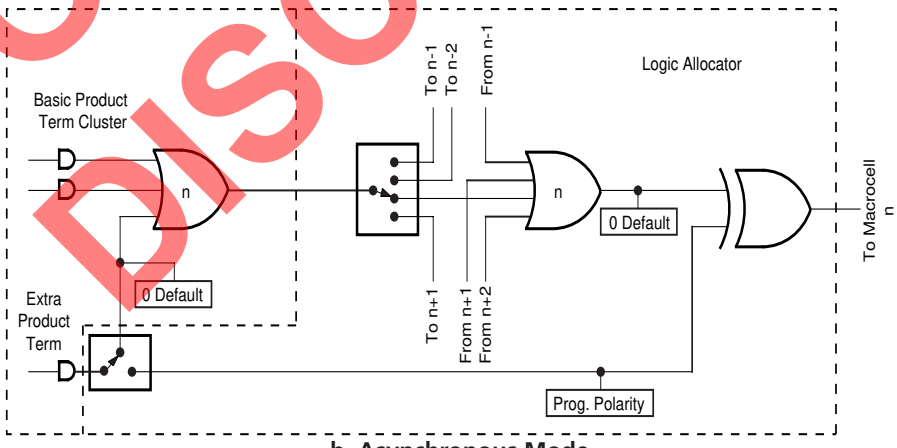
Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_7, C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7, C_8	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8, C_9	M_{15}	C_{14}, C_{15}

Table 7. Logic Allocator for M4(LV)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}



a. Synchronous Mode



b. Asynchronous Mode

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Figure 2. Logic Allocator: Configuration of Cluster "n" Set by Mode of Macrocell "n"

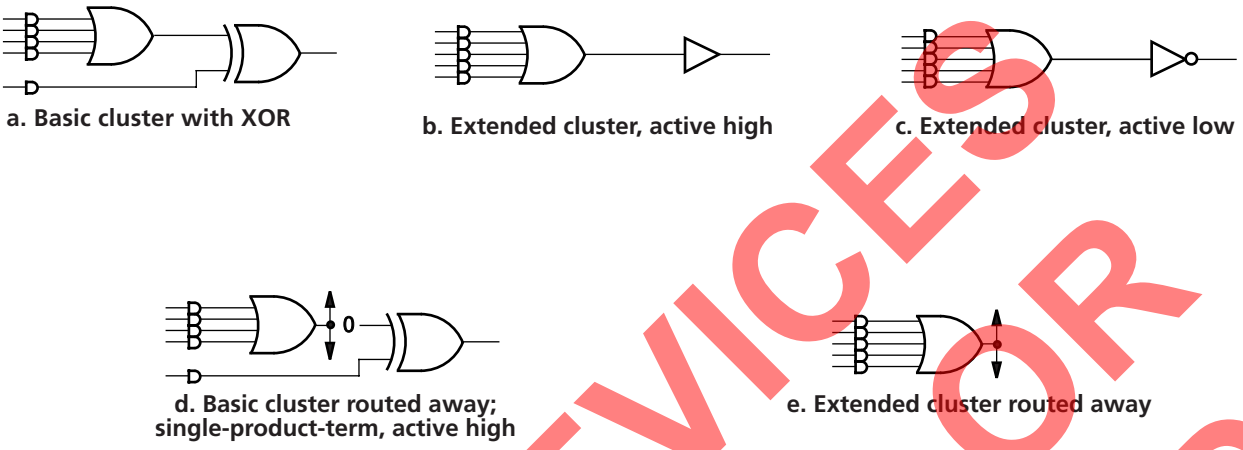


Figure 3. Logic Allocator Configurations: Synchronous Mode

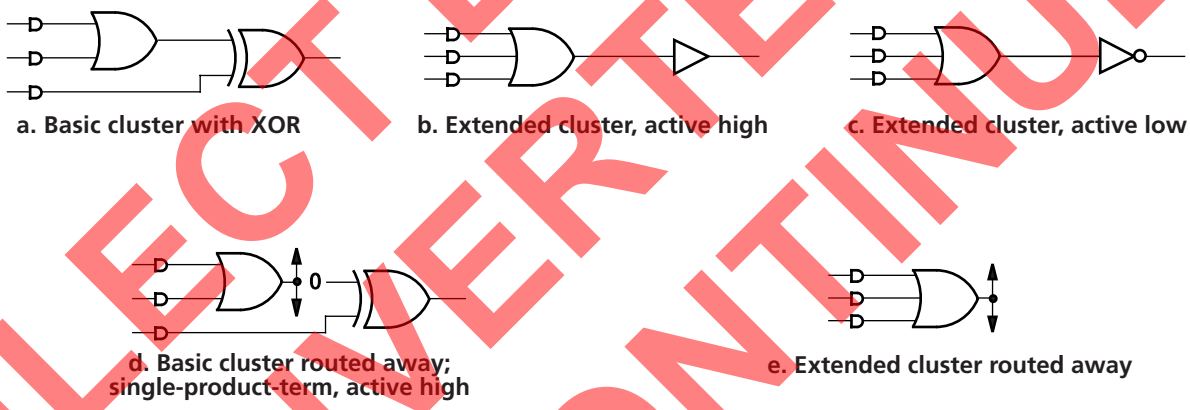


Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.

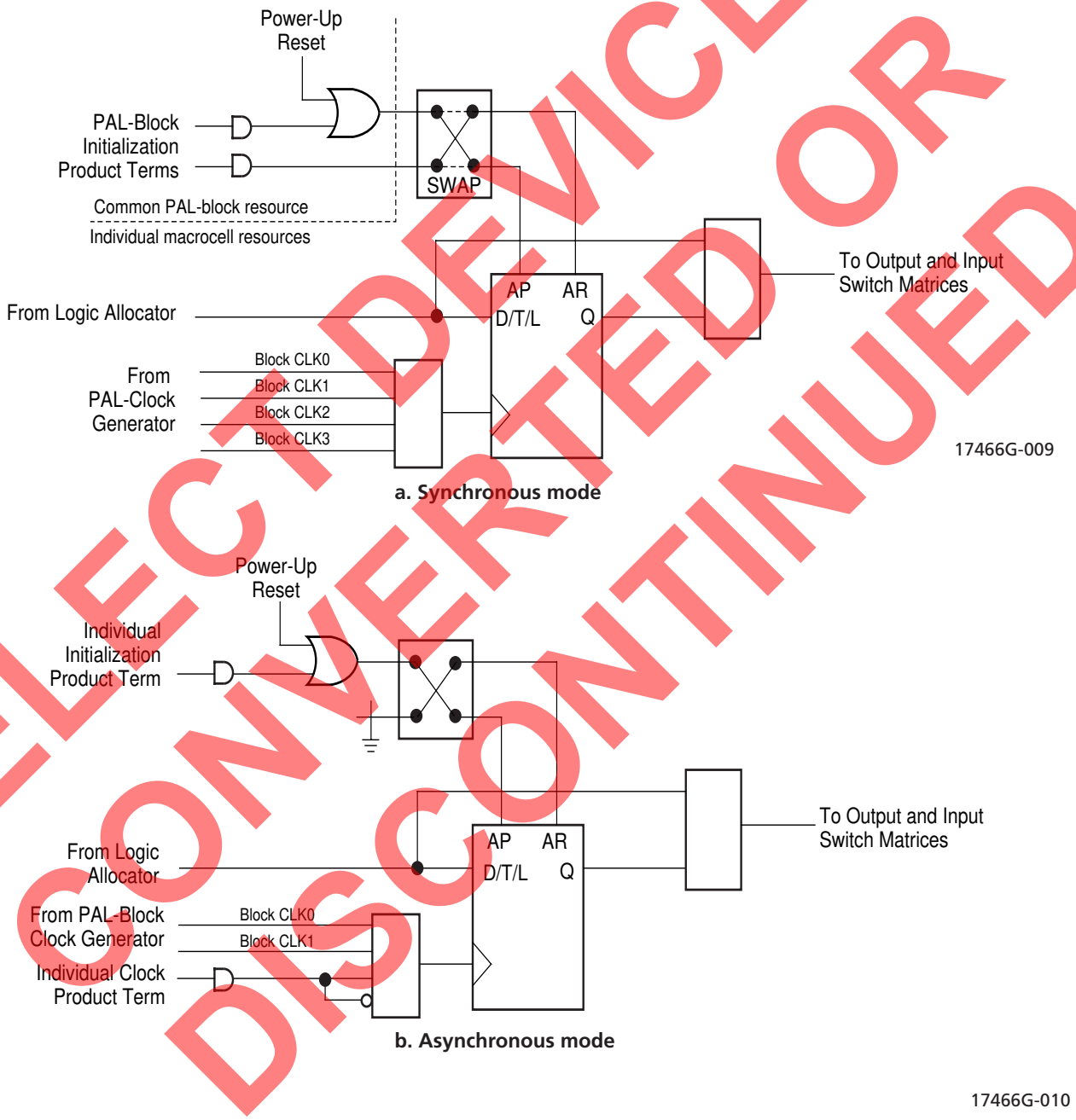
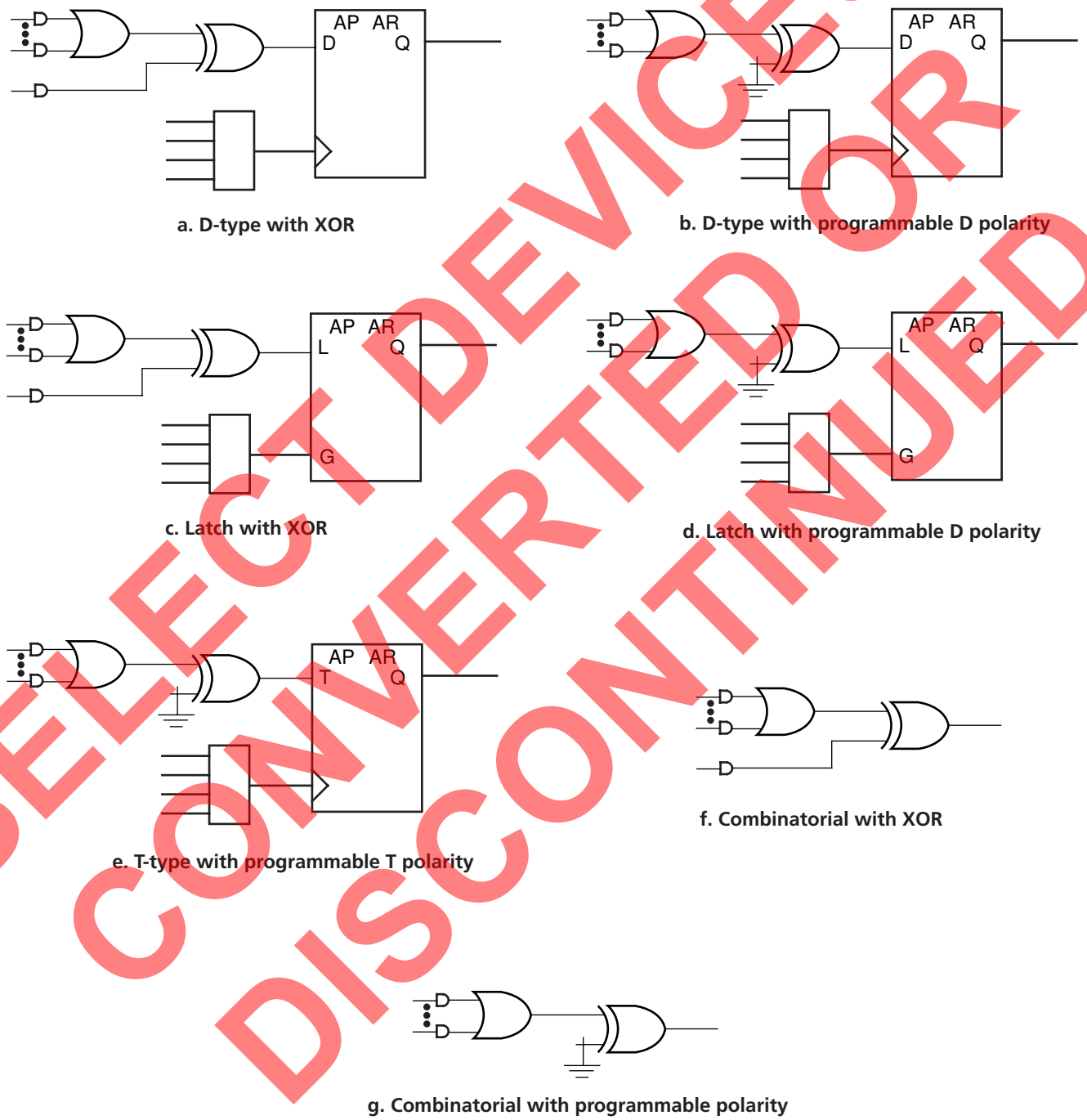


Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



a. D-type with XOR

b. D-type with programmable D polarity

c. Latch with XOR

d. Latch with programmable D polarity

e. T-type with programmable T polarity

f. Combinatorial with XOR

g. Combinatorial with programmable polarity

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Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

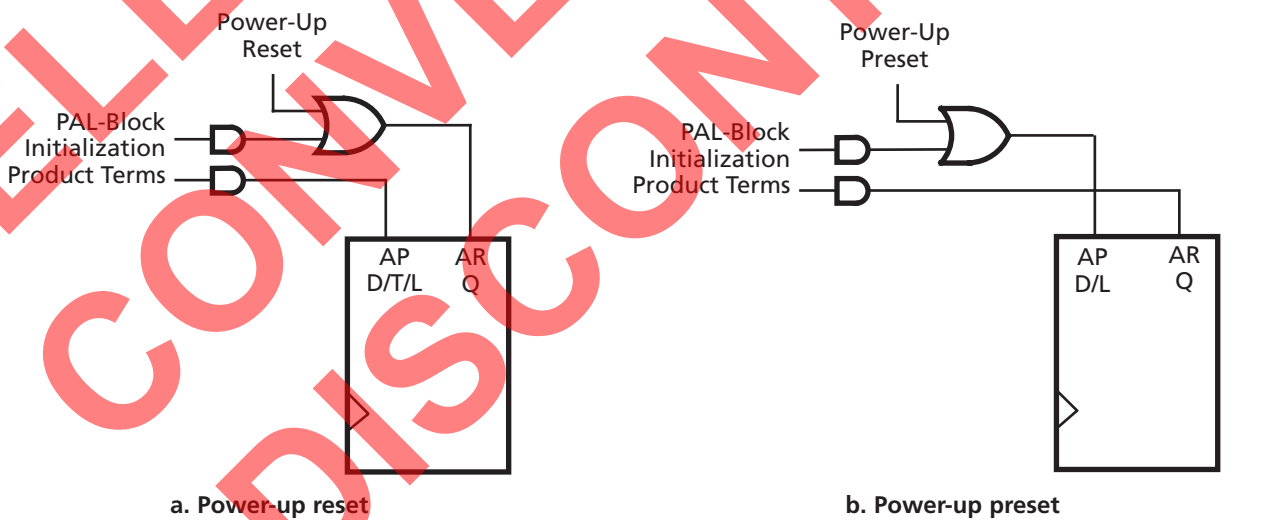
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

b. Power-up preset

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17466G-013

Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.

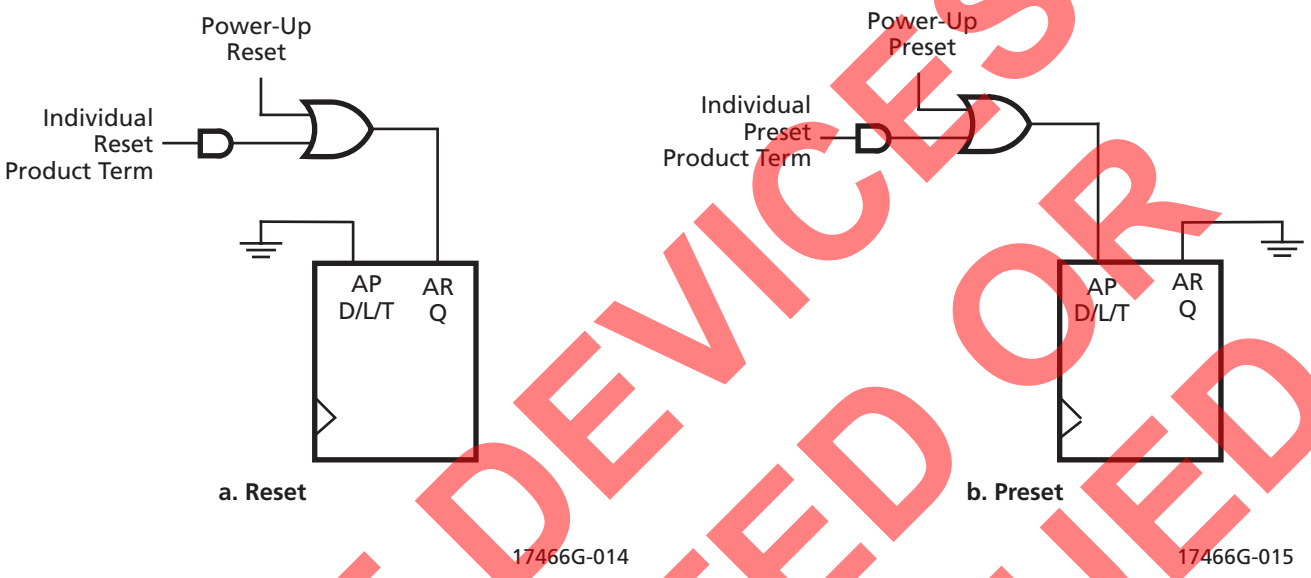


Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

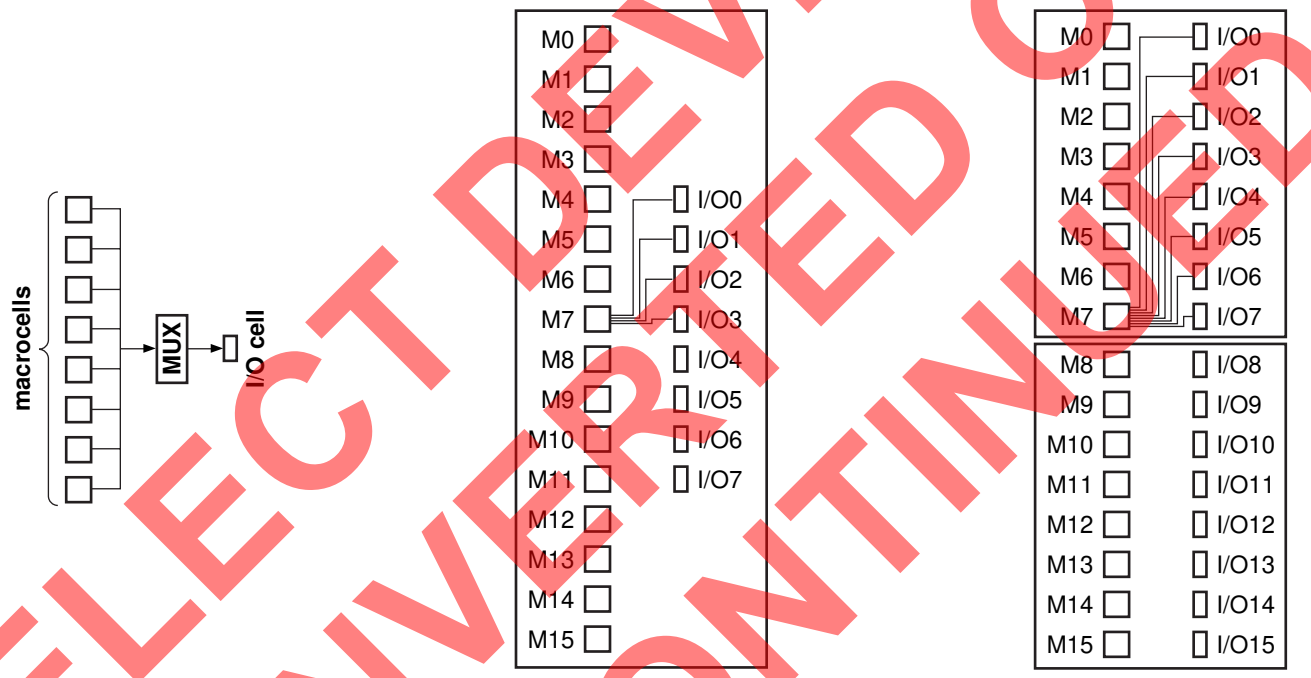
Note:

1. Transparent latch is unaffected by AR, AP

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In MACH 4 devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The MACH 4 devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).



Each I/O cell can choose one of 8 macrocells in all MACH 4 devices.

Each macrocell can drive one of 4 I/O cells in MACH 4 devices with 2:1 macrocell-I/O cell ratio.

Each macrocell can drive one of 8 I/O cells in M4(LV)-32/32 devices.

Figure 9. MACH 4 Output Switch Matrix

Table 10. Output Switch Matrix Combinations for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4(LV)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except MACH 4 devices with 1:1 macrocell-I/O cell ratio.) An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

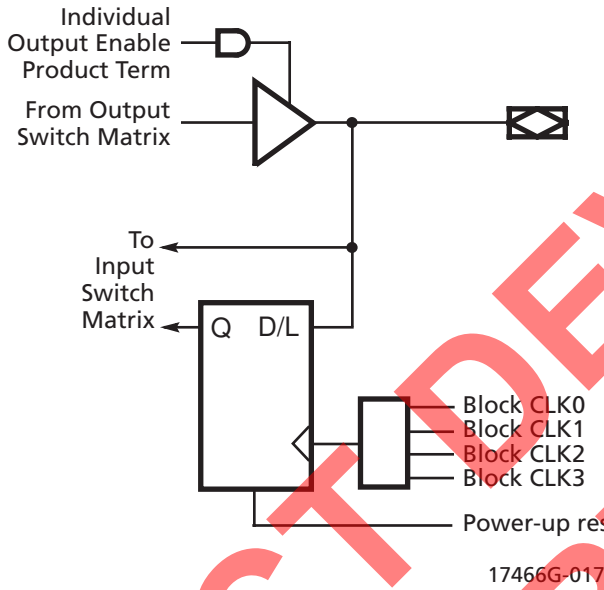


Figure 10. I/O Cell for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

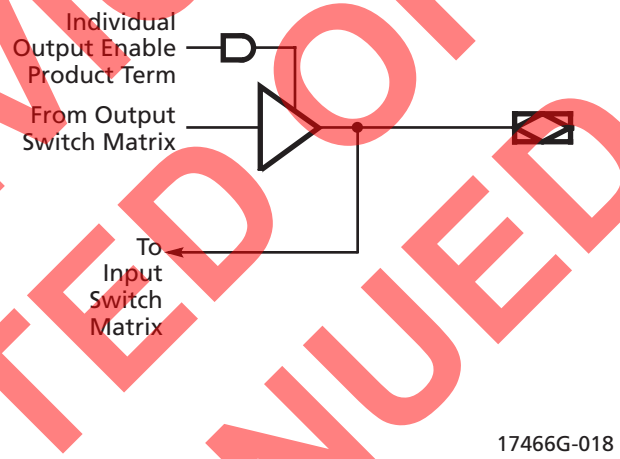


Figure 11. I/O Cell for MACH 4 Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

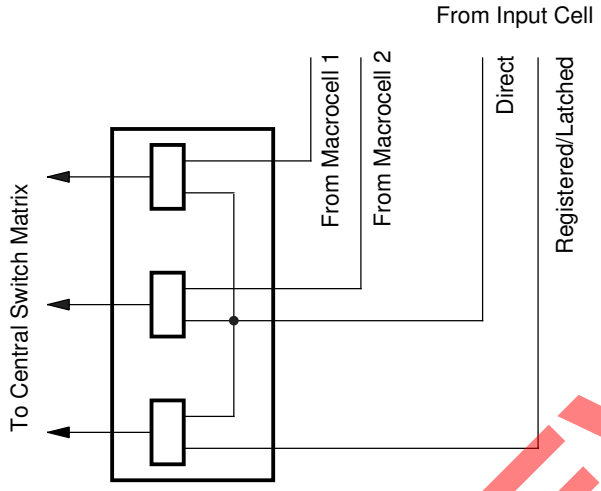


Figure 12. MACH 4 with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

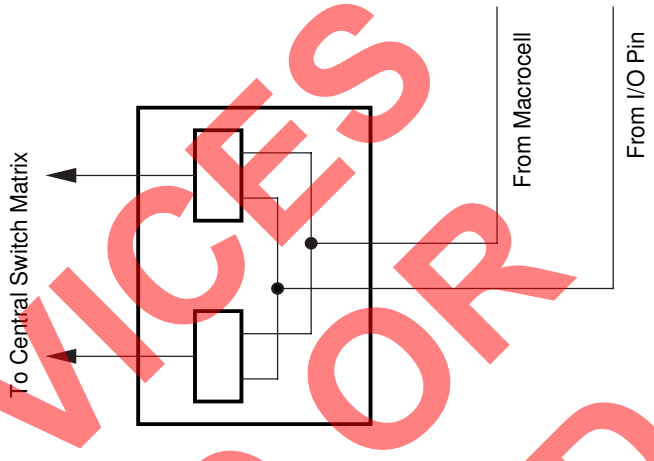


Figure 13. MACH 4 with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 12 lists the possible combinations.

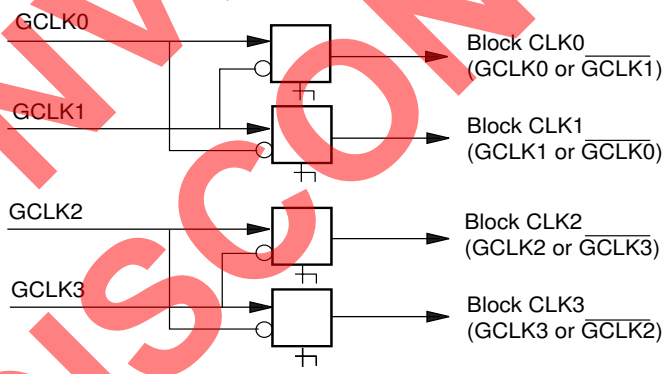


Figure 14. PAL Block Clock Generator [1]

Note:

1. *M4(LV)-32/32 and M4(LV)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

Table 12. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4(LV)-32/32 and M4(LV)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 4 timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

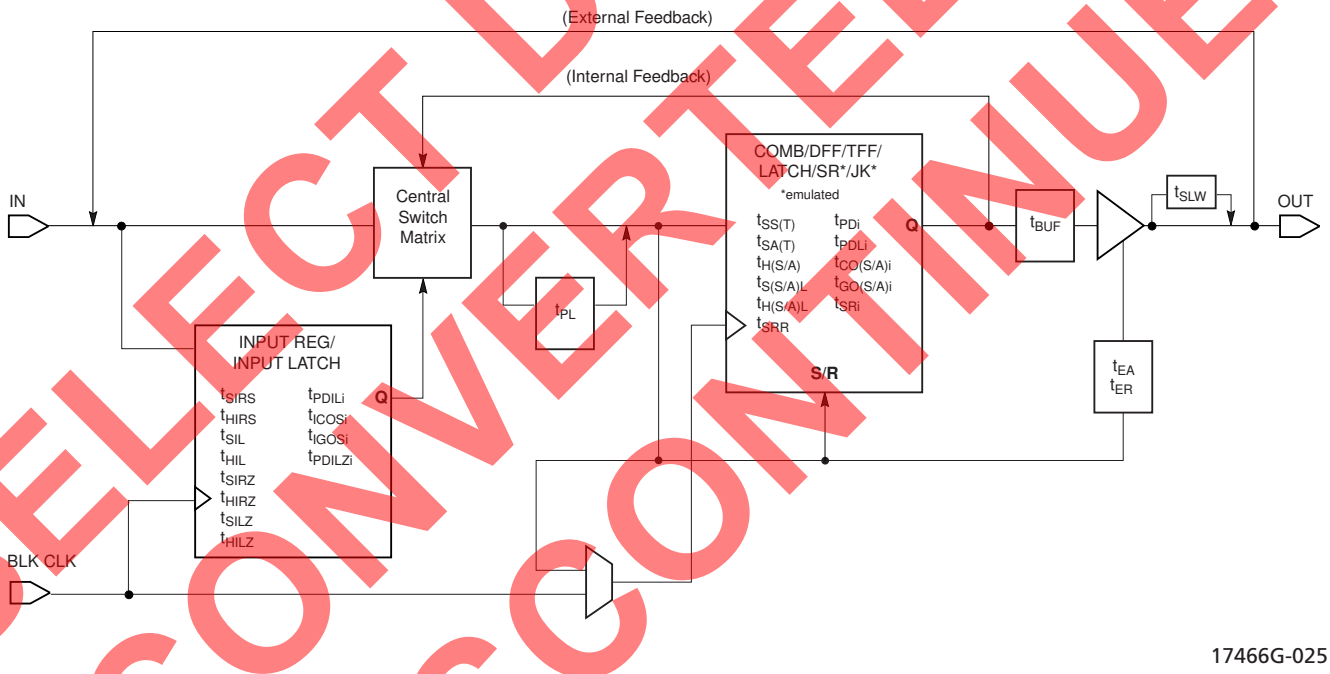


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Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.