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M41ST85W

3.0/3.3 V I²C combination serial RTC, NVRAM supervisor and microprocessor supervisor

Features

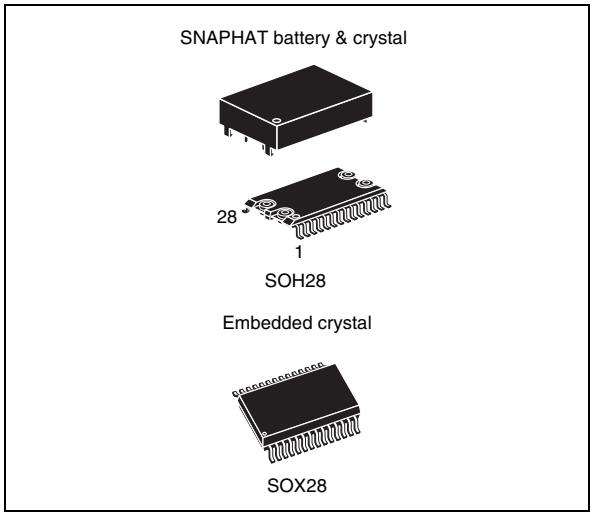
- Automatic battery switchover and WRITE protect for:
  - Internal serial RTC and
  - External low power SRAM (LPSRAM)
- 400 kHz I²C serial interface
- 3.0/3.3 V operating voltage
  - V_{CC} = 2.7 to 3.6 V
- Ultralow battery supply current of 500 nA (max)
- RoHS compliant
  - Lead-free second level interconnect

Serial RTC features

- 400 kHz I²C
- 44 bytes of general purpose NVRAM
- Counters for:
  - Seconds, minutes, hours, day, date, month, and year
  - Century
  - Tenths/hundredths of seconds
  - Clock calibration register allows compensation for crystal variations over temperature
- Programmable alarm with repeat modes
  - Functions in battery back-up mode
- Power-down timestamp (HT bit)
- 2.5 to 5.5 V oscillator operating voltage

Microprocessor supervisor features

- Programmable watchdog
  - 62.5 ms to 128 s time-out period
- Early power-fail warning circuit (PFI/PFO) with 1.25 V precision reference



- Power-on reset/low voltage detect
  - Open drain reset output
  - Reset voltage, V_{PFD} = 2.60 V (nom)
  - Two reset input pins
  - Watchdog can be steered to reset output

NVRAM supervisor features

- Non-volatizes external LPSRAM
  - Automatically switches to back-up battery and deselects (write-protects) external LPSRAM via chip-enable gate
  - Power-fail deselect (write protect) voltage, V_{PFD} = 2.60 V (nom)
  - Switchover, V_{SO} = 2.50 V (nom)
- Battery monitor (battery low flag)

Other features

- Programmable squarewave generator (1 Hz to 32 KHz)
- –40°C to +85°C operation
- Package options:
  - 28-lead SNAPHAT® IC (SOH28) SNAPHAT battery/crystal top to be ordered separately
  - 28-lead embedded crystal SOIC (SOX28)

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1 Description

The M41ST85W is a combination serial real-time clock, microprocessor supervisor, and NVRAM supervisor. It is built in a low-power CMOS SRAM process and has a 64-byte memory space with 44 bytes of NVRAM and 20 memory-mapped RTC registers (see *Table 2 on page 20*). The RTC registers are configured in binary coded decimal (BCD) format.

The M41ST85W combines a 400 kHz I^2C serial RTC with an automatic backup battery switchover circuit for powering an external LPSRAM as well as the internal RTC. When power begins to fail, the switchover automatically connects to the backup battery to keep the RTC and external LPSRAM alive in the absence of system power. Access to the LPSRAM is also cut off via a chip-enable gate function, thereby write-protecting the memory. A programmable watchdog and power-on reset/low voltage detect function are the key elements in the microprocessor supervisor section.

The real-time clock includes a built-in 32.768 kHz oscillator (crystal-controlled), which provides the time base for the timekeeping and calendar functions. Eight of the 20 clock registers provide the basic clock/calendar functions while the other 12 bytes provide status/control for the alarm, watchdog, and squarewave functions.

RTC addresses and data are transferred serially via the two-line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41ST85W has a built-in power sense circuit which detects power failures and automatically switches to the backup battery when a power failure occurs. During an outage, the power to sustain the SRAM and clock operations is typically supplied by a small lithium button-cell battery as is the case when using the SNAPHAT® package option.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, watchdog timer, and programmable squarewave generator. Other features include a power-on reset as well as two additional debounce reset inputs ($\overline{\text{RSTIN1}}$ and $\overline{\text{RSTIN2}}$) which can also generate an output reset ($\overline{\text{RST}}$).

The eight registers for basic clock/calendar functions contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The M41ST85W is offered in two 28-lead SOIC packages. The 300 mil SOH28 SNAPHAT® IC package mates with ST's SNAPHAT battery/crystal top (ordered separately). SNAPHAT battery options include 48 mAh and 120 mAh. ST's 300 mil SOX28 embedded crystal IC includes the 32 KHz crystal and is perfect for applications where a low profile is a must.

The SOH28 SNAPHAT SOIC includes sockets with gold plated contacts at both ends for direct connection to the SNAPHAT top. The SNAPHAT battery/crystal top is inserted atop the IC package after the completion of the surface mount assembly process which avoids potential battery and crystal damage due to the high temperatures required for device surface-mounting. The unique design allows the battery to be replaced, thus extending the life of the RTC and NVRAM indefinitely.

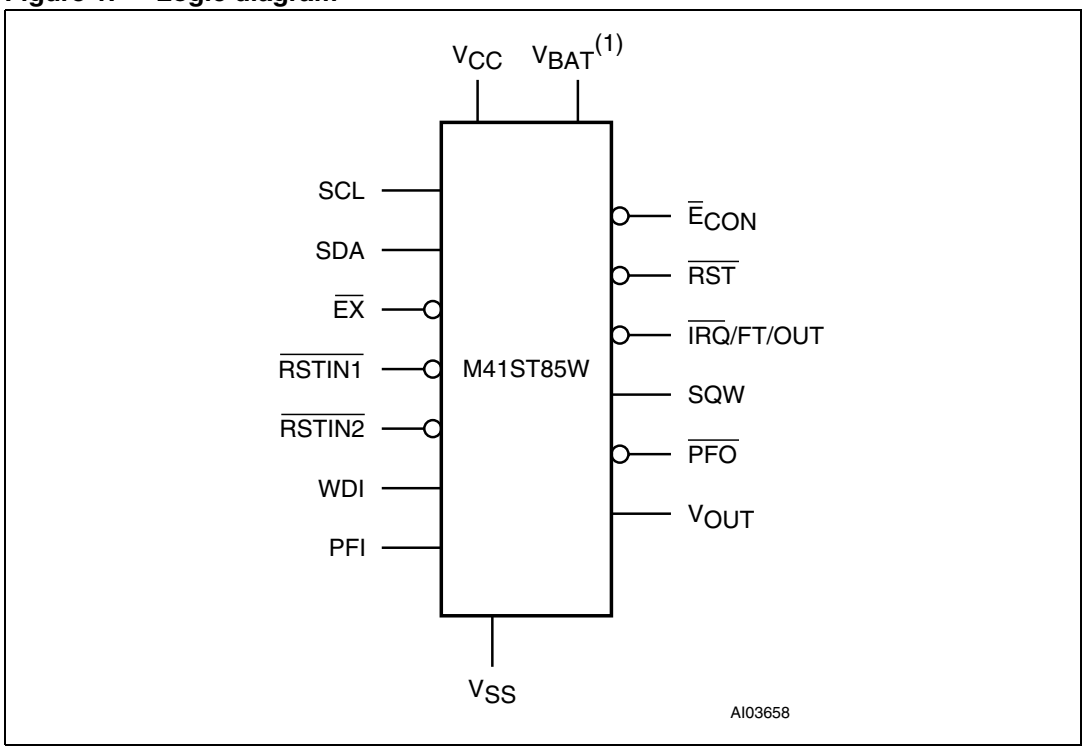
The SNAPHAT top is keyed to prevent reverse insertion. The SNAPHAT IC and SNAPHAT tops are shipped separately. The ICs are available in plastic anti-static tubes or in tape & reel form. The SNAPHAT tops are shipped in plastic anti-static tubes. The part numbers are

M4T28-BR12SH1 (48 mAh) and M4T32-BR12SH1 (120 mAh). For the extended temperature requirement, the 120 mAh M4T32-BR12SH6 is available. For more information, see *Table 21 on page 40*.

Caution: Do not place the SNAPHAT® battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

The 300 mil SOX embedded crystal SOIC typically requires a user-supplied battery for non-volatile operation. Capacitor backup can also be implemented with this package.

Figure 1. Logic diagram



1. For 28-pin, 300 mil embedded crystal SOIC only.

Table 1. Signal names

$\overline{E}_{CON}$	Conditioned chip enable output
$\overline{EX}$	External chip enable
$\overline{IRQ}$/FT/OUT	Interrupt/frequency test/out output (open drain)
PFI	Power fail input
$\overline{PFO}$	Power fail output
$\overline{RST}$	Reset output (open drain)
$\overline{RSTIN1}$	Reset 1 Input
$\overline{RSTIN2}$	Reset 2 Input
SCL	Serial clock input
SDA	Serial data input/output
SQW	Square wave output
WDI	Watchdog input
V_{CC}	Supply voltage
V_{OUT}	Voltage output
V_{SS}	Ground
V_{BAT}(1)	Battery supply voltage
NC	No connect
NF	No function

1. For 28-pin, 300 mil embedded crystal SOIC only.

Figure 2. 28-pin SOIC connections

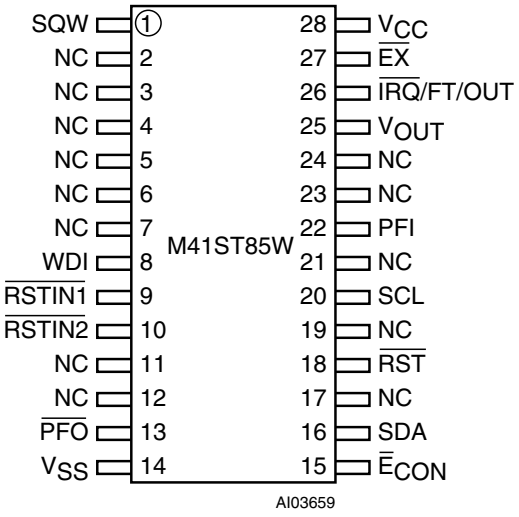
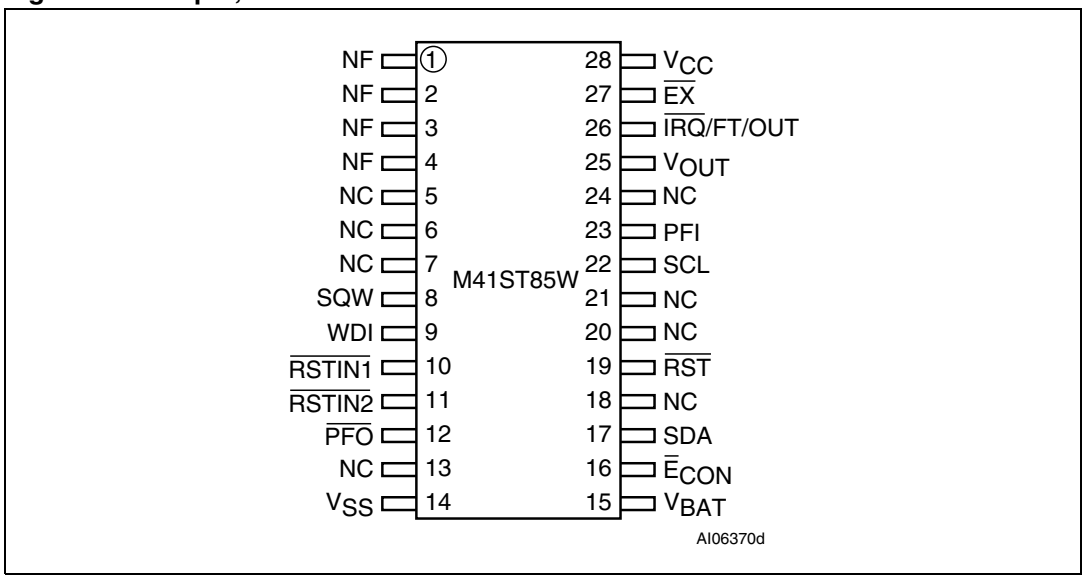
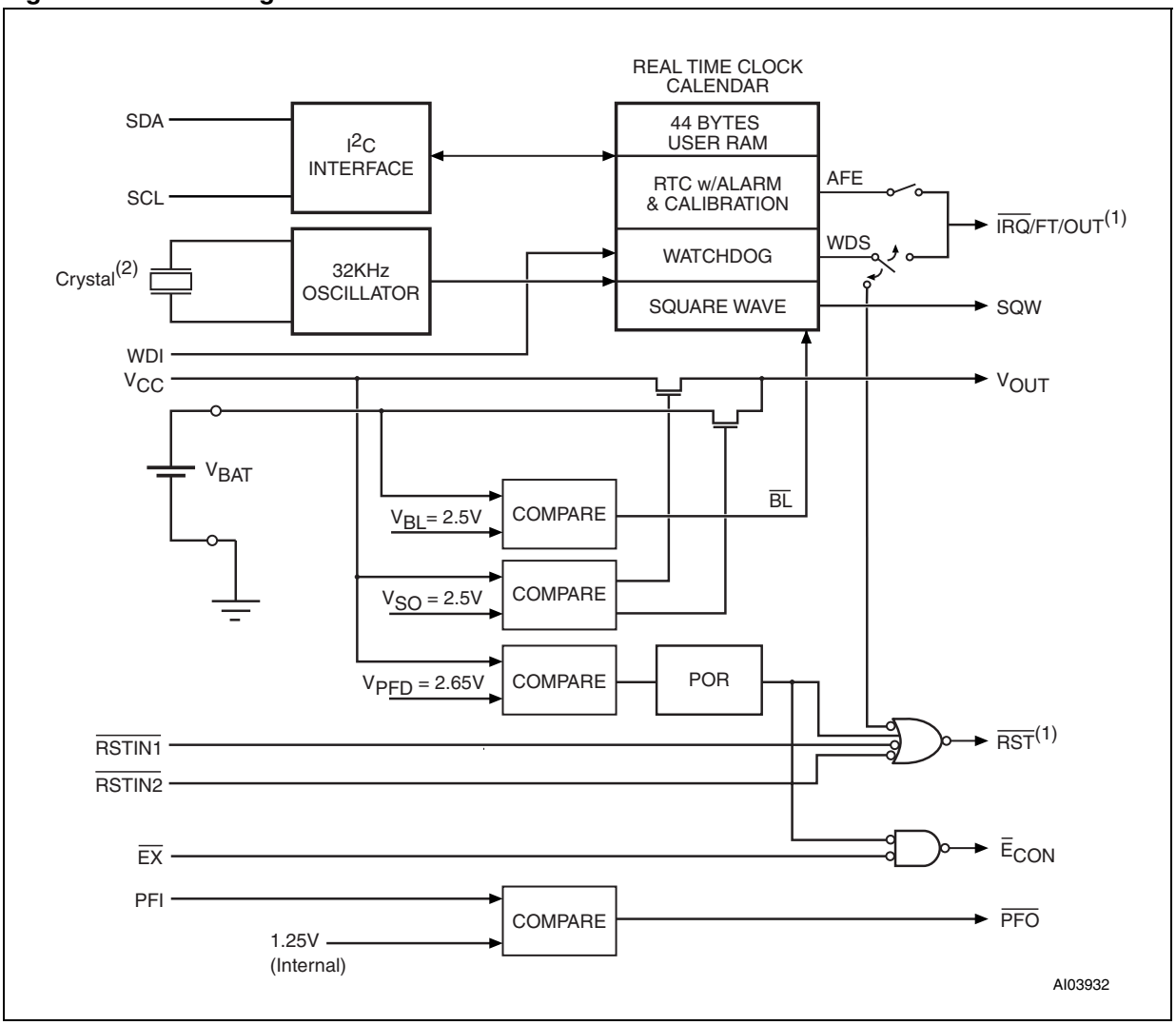


Figure 3. 28-pin, 300 mil SOIC connections



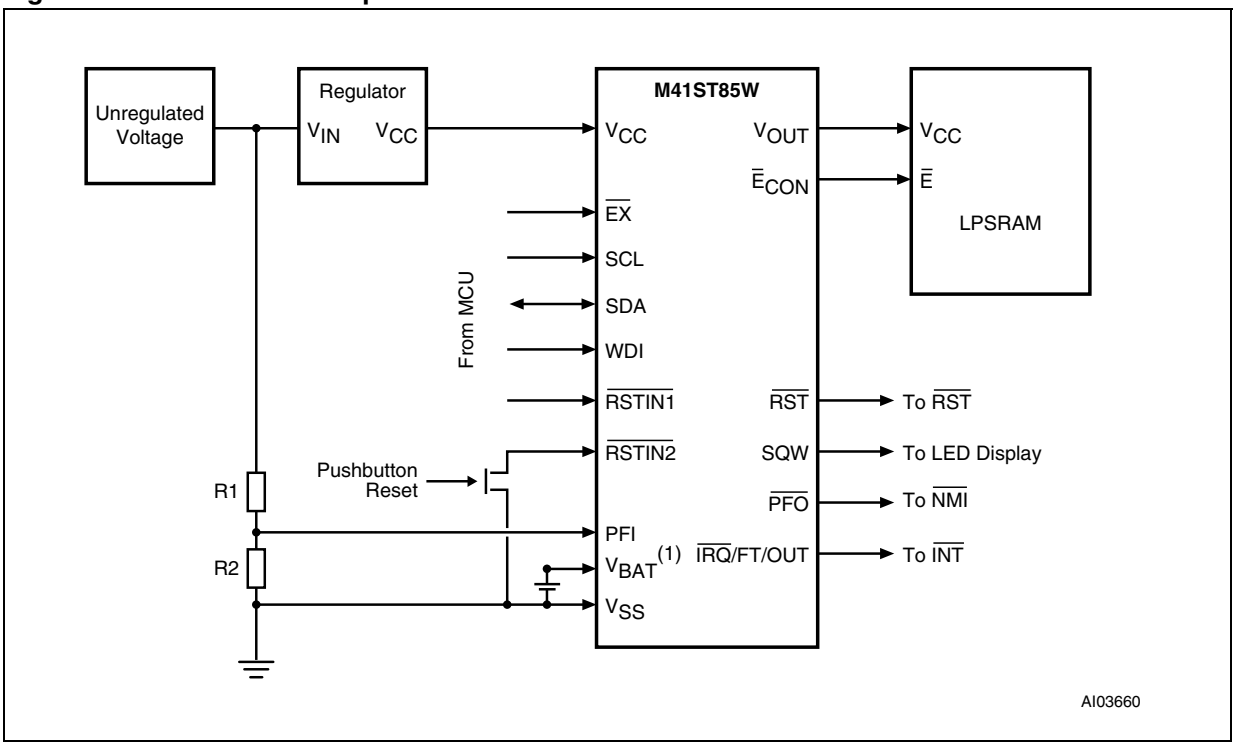
Note: No function (NF) pins should be tied to V_{SS}. Pins 1, 2, 3, and 4 are internally shorted together.

Figure 4. Block diagram



1. Open drain output.
2. Crystal integrated into SOIC package for MX package option.

Figure 5. Hardware hookup



1. Required for embedded crystal (MX) package only.

2 Operating modes

The M41ST85W clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/hundredths of a second register
2. Seconds register
3. Minutes register
4. Century/hours register
5. Day register
6. Date register
7. Month register
8. Year register
9. Control register
10. Watchdog register

11 - 16. Alarm registers

17 - 19. Reserved

20. Square wave register

21 - 64. User RAM

The M41ST85W clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultralow current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD}(min) plus t_{rec} (min).

For more information on battery storage life refer to application note AN1012.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 6. Serial bus data transfer sequence

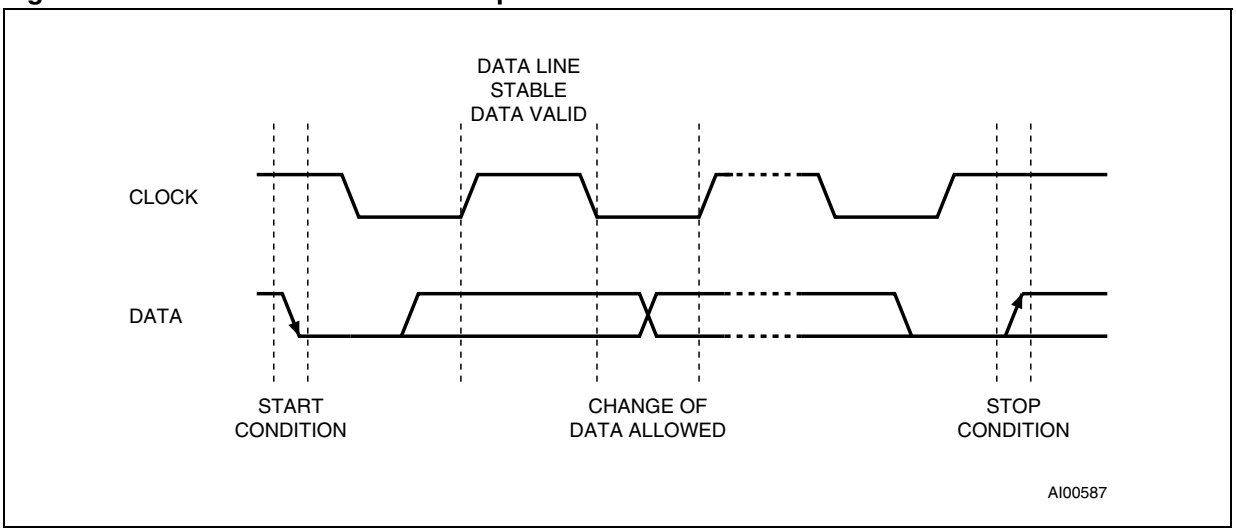


Figure 7. Acknowledgement sequence

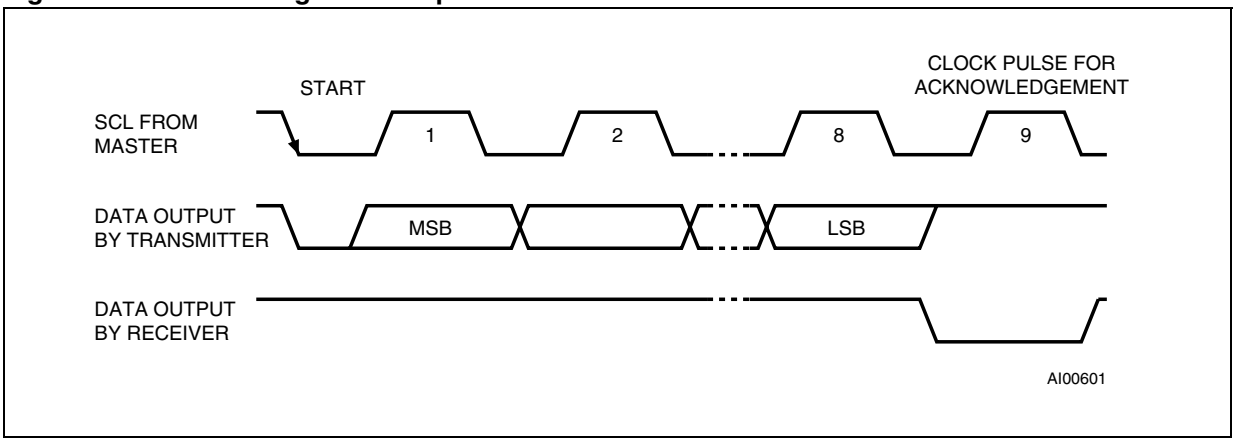
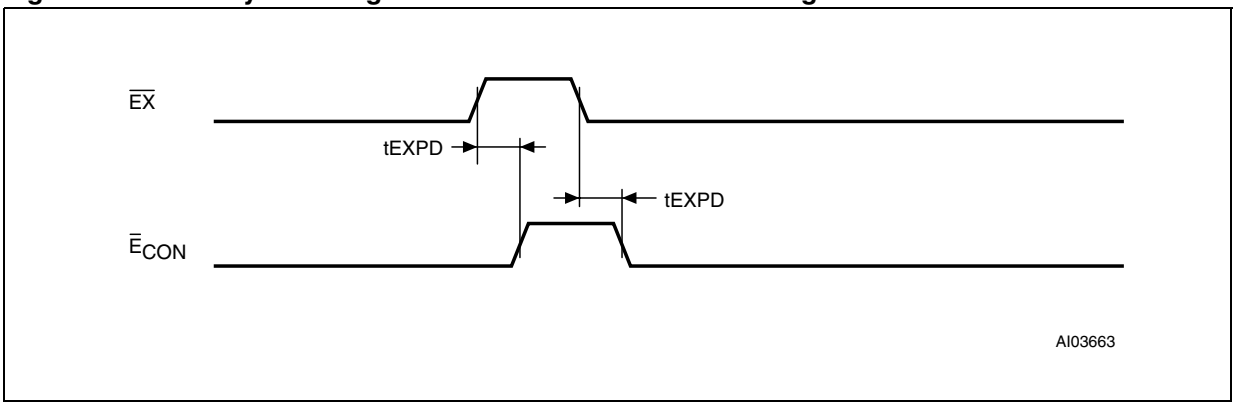


Figure 8. Write cycle timing: RTC & external SRAM control signals



2.2 Read mode

In this mode the master reads the M41ST85W slave after setting the slave address (see *Figure 9*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver.

The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter (see *Figure 10 on page 16*). The address pointer is only incremented on reception of an acknowledge clock. The M41ST85W slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41ST85W slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 11 on page 16*).

Figure 9. Slave address location

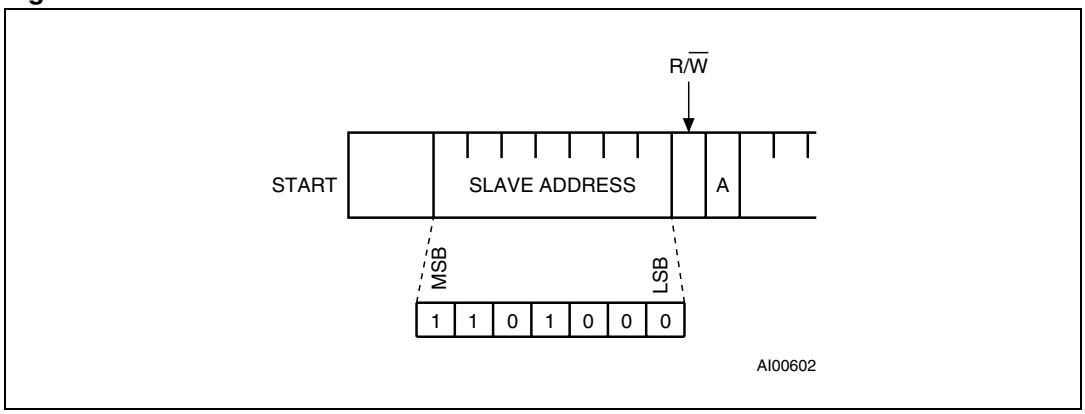


Figure 10. Read mode sequence

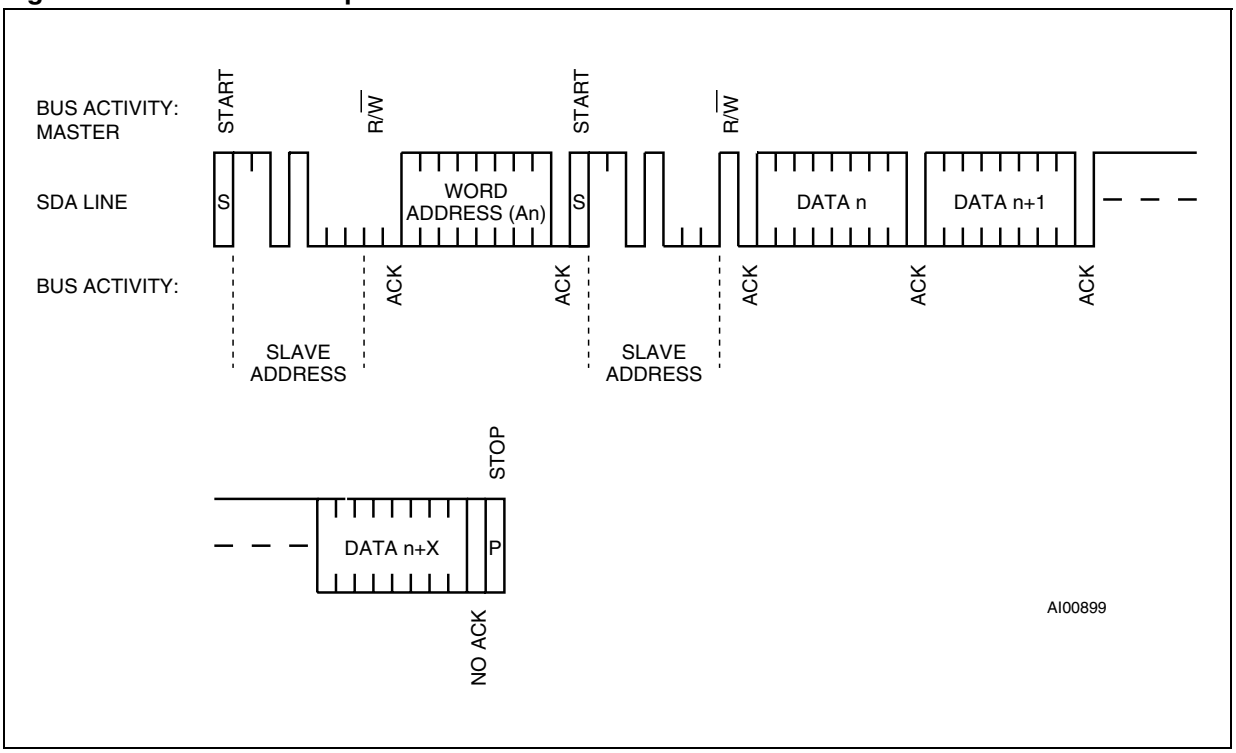
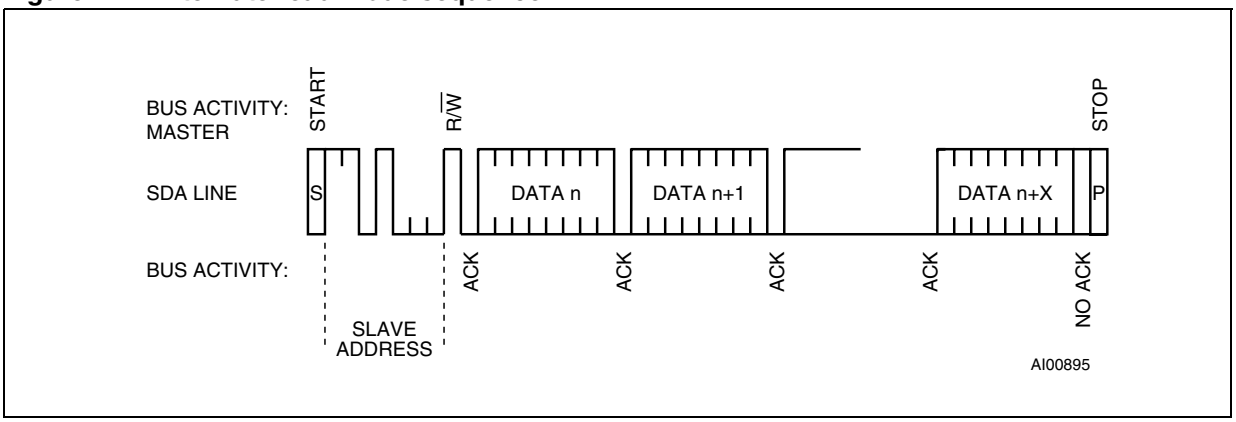


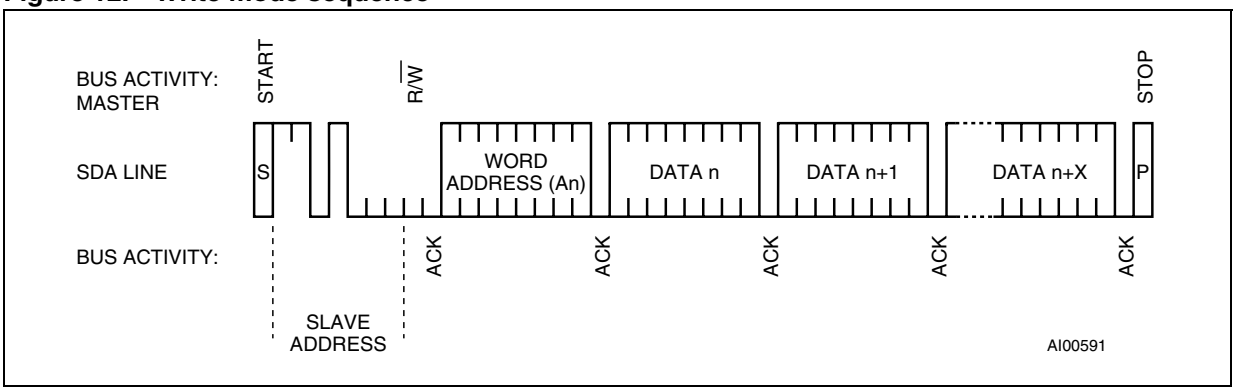
Figure 11. Alternate read mode sequence



2.3 Write mode

In this mode the master transmitter transmits to the M41ST85W slave receiver. Bus protocol is shown in *Figure 12*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41ST85W slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

Figure 12. Write mode sequence



2.4 Data retention mode

With valid V_{CC} applied, the M41ST85W can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41ST85W will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD}(max) and V_{PFD}(min). This is accomplished by internally inhibiting access to the clock registers. At this time, the reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{E}_{CON}$ to a high level. This level is within 0.2 volts of the V_{BAT}. $\overline{E}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition. When V_{CC} falls below the battery backup switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the SNAPHAT® battery, and the clock registers and external SRAM are maintained from the attached battery supply.

All outputs become high impedance. The V_{OUT} pin is capable of supplying 100 µA of current to the attached memory with less than 0.3 volts drop under this condition. On power-up, when V_{CC} returns to a nominal value, write protection continues for t_{rec} by inhibiting $\overline{E}_{CON}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 20 on page 33*).

Note: Most low power SRAMs on the market today can be used with the M41ST85W RTC SUPERVISOR. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41ST85W and SRAMs to be "Don't Care" once V_{CC} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC} = 2.0 volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M41ST85W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT® top of your choice can then be divided by this current to determine the amount of data retention available (see *Table 21 on page 40*).

For a further more detailed review of lifetime calculations, please see application note AN1012.

3 Clock operation

The eight byte clock register (see *Table 2 on page 20*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Note: A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to "00," and tenths/hundredths of seconds cannot be written to any value other than "00."

Bits D6 and D7 of clock register 03h (century/hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month and years. The ninth clock register is the control register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight clock registers may be read one byte at a time, or in a sequential block. The control register (address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Power-down time-stamp

When a power failure occurs, the halt update bit (HT) will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER® registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a '0' will allow the clock to update the TIMEKEEPER registers with the current time. For more information, see application note AN1572.

3.2 TIMEKEEPER® registers

The M41ST85W offers 20 internal registers which contain clock, alarm, watchdog, flag, square wave and control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

TIMEKEEPER and alarm registers store data in BCD. control, watchdog and square wave registers store data in binary format.

Table 2. TIMEKEEPER® register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 seconds				0.01 seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 hours		Hours (24-hour format)				Century/hours	0-1/00-23
04h	TR	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	HT	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	BL	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

Keys:
- S = Sign bit
- FT = Frequency test bit
- ST = Stop bit
- 0 = Must be set to zero
- BL = Battery low flag (read only)
- BMB0-BMB4 = Watchdog multiplier bits
- CEB = Century enable bit
- CB = Century bit
- OUT = Output level
- AFE = Alarm flag enable flag
- RB0-RB1 = Watchdog resolution bits
- WDS = Watchdog steering bit
- ABE = Alarm in battery backup mode enable bit
- RPT1-RPT5 = Alarm repeat mode bits
- WDF = Watchdog flag (read only)
- AF = Alarm flag (read only)
- SQWE = Square wave enable
- RS0-RS3 = SQW frequency
- HT = Halt update bit
- TR = t_{rec} bit

3.3 Calibrating the clock

The M41ST85W is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed +/–35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about +/–1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 13 on page 22*). Therefore, the M41ST85W design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 14 on page 22*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41ST85W may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT/OUT pin. The pin will toggle at 512 Hz, when the stop bit (ST, D7 of 01h) is '0,' the frequency test bit (FT, D6 of 08h) is '1,' the alarm flag enable bit (AFE, D7 of 0Ah) is '0,' and the watchdog steering bit (WDS, D7 of 09h) is '1' or the watchdog register (09h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{\text{IRQ}}$/FT/OUT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500 to 10 k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 13. Crystal accuracy across temperature

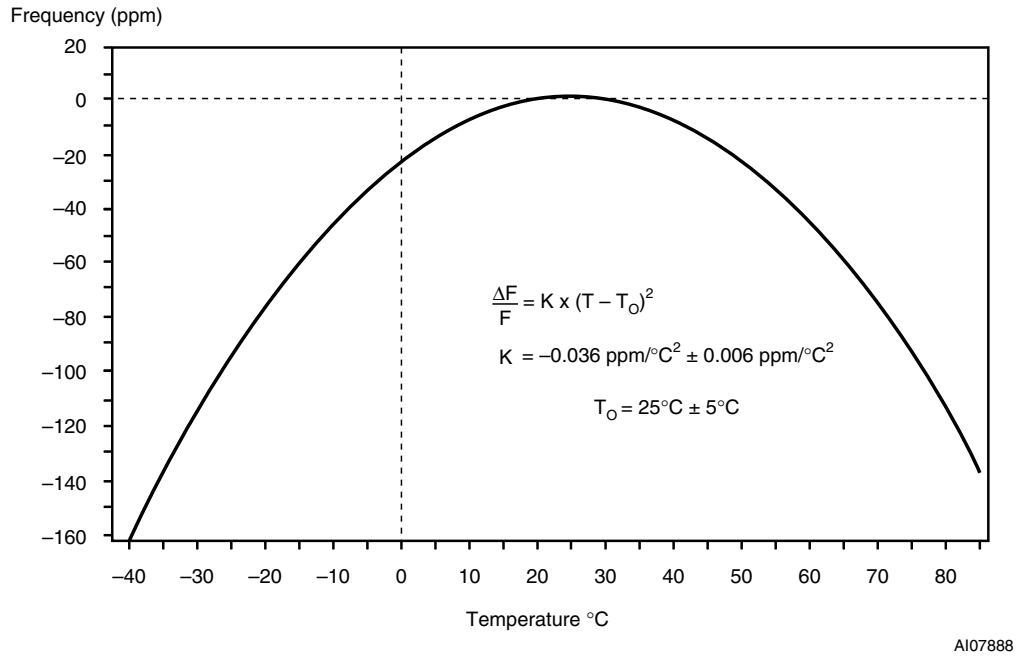
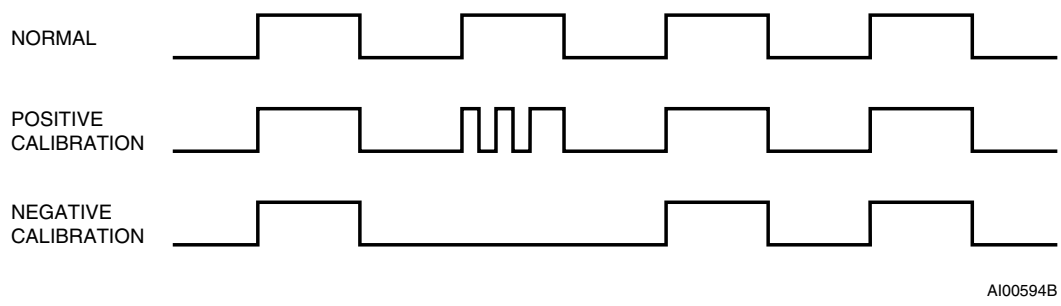


Figure 14. Calibration waveform



3.4 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41ST85W is in the battery backup to serve as a system wake-up call.

Bits RPT5–RPT1 put the alarm in the repeat mode of operation. *Table 3* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT/OUT pin as shown in *Figure 15*. To disable alarm, write '0' to the alarm date register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{IRQ}$/FT/OUT output is cleared by a READ to the flags register. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{IRQ}$/FT/OUT pin can also be activated in the battery backup mode. The $\overline{IRQ}$/FT/OUT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M41ST85W was in the deselect mode during power-up. *Figure 16 on page 24* illustrates the backup mode alarm timing.

Figure 15. Alarm interrupt reset waveform

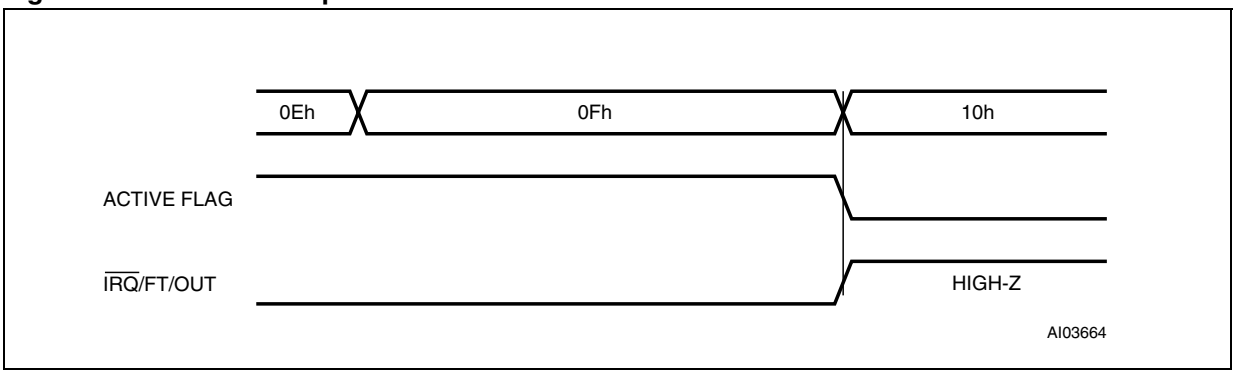
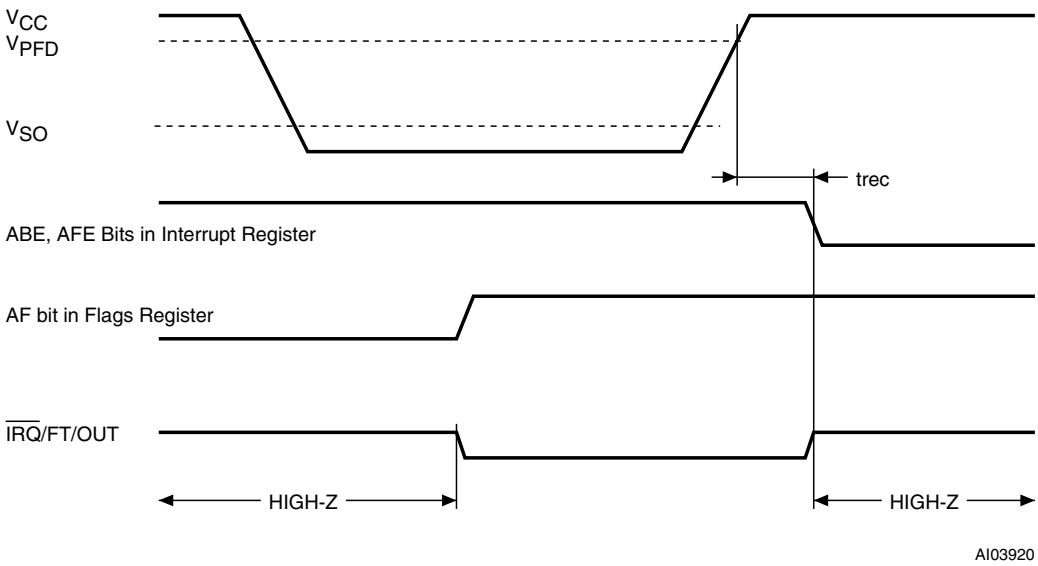


Table 3. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 16. Backup mode alarm waveform



3.5 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds).

Note: The accuracy of the timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M41ST85W sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0,' the watchdog will activate the $\overline{IRQ}$/FT/OUT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for t_{rec}. The watchdog register, FT, AFE, ABE and SQWE bits will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods: 1) a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI) or 2) the microprocessor can perform a WRITE of the watchdog register. The time-out period then starts over.

Note: The WDI pin should be tied to V_{SS} if not used.

In order to perform a software reset of the watchdog timer, the original time-out period can be written into the watchdog register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS bit is programmed to output an interrupt, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/FT/OUT

pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT/OUT pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied.

3.6 Square wave output

The M41ST85W offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 4*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Table 4. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.7 Power-on reset

The M41ST85W continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD}(max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.