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M41ST85Y
M41ST85W

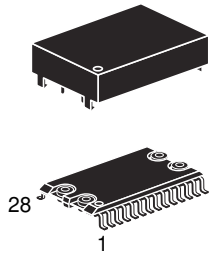
5.0 or 3.0V, 512 bit (64 x 8) Serial RTC and NVRAM Supervisor

FEATURES SUMMARY

- 5.0 OR 3.0V OPERATING VOLTAGE
- SERIAL INTERFACE SUPPORTS I^2C BUS (400 KHz)
- NVRAM SUPERVISOR FOR EXTERNAL LPSRAM
- OPTIMIZED FOR MINIMAL INTERCONNECT TO MCU
- 2.5 TO 5.5V OSCILLATOR OPERATING VOLTAGE
- AUTOMATIC SWITCH-OVER AND DESELECT CIRCUITRY
- CHOICE OF POWER-FAIL DESELECT VOLTAGES
  - M41ST85Y: V_{CC} = 4.5 to 5.5V; $4.20V \le V_{PFD} \le 4.50V$
  - M41ST85W: V_{CC} = 2.7 to 3.6V; $2.55V \le V_{PFD} \le 2.70V$
- 1.25V REFERENCE (for PFI/$\overline{PFO}$)
- COUNTERS FOR TENTHS/HUNDREDTHS OF SECONDS, SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEAR, AND CENTURY
- 44 BYTES OF GENERAL PURPOSE RAM
- PROGRAMMABLE ALARM AND INTERRUPT FUNCTION (VALID EVEN DURING BATTERY BACK-UP MODE)
- WATCHDOG TIMER
- MICROPROCESSOR POWER-ON RESET
- BATTERY LOW FLAG
- POWER-DOWN TIMESTAMP (HT BIT)
- ULTRA-LOW BATTERY SUPPLY CURRENT OF 500nA (MAX)
- PACKAGING INCLUDES A 28-LEAD SOIC AND SNAPHAT® TOP (to be ordered separately)
- SOIC SNAPHAT PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY AND CRYSTAL
- SOIC EMBEDDED CRYSTAL PACKAGE (MX) OPTION

Figure 1. 28-pin SOIC Package

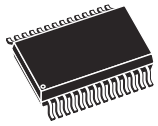
SNAPHAT (SH)
Battery & Crystal



SOH28 (MH)

Figure 2. 28-pin (300mil) SOIC Package

EMBEDDED Crystal



SOX28 (MX)

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SUMMARY DESCRIPTION

The M41ST85Y/W Serial TIMEKEEPER®/Controller SRAM is a low power 512-bit, static CMOS SRAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (external crystal controlled) and 8 bytes of the SRAM (see Table 2., page 14) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format.

An additional 12 bytes of RAM provide status/control of Alarm, Watchdog and Square Wave functions. Addresses and data are transferred serially via a two line, bi-directional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41ST85Y/W has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs.

Functions available to the user include a non-volatile, time-of-day clock/calendar, Alarm interrupts, Watchdog Timer and programmable Square Wave output. Other features include a Power-On Reset as well as two additional debounced inputs ($\overline{RSTIN1}$ and $\overline{RSTIN2}$) which can also generate an output Reset ($\overline{RST}$). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The M41ST85Y/W is supplied in a 28-lead SOIC SNAPHAT® package (which integrates both crystal and battery in a single SNAPHAT top) or a 28-pin, 300mil SOIC package (MX) which includes an embedded 32kHz crystal.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

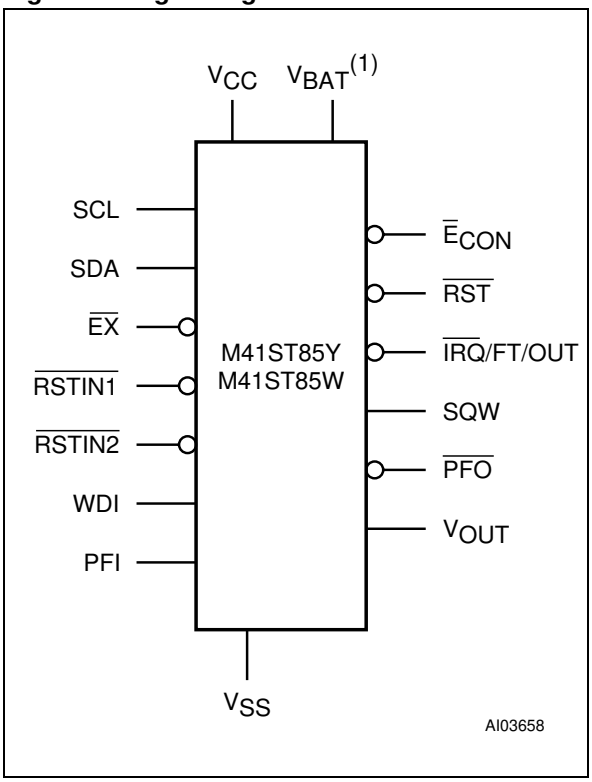
Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4TXX-BR12SH” (see Table 19., page 32).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

The 300mil, embedded crystal SOIC requires only a user-supplied battery to provide non-volatile operation.

Figure 3. Logic Diagram



Note: 1. For 28-pin, 300mil embedded crystal SOIC only.

Table 1. Signal Names

$\overline{E}_{CON}$	Conditioned Chip Enable Output
$\overline{EX}$	External Chip Enable
$\overline{IRQ}$/FT/OUT	Interrupt/Frequency Test/Out Output (Open Drain)
PFI	Power Fail Input
$\overline{PFO}$	Power Fail Output
$\overline{RST}$	Reset Output (Open Drain)
$\overline{RSTIN1}$	Reset 1 Input
$\overline{RSTIN2}$	Reset 2 Input
SCL	Serial Clock Input
SDA	Serial Data Input/Output
SQW	Square Wave Output
WDI	Watchdog Input
V_{CC}	Supply Voltage
V_{OUT}	Voltage Output
V_{SS}	Ground
V_{BAT}(1)	Battery Supply Voltage
NC	No Connect
NF	No Function

Note: 1. For 28-pin, 300mil embedded crystal SOIC only.

Figure 4. 28-pin SOIC Connections

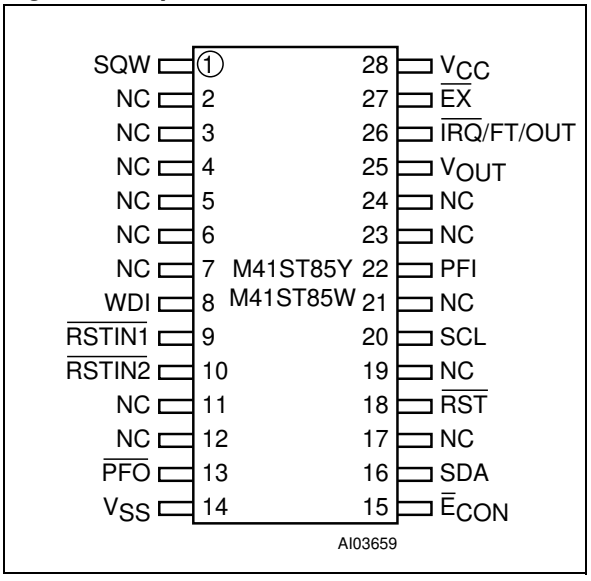
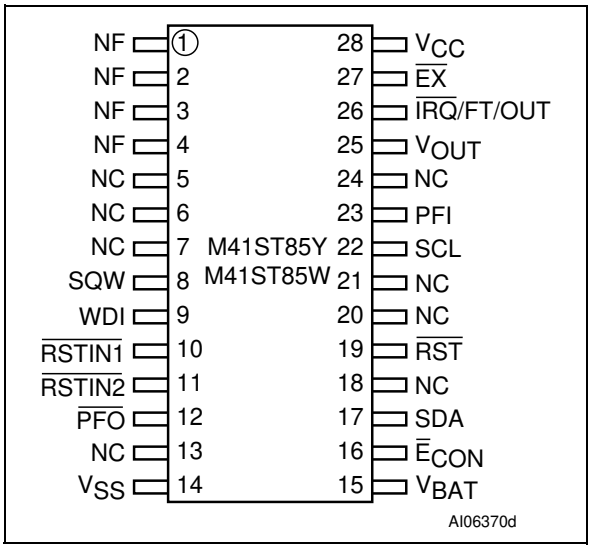
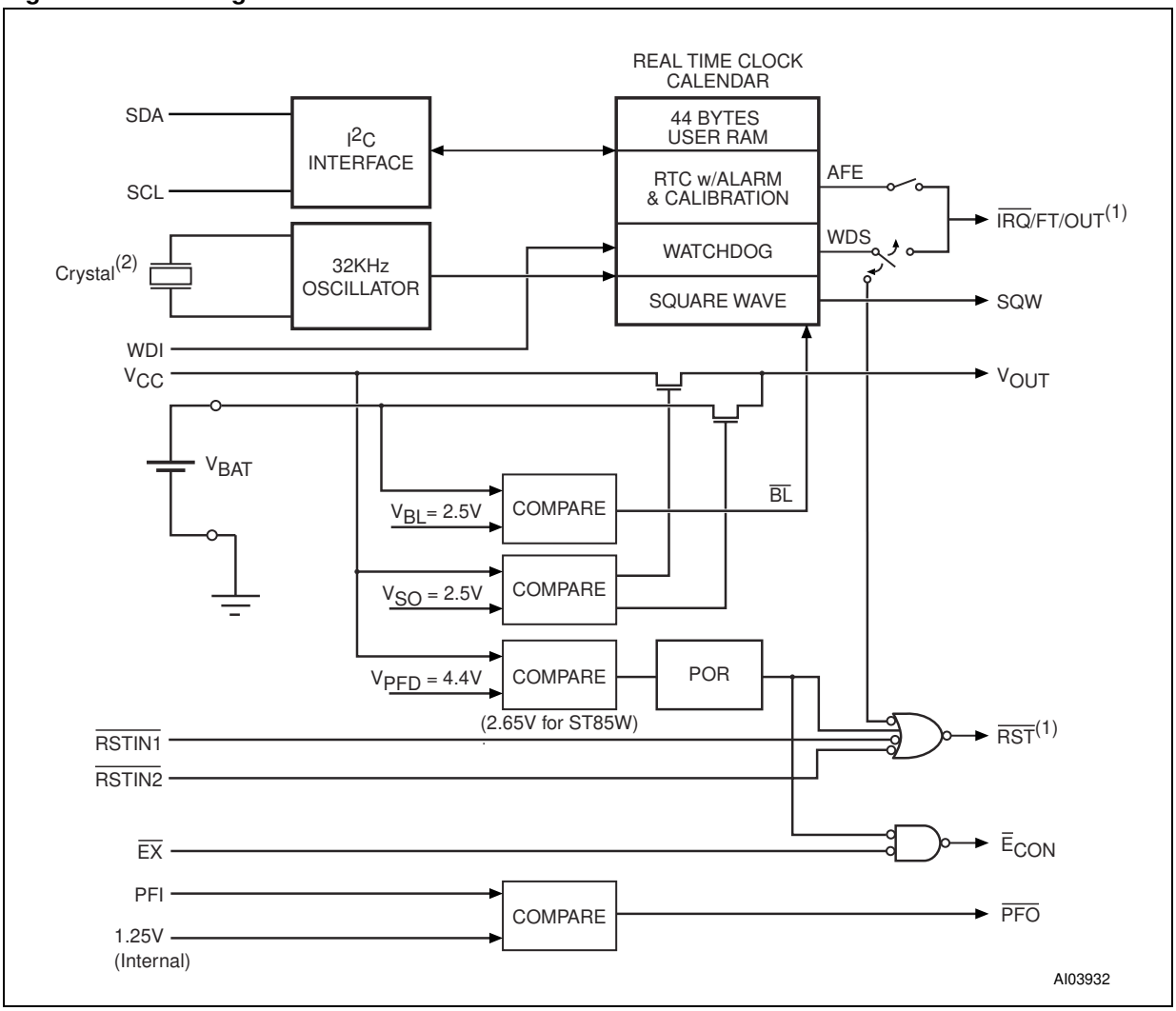


Figure 5. 28-pin, 300mil SOIC (MX) Connections



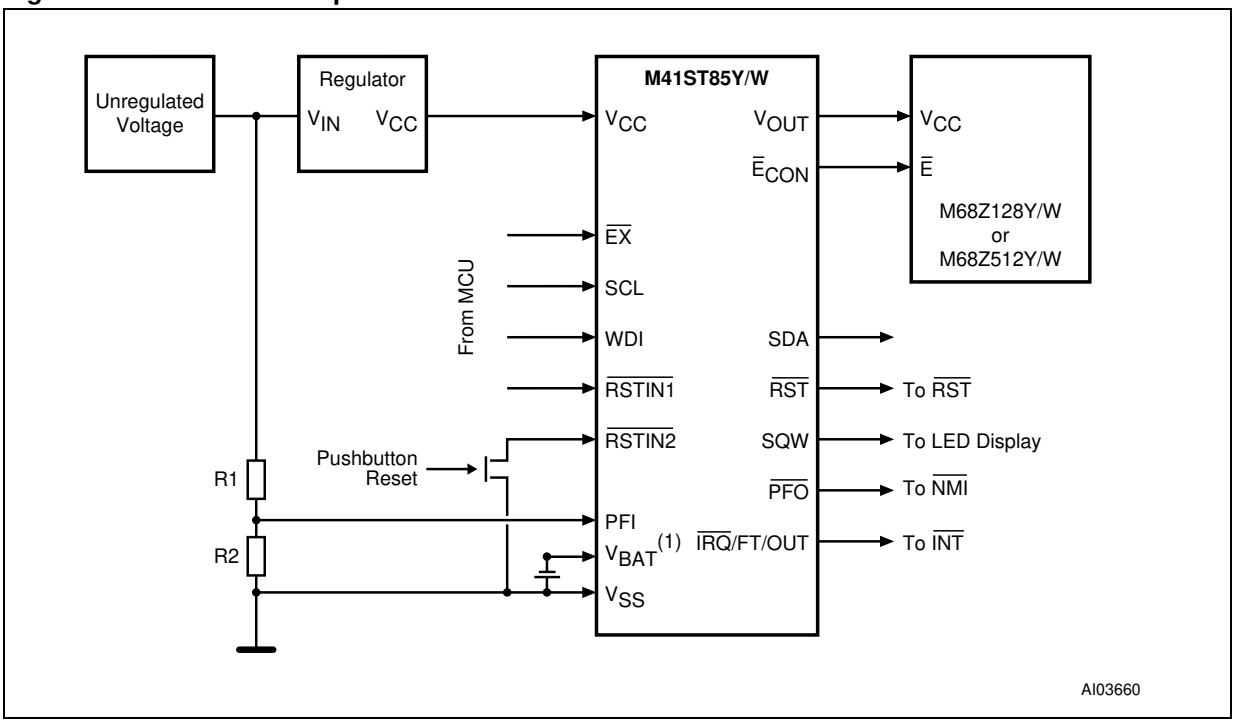
Note: No Function (NF) pins should be tied to V_{SS}. Pins 1, 2, 3, and 4 are internally shorted together.

Figure 6. Block Diagram



Note: 1. Open drain output
2. Integrated into SOIC package for MX package option.

Figure 7. Hardware Hookup



Note: 1. Required for embedded crystal (MX) package only.

OPERATING MODES

The M41ST85Y/W clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/Hundredths of a Second Register
2. Seconds Register
3. Minutes Register
4. Century/Hours Register
5. Day Register
6. Date Register
7. Month Register
8. Year Register
9. Control Register
10. Watchdog Register

11 - 16. Alarm Registers

17 - 19. Reserved

20. Square Wave Register

21 - 64. User RAM

The M41ST85Y/W clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD}(min) plus t_{rec} (min).

For more information on Battery Storage Life refer to Application Note AN1012.

2-Wire Bus Characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.

– During data transfer, the data line must remain stable whenever the clock line is High.

– Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data Valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

Acknowledge. Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 8. Serial Bus Data Transfer Sequence

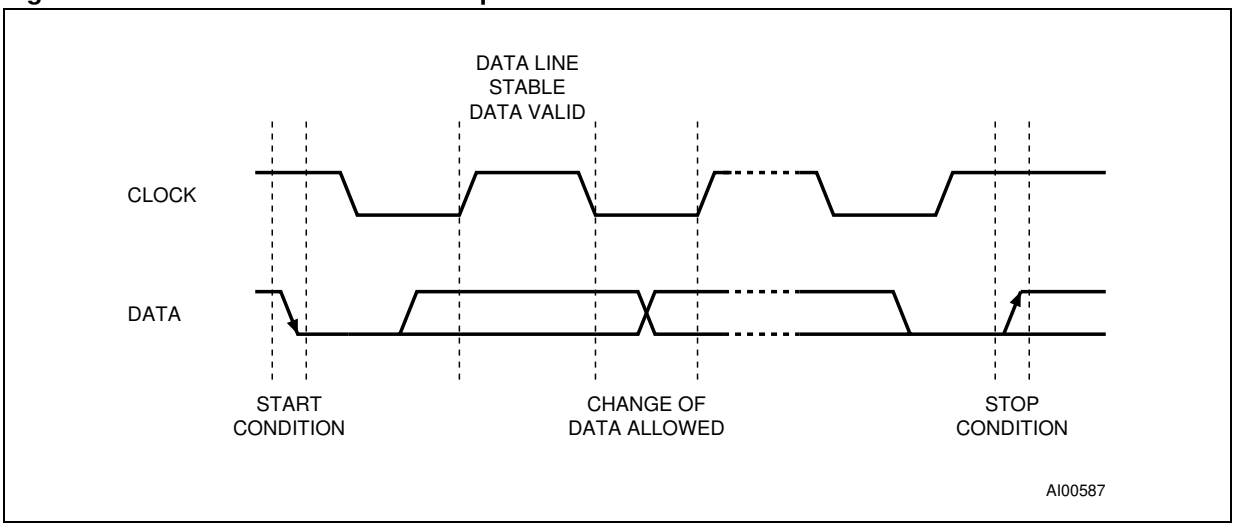


Figure 9. Acknowledgement Sequence

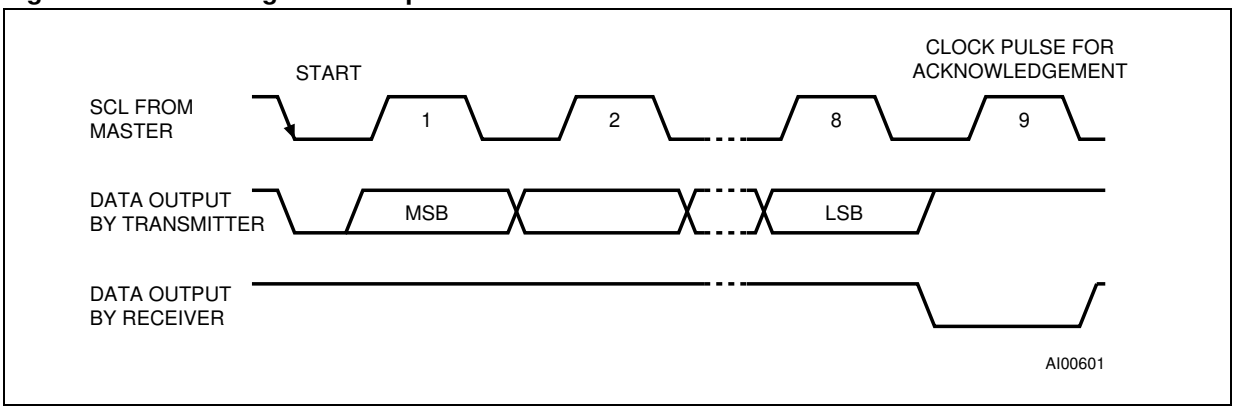
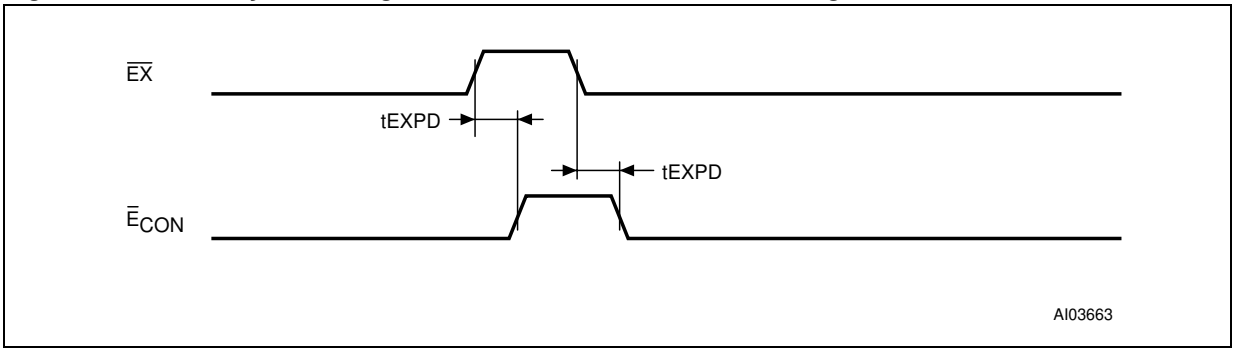


Figure 10. WRITE Cycle Timing: RTC & External SRAM Control Signals



READ Mode

In this mode the master reads the M41ST85Y/W slave after setting the slave address (see Figure 11., page 10). Following the WRITE Mode Control Bit (R/$\overline{W}$=0) and the Acknowledge Bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ Mode Control Bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver.

The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge Bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge Clock. The M41ST85Y/W slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter (see Figure 12., page 10).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a non-clock or RAM address.

Note: This is true both in READ Mode and WRITE Mode.

An alternate READ Mode may also be implemented whereby the master reads the M41ST85Y/W slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 13., page 11).

Figure 11. Slave Address Location

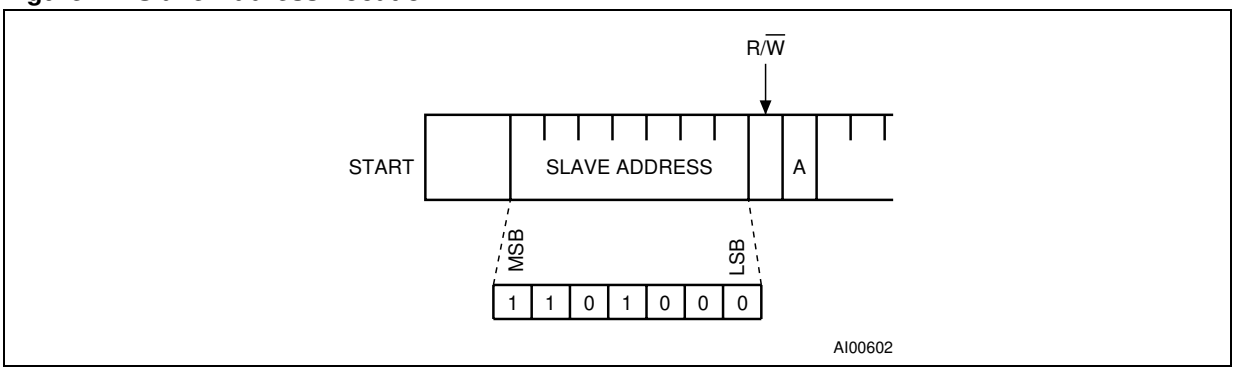


Figure 12. READ Mode Sequence

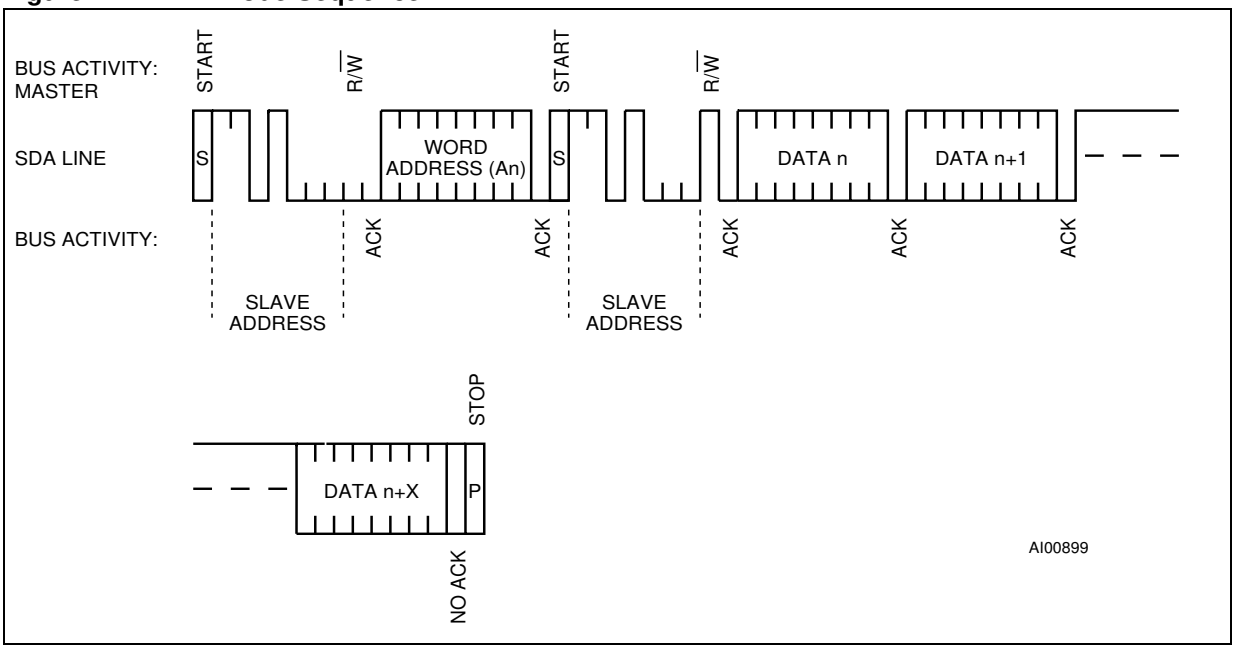
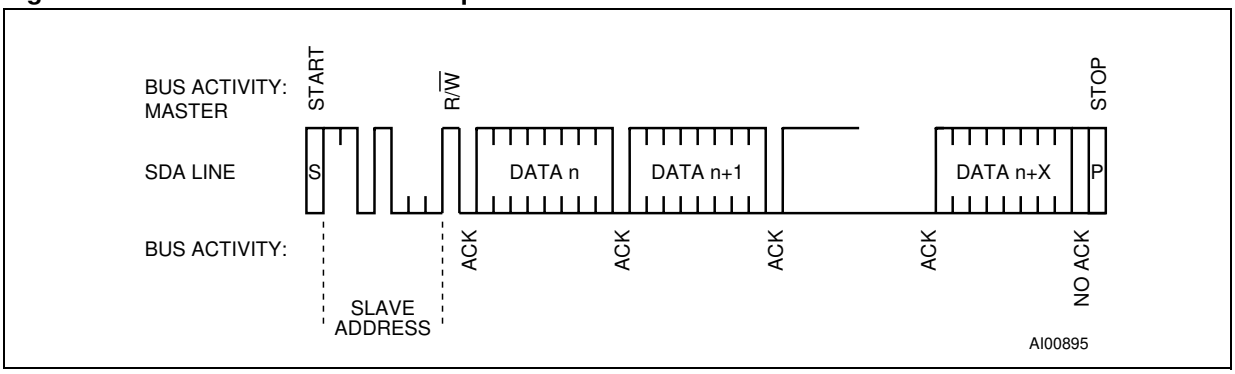


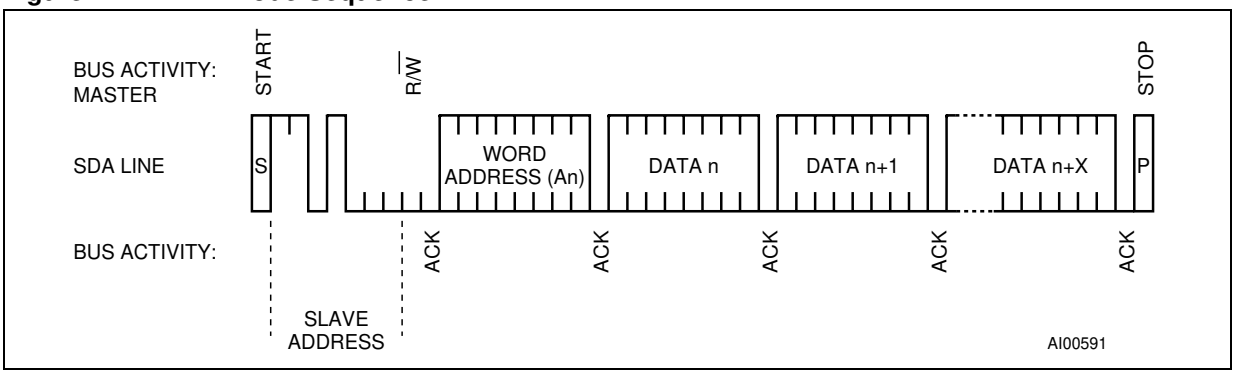
Figure 13. Alternate READ Mode Sequence



WRITE Mode

In this mode the master transmitter transmits to the M41ST85Y/W slave receiver. Bus protocol is shown in Figure 14., page 11. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41ST85Y/W slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see Figure 11., page 10) and again after it has received the word address and each data byte.

Figure 14. WRITE Mode Sequence



Data Retention Mode

With valid V_{CC} applied, the M41ST85Y/W can be accessed as described above with READ or WRITE Cycles. Should the supply voltage decay, the M41ST85Y/W will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD}(max) and V_{PFD}(min). This is accomplished by internally inhibiting access to the clock registers. At this time, the Reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{E}_{CON}$ to a high level. This level is within 0.2 volts of the V_{BAT}. $\overline{E}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition. When V_{CC} falls below the Battery Back-up Switchover Voltage (V_{SO}), power input is switched from the V_{CC} pin to the SNAPHAT® battery, and the clock registers and external SRAM are maintained from the attached battery supply.

All outputs become high impedance. The V_{OUT} pin is capable of supplying 100 µA of current to the attached memory with less than 0.3 volts drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{rec} by inhibiting $\overline{E}_{CON}$. The $\overline{RST}$ signal also remains active during this time (see Figure 22., page 27).

Note: Most low power SRAMs on the market today can be used with the M41ST85Y/W RTC SUPERVISOR. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41ST85Y/W and SRAMs to be “Don’t Care” once V_{CC} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC}=2.0 volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M41ST85Y/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the amount of data retention available (see Table 19., page 32).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

CLOCK OPERATION

The eight byte clock register (see Table 2., page 14) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/Hundredths of Seconds, Seconds, Minutes, and Hours are contained within the first four registers.

Note: A WRITE to any clock register will result in the Tenths/Hundredths of Seconds being reset to "00," and Tenths/Hundredths of Seconds cannot be written to any value other than "00."

Bits D6 and D7 of Clock Register 03h (Century/ Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of Register 04h contain the Day (day of week). Registers 05h, 06h, and 07h contain the Date (day of month), Month and Years. The ninth clock register is the Control Register (this is described in the Clock Calibration section). Bit D7 of Register 01h contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight Clock Registers may be read one byte at a time, or in a sequential block. The Control Register (Address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

Power-down Time-Stamp

When a power failure occurs, the Halt Update Bit (HT) will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER® registers, and will allow the user to read the exact time of the power-down event. Resetting the HT Bit to a '0' will allow the clock to update the TIMEKEEPER registers with the current time. For more information, see Application Note AN1572.

TIMEKEEPER® Registers

The M41ST85Y/W offers 20 internal registers which contain Clock, Alarm, Watchdog, Flag, Square Wave and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a non-clock or RAM address.

TIMEKEEPER and Alarm Registers store data in BCD. Control, Watchdog and Square Wave Registers store data in Binary Format.

Table 2. TIMEKEEPER® Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 Seconds				0.01 Seconds				Seconds	00-99
01h	ST	10 Seconds			Seconds				Seconds	00-59
02h	0	10 Minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 Hours		Hours (24 Hour Format)				Century/Hours	0-1/00-23
04h	TR	0	0	0	0	Day of Week			Day	01-7
05h	0	0	10 Date		Date: Day of Month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	Al 10M	Alarm Month				Al Month	01-12
0Bh	RPT4	RPT5	Al 10 Date		Alarm Date				Al Date	01-31
0Ch	RPT3	HT	Al 10 Hour		Alarm Hour				Al Hour	00-23
0Dh	RPT2	Alarm 10 Minutes			Alarm Minutes				Al Min	00-59
0Eh	RPT1	Alarm 10 Seconds			Alarm Seconds				Al Sec	00-59
0Fh	WDF	AF	0	BL	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

Keys: S = Sign Bit
FT = Frequency Test Bit
ST = Stop Bit
0 = Must be set to zero
BL = Battery Low Flag (Read only)
BMB0-BMB4 = Watchdog Multiplier Bits
CEB = Century Enable Bit
CB = Century Bit
OUT = Output level
AFE = Alarm Flag Enable Flag
RB0-RB1 = Watchdog Resolution Bits
WDS = Watchdog Steering Bit
ABE = Alarm in Battery Back-Up Mode Enable Bit
RPT1-RPT5 = Alarm Repeat Mode Bits
WDF = Watchdog flag (Read only)
AF = Alarm flag (Read only)
SQWE = Square Wave Enable
RS0-RS3 = SQW Frequency
HT = Halt Update Bit
TR = t_{rec} Bit

Calibrating the Clock

The M41ST85Y/W is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed +/–35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about +/–1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see Figure 15., page 16). Therefore, the M41ST85Y/W design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 16., page 16. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration Bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Bits occupy the five lower order bits (D4-D0) in the Control Register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41ST85Y/W may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note AN934, “TIMEKEEPER® CALIBRATION.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT/OUT pin. The pin will toggle at 512Hz, when the Stop Bit (ST, D7 of 01h) is '0,' the Frequency Test Bit (FT, D6 of 08h) is '1,' the Alarm Flag Enable Bit (AFE, D7 of 0Ah) is '0,' and the Watchdog Steering Bit (WDS, D7 of 09h) is '1' or the Watchdog Register (09h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{IRQ}$/FT/OUT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500 to10k resistor is recommended in order to control the rise time. The FT Bit is cleared on power-down.

Figure 15. Crystal Accuracy Across Temperature

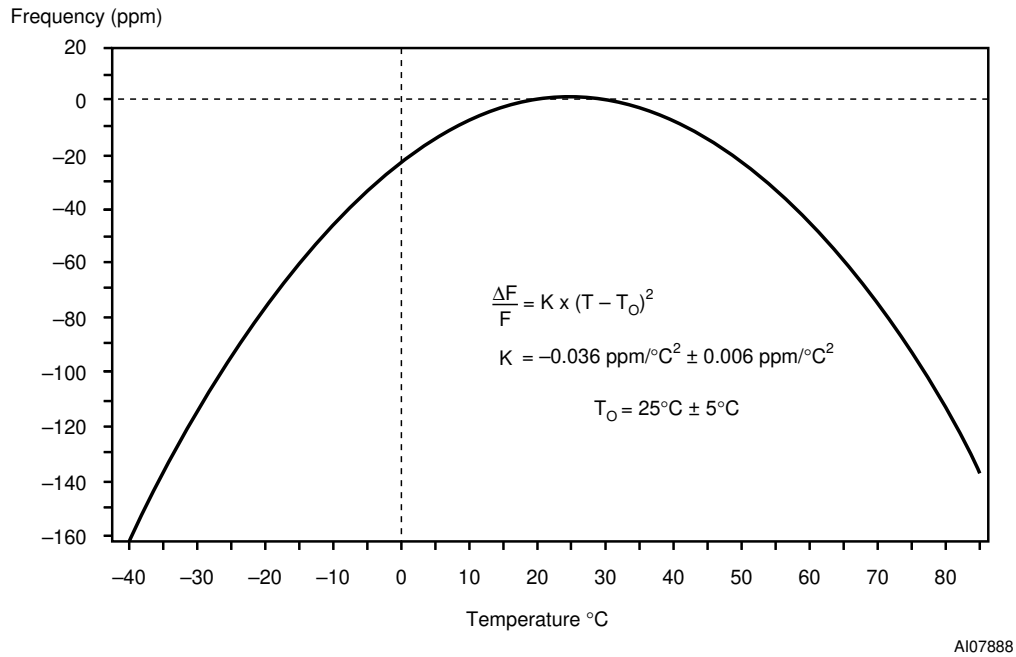
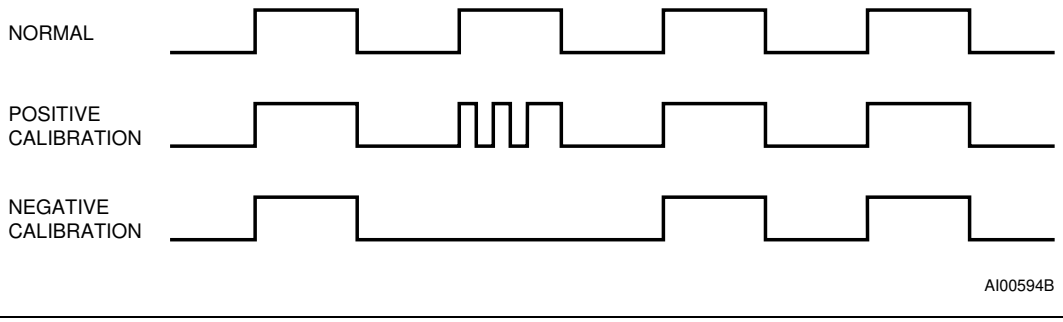


Figure 16. Calibration Waveform



Setting Alarm Clock Registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41ST85Y/W is in the battery back-up to serve as a system wake-up call.

Bits RPT5–RPT1 put the alarm in the repeat mode of operation. Table 3., page 17 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT/OUT pin as shown in Figure 17., page 17. To disable alarm, write '0' to the Alarm Date Register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the Flag Register address, an alarm condition will not cause the Interrupt/Flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the “Alarm Seconds,” the address pointer will increment to the Flag address, causing this situation to occur.

The $\overline{IRQ}$/FT/OUT output is cleared by a READ to the Flags Register. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

The $\overline{IRQ}$/FT/OUT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT/OUT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE Bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M41ST85Y/W was in the deselect mode during power-up. Figure 18., page 18 illustrates the back-up mode alarm timing.

Figure 17. Alarm Interrupt Reset Waveform

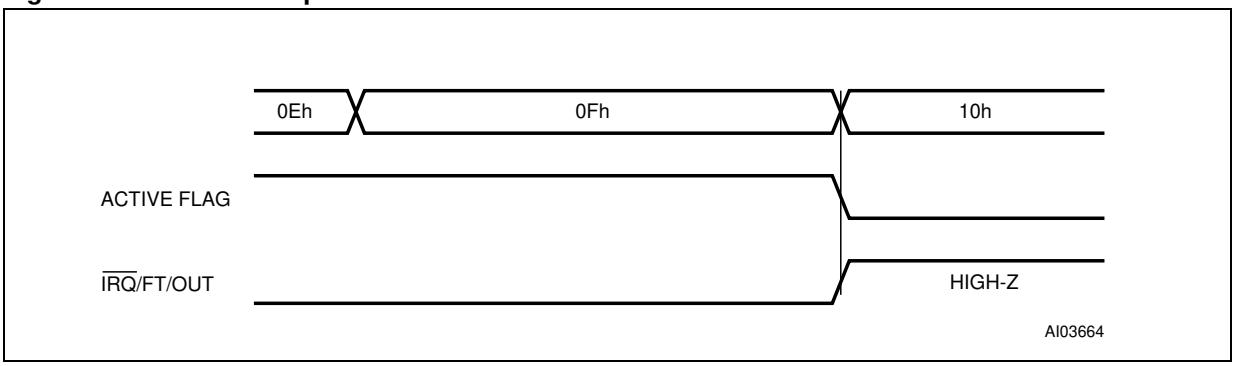
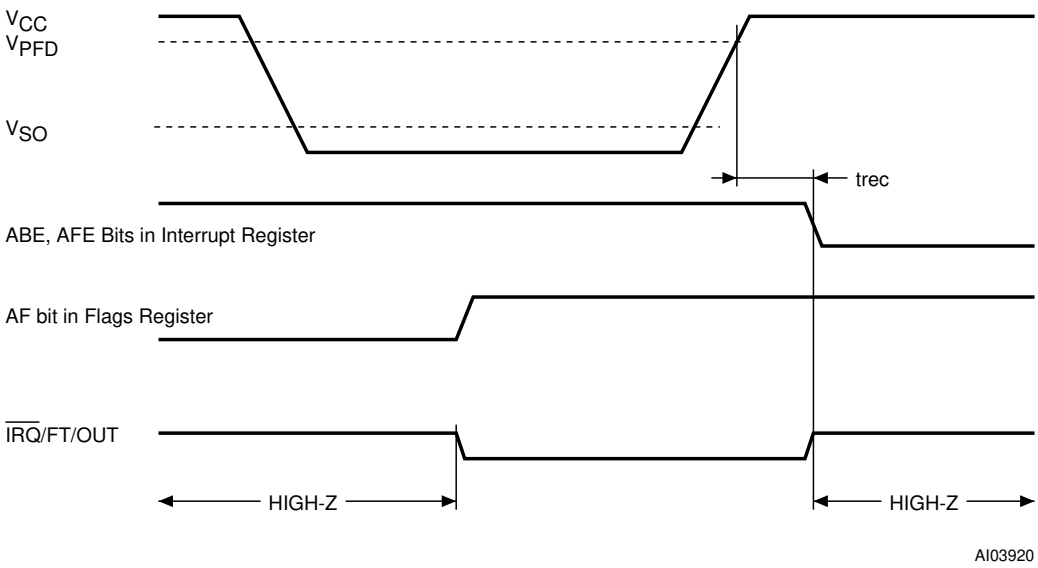


Table 3. Alarm Repeat Modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm Setting
1	1	1	1	1	Once per Second
1	1	1	1	0	Once per Minute
1	1	1	0	0	Once per Hour
1	1	0	0	0	Once per Day
1	0	0	0	0	Once per Month
0	0	0	0	0	Once per Year

Figure 18. Back-Up Mode Alarm Waveform



Watchdog Timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3*1 or 3 seconds).

Note: The accuracy of the timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M41ST85Y/W sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the Watchdog Register is the Watchdog Steering Bit (WDS). When set to a '0,' the watchdog will activate the $\overline{IRQ}$/FT/OUT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for t_{rec}. The Watchdog register, FT, AFE, ABE and SQWE Bits will reset to a '0' at the end of a Watchdog time-out when the WDS Bit is set to a '1.'

The watchdog timer can be reset by two methods: 1) a transition (high-to-low or low-to-high) can be applied to the Watchdog Input pin (WDI) or 2) the microprocessor can perform a WRITE of the Watchdog Register. The time-out period then starts over.

Note: The WDI pin should be tied to V_{SS} if not used.

In order to perform a software reset of the watchdog timer, the original time-out period can be written into the Watchdog Register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS Bit is programmed to output an interrupt, a value of 00h needs to be written to the Watchdog Register in order to clear the $\overline{IRQ}$/FT/OUT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (Bit D7; Register 0Fh).

The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT/OUT pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied.

Square Wave Output

The M41ST85Y/W offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in Table 4. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the Square Wave Enable Bit (SQWE) located in Register 0Ah.

Table 4. Square Wave Output Frequency

Square Wave Bits				Square Wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

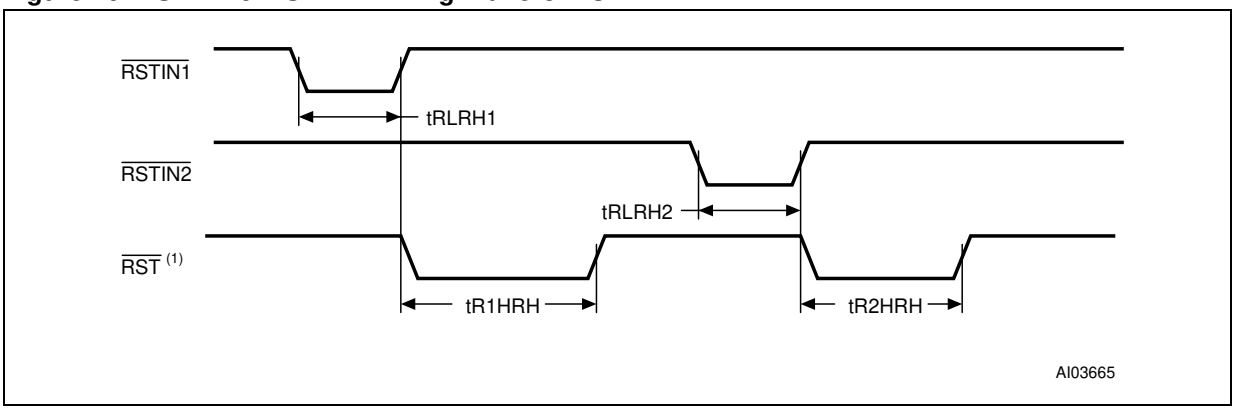
Power-on Reset

The M41ST85Y/W continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD}(max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

Reset Inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M41ST85Y/W provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. Table 5 and Figure 19 illustrate the AC reset characteristics of this function. Pulses shorter than t_{RLRH1} and t_{RLRH2} will not generate a reset condition. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to V_{CC} through a 100kΩ resistor.

Figure 19. $\overline{RSTIN1}$ & $\overline{RSTIN2}$ Timing Waveforms



Note: With pull-up resistor

Table 5. Reset AC Characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{RLRH1}(2)	$\overline{RSTIN1}$ Low to $\overline{RSTIN1}$ High	200		ns
t_{RLRH2}(3)	$\overline{RSTIN2}$ Low to $\overline{RSTIN2}$ High	100		ms
t_{R1HRH}(4)	$\overline{RSTIN1}$ High to $\overline{RST}$ High	40	200	ms
t_{R2HRH}(4)	$\overline{RSTIN2}$ High to $\overline{RST}$ High	40	200	ms

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. Pulse width less than 50ns will result in no RESET (for noise immunity).
3. Pulse width less than 20ms will result in no RESET (for noise immunity).
4. Programmable (see Table 6., page 22).

Power-fail INPUT/OUTPUT

The Power-Fail Input (PFI) is compared to an internal reference voltage (1.25V). If PFI is less than the power-fail threshold (V_{PFI}), the Power-Fail Output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 7., page 7) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the M41ST85Y/W or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator turns off and $\overline{PFO}$ goes (or remains) low. This occurs after V_{CC} drops below V_{PFD}(min). When power returns, $\overline{PFO}$ is forced high, irrespective of V_{PFI} for the write protect time (t_{rec}), which is the time from V_{PFD}(max) until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected.

Century Bit

Bits D7 and D6 of Clock Register 03h contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Output Driver Pin

When the FT Bit, AFE Bit and watchdog register are not set, the $\overline{IRQ}$/FT/OUT pin becomes an output driver that reflects the contents of D7 of the Control Register. In other words, when D7 (OUT Bit) and D6 (FT Bit) of address location 08h are a '0,' then the $\overline{IRQ}$/FT/OUT pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT pin is an open drain which requires an external pull-up resistor.

Battery Low Warning

The M41ST85Y/W automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The Battery Low (BL) Bit, Bit D4 of Flags Register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL Bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced. The SNAPHAT top may be replaced while V_{CC} is applied to the device.

Note: This will cause the clock to lose time during the interval the SNAPHAT battery/crystal top is disconnected.

The M41ST85Y/W only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

t_{rec} Bit

Bit D7 of Clock Register 04h contains the t_{rec} Bit (TR). t_{rec} refers to the automatic continuation of the deselect time after V_{CC} reaches V_{PFD}. This allows for a voltage settling time before WRITEs may again be performed to the device after a power-down condition. The t_{rec} Bit will allow the user to set the length of this deselect time as defined by Table 6., page 22.

Initial Power-on Defaults

Upon initial application of power to the device, the following register bits are set to a '0' state: Watchdog Register, FT, AFE, ABE, SQWE, and TR. The following bits are set to a '1' state: ST, OUT, and HT (see Table 7., page 22).

Table 6. t_{rec} Definitions

t_{rec} Bit (TR)	STOP Bit (ST)	t_{rec} Time		Units
		Min	Max	
0	0	96	98	ms
0	1	40	200(1)	ms
1	X	50	2000	µs

Note: 1. Default Setting

Table 7. Default Values

Condition	TR	ST	HT	Out	FT	AFE	ABE	SQWE	WATCHDOG Register(1)
Initial Power-up(2)	0	1	1	1	0	0	0	0	0
Subsequent Power-up (with battery back-up)(3)	UC	UC	1	UC	0	0	0	0	0

Note: 1. WDS, BMB0-BMB4, RB0, RB1.
2. State of other control bits undefined.
3. UC = Unchanged

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	SNAPHAT®	–40 to 85	°C
		SOIC	–55 to 125	°C
T_{SLD}	Lead Solder Temperature for 10 seconds	Lead-free lead finish(1)	260	°C
		Standard (SnPb) lead finish(2,3)	240	°C
V_{IO}	Input or Output Voltage		–0.3 to V_{CC}+0.3	V
V_{CC}	Supply Voltage	M41ST85Y	–0.3 to 7	V
		M41ST85W	–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. For SOH28 package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).
2. For SOH28 package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
3. The SOX28 package has Lead-free (Pb-free) lead finish, but cannot be exposed to peak reflow temperature in excess of 240°C (use same reflow profile as standard (SnPb) lead finish).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*
CAUTION: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

DC AND AC PARAMETERS

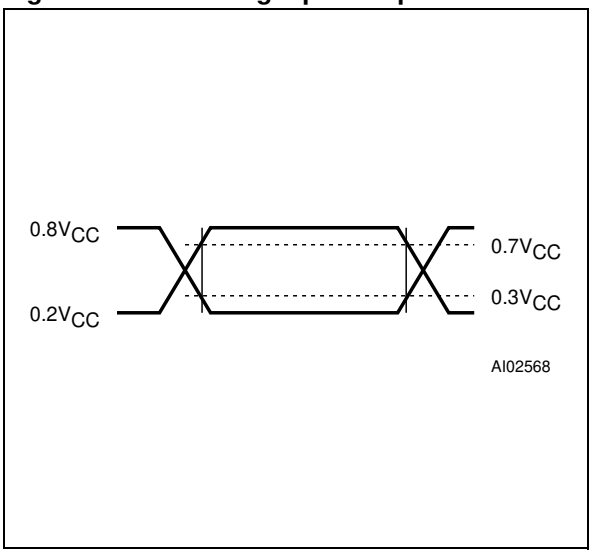
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 9. DC and AC Measurement Conditions

Parameter	M41ST85Y	M41ST85W
V_{CC} Supply Voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient Operating Temperature	–40 to 85°C	–40 to 85°C
Load Capacitance (C_L)	100pF	50pF
Input Rise and Fall Times	≤ 50ns	≤ 50ns
Input Pulse Voltages	0.2 to 0.8V_{CC}	0.2 to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3 to 0.7V_{CC}	0.3 to 0.7V_{CC}

Note: Output High Z is defined as the point where data is no longer driven.

Figure 20. AC Testing Input/Output Waveforms



Note: 50pF for M41ST85W.

Table 10. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		7	pF
C_{OUT}[3]	Output Capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

Note: 1. Effective capacitance measured with power supply at 5V. Sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs are deselected.

Table 11. DC Characteristics

Sym	Parameter	Test Condition(1)	M41ST85Y			M41ST85W			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{BAT}(2)	Battery Current OSC ON	T_A = 25°C, V_{CC} = 0V, V_{BAT} = 3V		400	500		400	500	nA
	Battery Current OSC OFF			50			50		nA
I_{CC1}	Supply Current	f = 400kHz			1.4			0.75	mA
I_{CC2}	Supply Current (Standby)	SCL, SDA = V_{CC} – 0.3V			1			0.50	mA
I_{LI}(3)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}			±1			±1	µA
	Input Leakage Current (PFI)		–25	2	25	–25	2	25	nA
I_{LO}(4)	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}			±1			±1	µA
I_{OUT1}(5)	V_{OUT} Current (Active)	V_{OUT1} > V_{CC} – 0.3V			175			100	mA
I_{OUT2}	V_{OUT} Current (Battery Back-up)	V_{OUT2} > V_{BAT} – 0.3V			100			100	µA
V_{IH}	Input High Voltage		0.7V_{CC}		V_{CC} + 0.3	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.3V_{CC}	–0.3		0.3V_{CC}	V
V_{BAT}	Battery Voltage		2.5	3.0	3.5(9)	2.5	3.0	3.5(9)	V
V_{OH}	Output High Voltage(6)	I_{OH} = –1.0mA	2.4			2.4			V
	Pull-up Supply Voltage (Open Drain)	$\overline{RST}$, $\overline{IRQ}$/FT/OUT			5.5			3.6	V
V_{OHB}(7)	V_{OH} (Battery Back-up)	I_{OUT2} = –1.0µA	2.5	2.9	3.5	2.5	2.9	3.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0mA			0.4			0.4	V
	Output Low Voltage (Open Drain)(8)	I_{OL} = 10mA			0.4			0.4	V
V_{PFD}	Power Fail Deselect		4.20	4.40	4.50	2.55	2.60	2.70	V
V_{PFI}	PFI Input Threshold	V_{CC} = 5V(Y) V_{CC} = 3V(V)	1.225	1.250	1.275	1.225	1.250	1.275	V
	PFI Hysteresis	PFI Rising		20	70		20	70	mV
V_{SO}	Battery Back-up Switchover			2.5			2.5		V

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. Measured with V_{OUT} and $\overline{E}_{CON}$ open.
3. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ internally pulled-up to V_{CC} through 100KΩ resistor. WDI internally pulled-down to V_{SS} through 100KΩ resistor.
4. Outputs Deselected.
5. External SRAM must match RTC SUPERVISOR chip V_{CC} specification.
6. For $\overline{PFO}$ and SQW pins (CMOS).
7. Conditioned output ($\overline{E}_{CON}$) can only sustain CMOS leakage current in the battery back-up mode. Higher leakage currents will reduce battery life.
8. For $\overline{IRQ}$/FT/OUT, $\overline{RST}$ pins (Open Drain): if pulled-up to supply other than V_{CC}, this supply must be equal to, or less than 3.0V when V_{CC} = 0V (during battery back-up mode).
9. For rechargeable back-up, V_{BAT} (max) may be considered V_{CC}.