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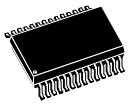
M41ST87W

5.0 and 3.3/3.0 V secure serial RTC and NVRAM supervisor with tamper detection and 128 bytes of clearable NVRAM

Datasheet - production data



28-pin, (300 mil)
SOX28, embedded crystal

SSOP20

Features

- 5.0, 3.3, or 3.0 V operation
- 400 kHz I^2C bus
- NVRAM supervisor to non-volatize external LPSRAM
- 2.5 to 5.5 V oscillator operating voltage
- Automatic switchover and deselect circuitry
- Choice of power-fail deselect voltages
  - M41ST87Y: (not recommended for new design, contact ST sales office for availability)
    THS = 1: V_{PFD}≈ 4.63 V;
    V_{CC} = 4.75 to 5.5 V
    THS = 0: V_{PFD}≈ 4.37 V;
    V_{CC} = 4.5 to 5.5 V
  - M41ST87W:
    THS = 1: V_{PFD} ≈ 2.9 V;
    V_{CC} = 3.0 to 3.6 V
    THS = 0: V_{PFD} ≈ 2.63 V;
    V_{CC} = 2.7 to 3.6 V
- Two independent power-fail comparators (1.25 V reference)
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- 128 bytes of clearable, general purpose NVRAM
- Programmable alarm and interrupt function (valid even during battery backup mode)
- Programmable watchdog timer
- Unique electronic serial number (8-byte)
- 32 kHz frequency output available upon power-on
- Microprocessor power-on reset output
- Battery low flag
- Ultra-low battery supply current of 500 nA (typ)

Security features

- Tamper indication circuits with timestamp and RAM clear
- LPSRAM clear function (TP_{CLR})
- Packaging includes a 28-lead, embedded crystal SOIC and a 20-lead SSOP
- Oscillator stop detection

Contents

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1 Description

The M41ST87Y/W secure serial RTC and NVRAM supervisor is a low power 1280-bit, static CMOS SRAM organized as 160 bytes by 8 bits. A built-in 32.768 kHz oscillator (internal crystal-controlled) and 8 bytes of the SRAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format.

An additional 11 bytes of RAM provide calibration, status/control of alarm, watchdog, tamper, and square wave functions. 8 bytes of ROM and finally 128 bytes of user RAM are also provided. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41ST87Y/W has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, tamper detection, watchdog timer, and programmable square wave output. Other features include a power-on reset as well as two additional debounced inputs ($\overline{RSTIN1}$ and $\overline{RSTIN2}$) which can also generate an output reset ($\overline{RST}$). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30 and 31 day months are made automatically.

Security features

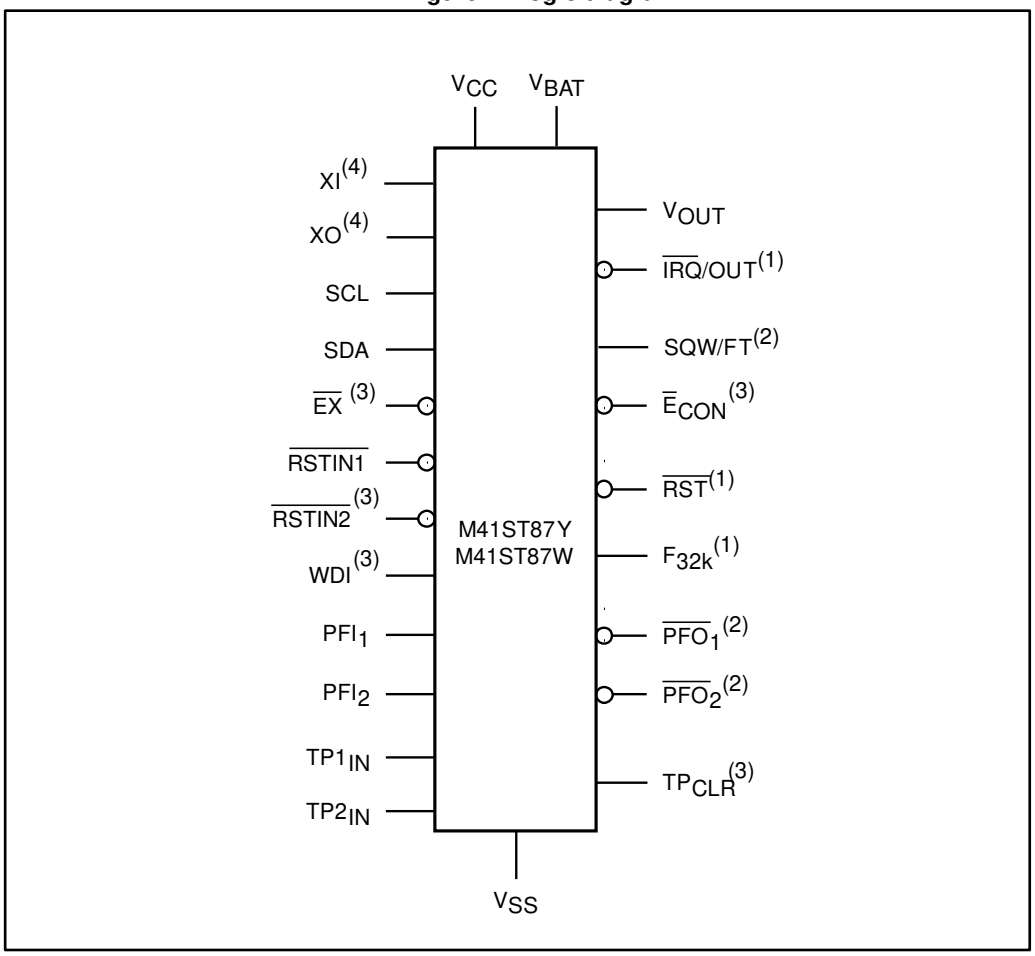
Two fully independent tamper detection Inputs allow monitoring of multiple locations within the system. User programmable bits provide both normally open and normally closed switch monitoring. Time stamping of the tamper event is automatically provided. There is also an option allowing data stored in either internal memory (128 bytes), and/or external memory to be cleared, protecting sensitive information in the event tampering occurs. By embedding the 32 kHz crystal in the SOX28 package, the clock is completely isolated from external tampering. An oscillator fail bit (OF) is also provided to ensure correct operation of the oscillator.

The M41ST87Y/W is supplied in a 28-pin, 300 mil SOIC package which includes an embedded 32 kHz crystal and a 20-pin SSOP package for use with an external crystal.

The SOIC and SSOP packages are shipped in plastic anti-static tubes or in tape and reel form.

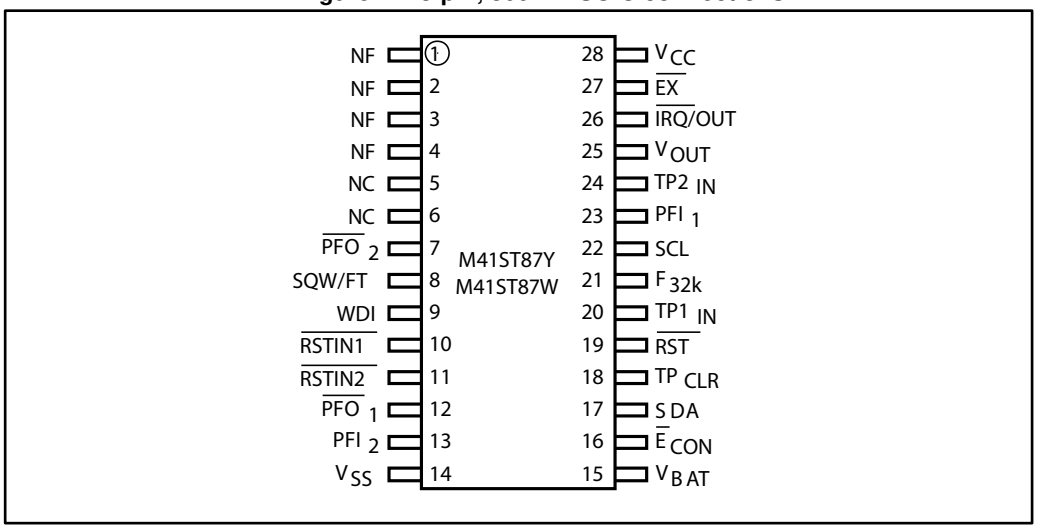
The 300 mil, embedded crystal SOIC requires only a user-supplied battery to provide non-volatile operation.

Figure 1: Logic diagram



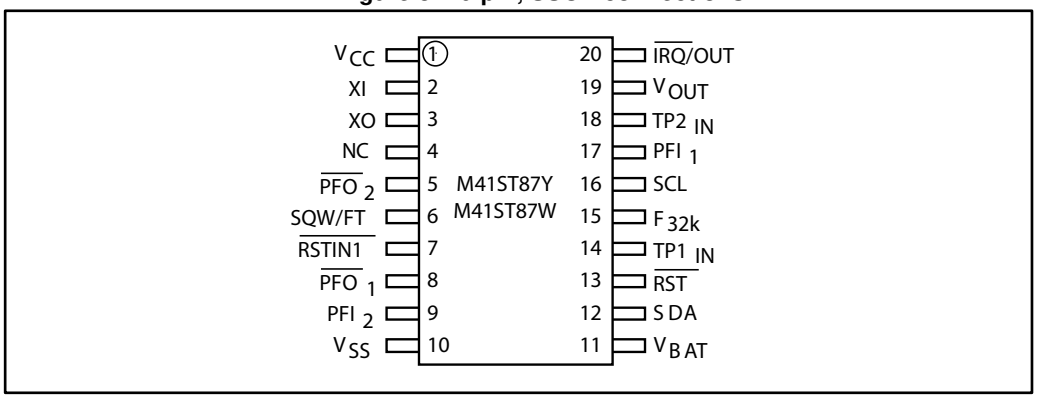
1. Open drain output.
2. Programmable output (open drain or full-CMOS). Defaults to open drain on first power-up.
3. Available in SOX28 package only.
4. Available in SSOP package only.

Figure 2: 28-pin, 300 mil SOIC connections



Note: No function (NF) and no connect (NC) pins should be tied to V_{SS}. Pins 1, 2, 3, and 4 are internally shorted together.

Figure 3: 20-pin, SSOP connections



Note: No connect (NC) pin should be tied to V_{SS}.

Table 1: Signal names

XI (1)	Oscillator input
XO(1)	Oscillator output
$\overline{E}_{CON}$ (2)	Conditioned chip enable output
$\overline{EX}$(2)	External chip enable
$\overline{IRQ}$/OUT (3)	Interrupt/out output (open drain)
PFI_1	Power fail input 1
PFI_2	Power fail input 2
$\overline{PFO}_1$ (4)	Power fail output 1
$\overline{PFO}_2$(4)	Power fail output 2
$\overline{RST}$(3)	Reset output (open drain)
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$(2)	Reset 2 input
SCL	Serial clock input
SDA	Serial data input/output
SQW/FT(4)	Square wave output/frequency test
WDI(2)	Watchdog input
V_{CC}	Supply voltage
V_{OUT}	Voltage output
V_{SS}	Ground
F_{32k}(3)	32 kHz square wave output (open drain)
$TP1_{IN}$	Tamper pin 1 input
$TP2_{IN}$	Tamper pin 2 input
TP_{CLR}(2)	Tamper pin RAM clear
V_{BAT}	Positive battery pin input
NF (5)	No function
NC(5)	No connect

Notes:

(1)Available in SSOP package only.

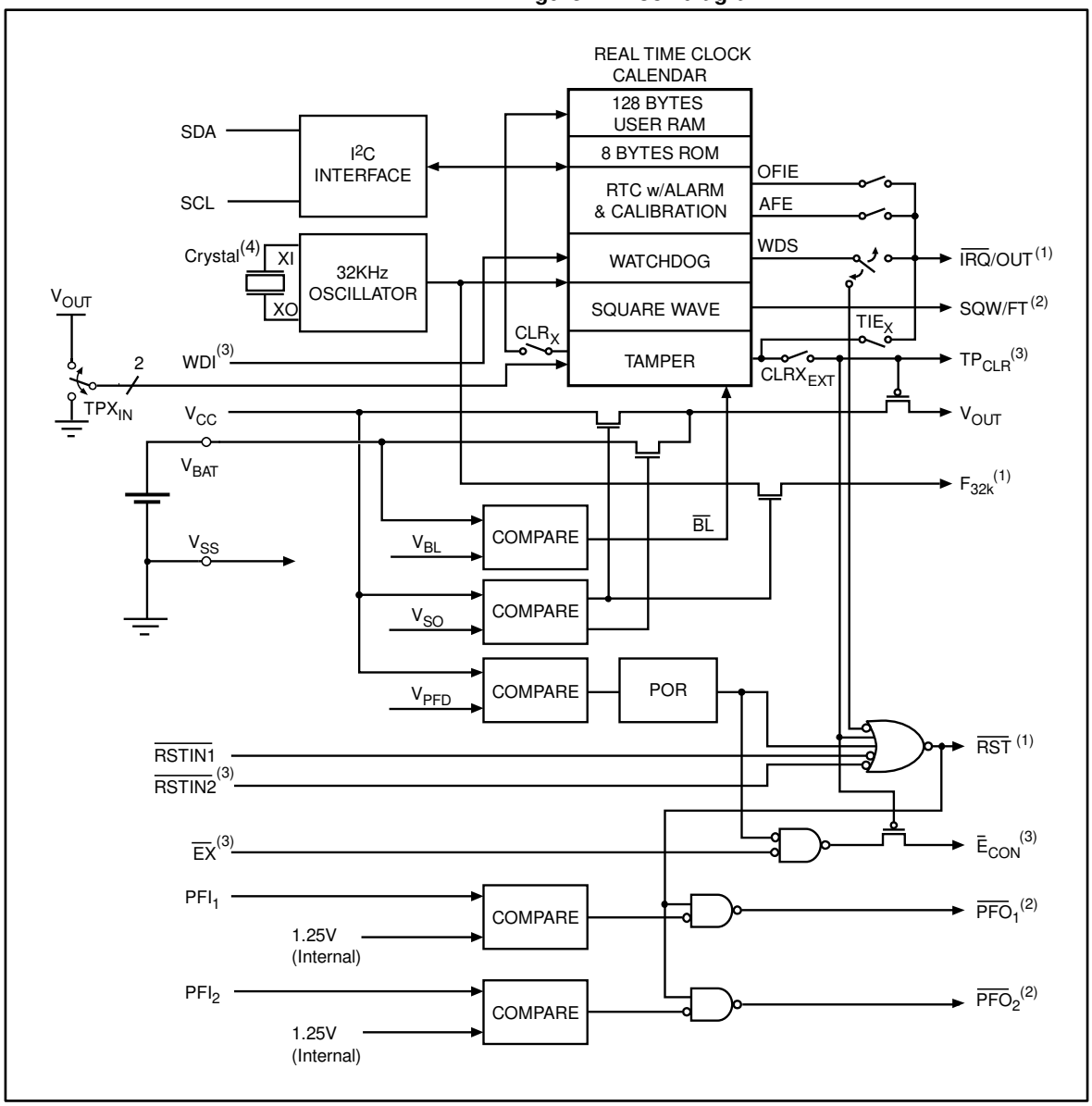
(2)Available in SOX28 package only.

(3)Open drain output.

(4)Programmable output (open drain or full-CMOS).

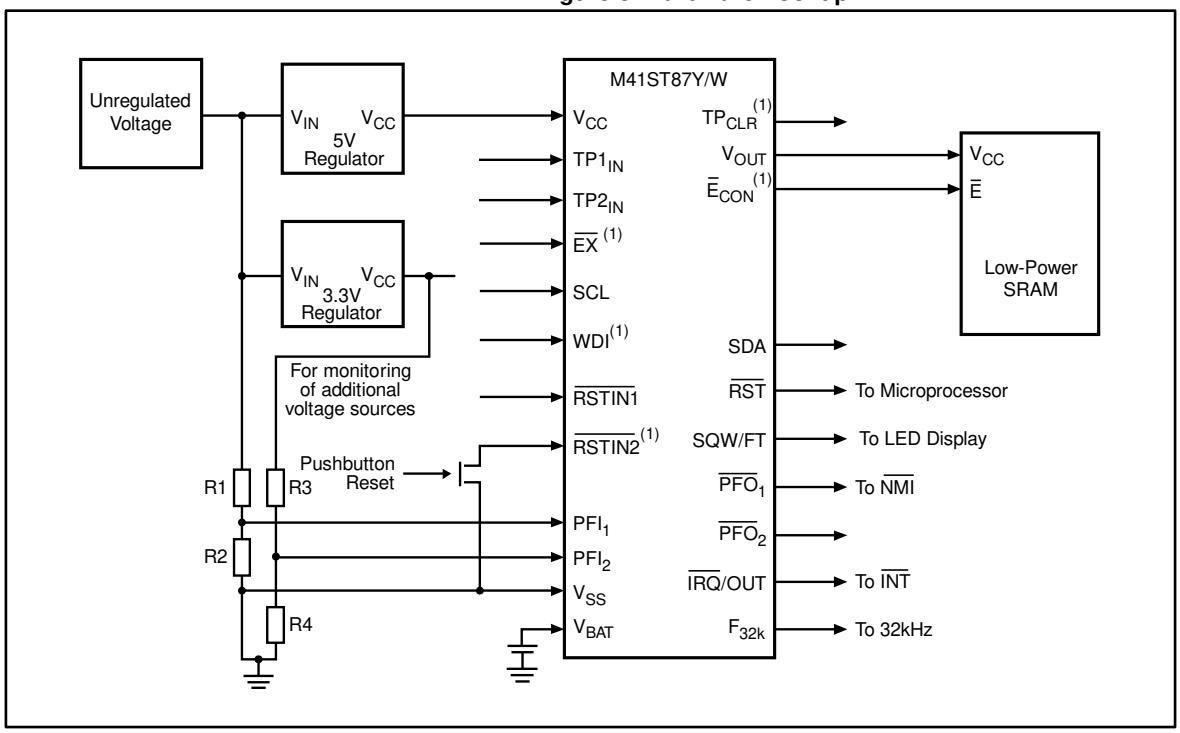
(5)Should be connected to V_{SS}.

Figure 4: Block diagram



1. Open drain output.
2. Programmable output (open drain or full-CMOS); if open drain option is selected and if pulled-up to supply other than V_{CC}, this supply must be equal to, or less than V_{BAT} when V_{CC} = 0 V (during battery backup mode).
3. Available in SOX28 package only.
4. Crystal is external on SSOP package and internal for the SOX28 package.

Figure 5: Hardware hookup



1. Available in SOX28 package only.

2 Operating modes

The M41ST87Y/W clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h).

Table 2: I^2C slave address

7-bit I^2C slave address	0x68
8-bit I^2C slave address	Write: 0xD0
	Read: 0xD1

The 160 bytes contained in the device can then be accessed sequentially in the following order:

00h. Tenths/hundredths of a second register

01h. Seconds register

02h. Minutes register

03h. Century/hours register

04h. Day register

05h. Date register

06h. Month register

07h. Year register

08h. Control register

09h. Watchdog register

0Ah-0Eh. Alarm registers

0Fh. Flag register

10h-12h. Reserved

13h. Square wave

14h. Tamper register 1

15h. Tamper register 2

16h-1Dh. Serial number (8 bytes)

1Eh-1Fh. Reserved (2 bytes)

20h-9Fh. User RAM (128 bytes)

The M41ST87Y/W clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the device is switched to external V_{CC}.

Write protection continues until t_{rec} (min) elapses after V_{CC} reaches V_{PFD} (min).

For more information on battery storage life refer to application note AN1012.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a clock signal (SCL) and a bidirectional data signal (SDA). The SDA line must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 6: Serial bus data transfer sequence

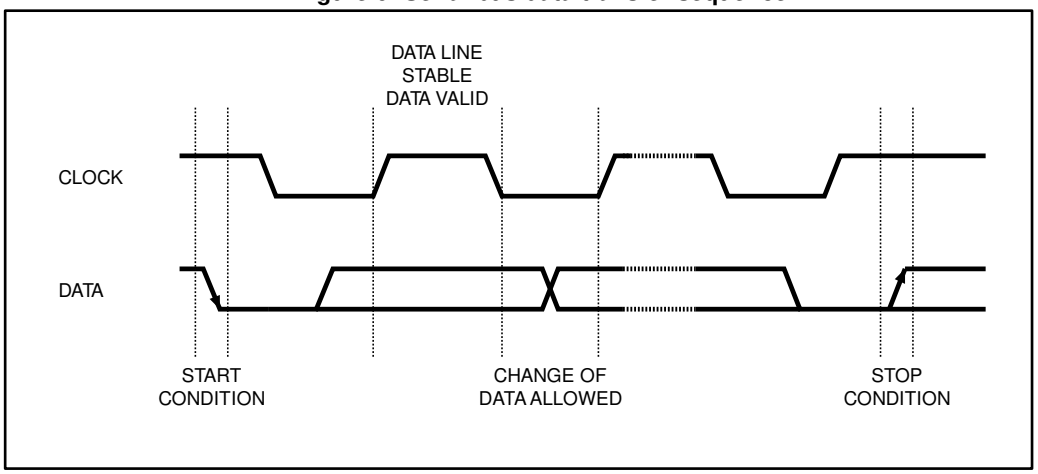


Figure 7: Acknowledgement sequence

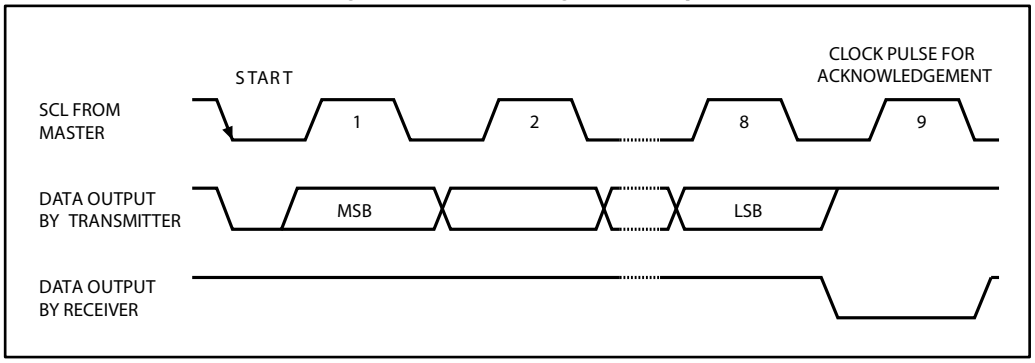


Figure 8: Bus timing requirements sequence

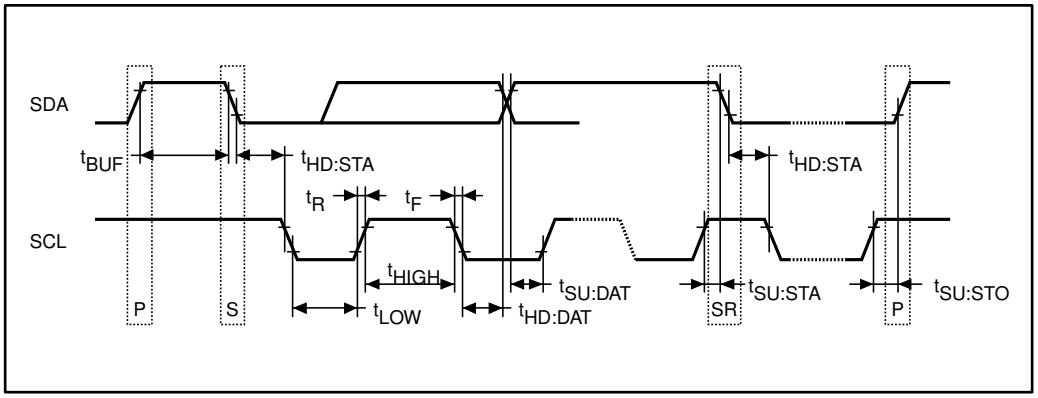


Table 3: AC characteristics

Symbol	Parameter (1)		Min	Max	Unit
f_{SCL}	SCL clock frequency		0	400	kHz
t_{BUF}	Time the bus must be free before a new transmission can start		1.3		µs
t_{EXPD} (2)	$\overline{EX}$ to $\overline{E}_{CON}$ propagation delay	M41ST87Y		10	ns
		M41ST87W		15	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:DAT}$ (3)	Data hold time		0		µs
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)		600		ns
t_{HIGH}	Clock high period		600		ns
t_{LOW}	Clock low period		1.3		µs
t_R	SDA and SCL rise time			300	ns
$t_{SU:DAT}$	Data setup time		100		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)		600		ns
$t_{SU:STO}$	STOP condition setup time		600		ns

Notes:

(1) Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V (except where noted).

(2) Available in SOX28 package only.

(3) Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

2.2 READ mode

In this mode the master reads the M41ST87Y/W slave after setting the slave address (see *Figure 9: "Slave address location"*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver.

The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41ST87Y/W slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter (see *Figure 10: "READ mode sequence"*).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41ST87Y/W slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 11: "Alternate READ mode sequence"*).

Figure 9: Slave address location

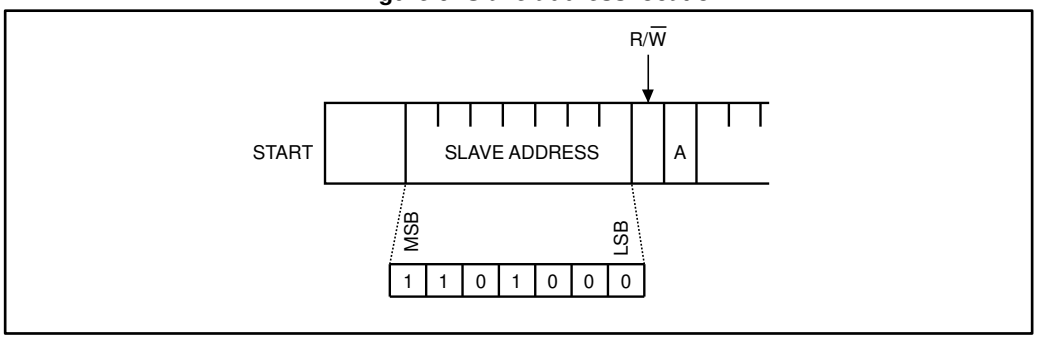


Figure 10: READ mode sequence

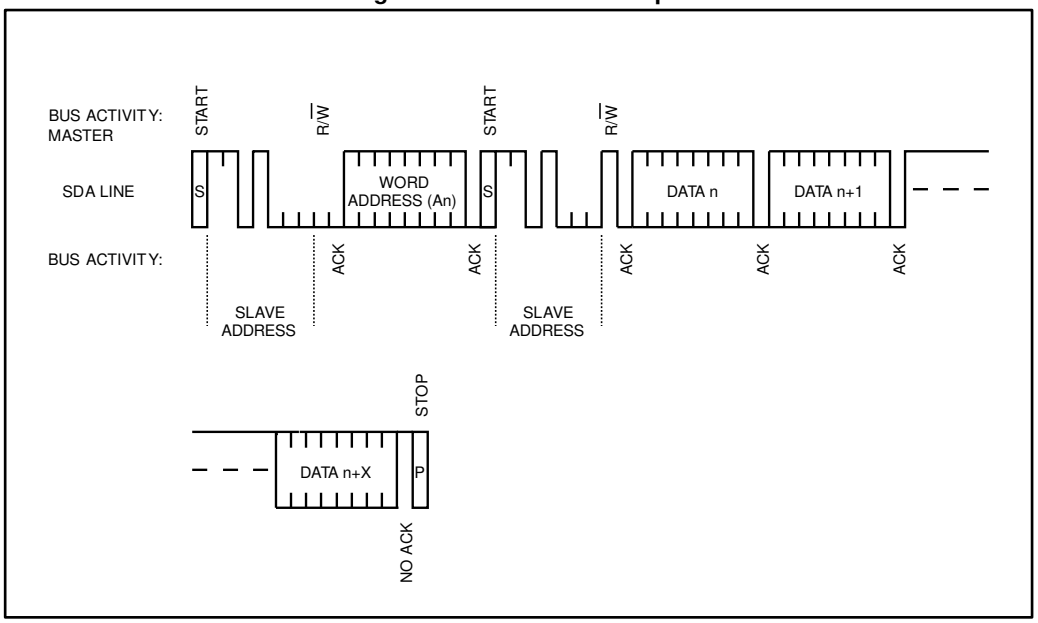
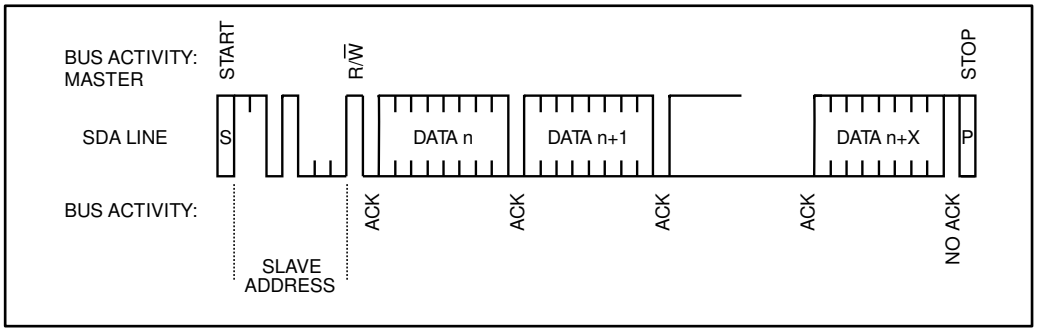


Figure 11: Alternate READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41ST87Y/W slave receiver. Bus protocol is shown in *Figure 12: "WRITE mode sequence"*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41ST87Y/W slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Figure 9: "Slave address location"*) and again after it has received the word address and each data byte.

Figure 12: WRITE mode sequence

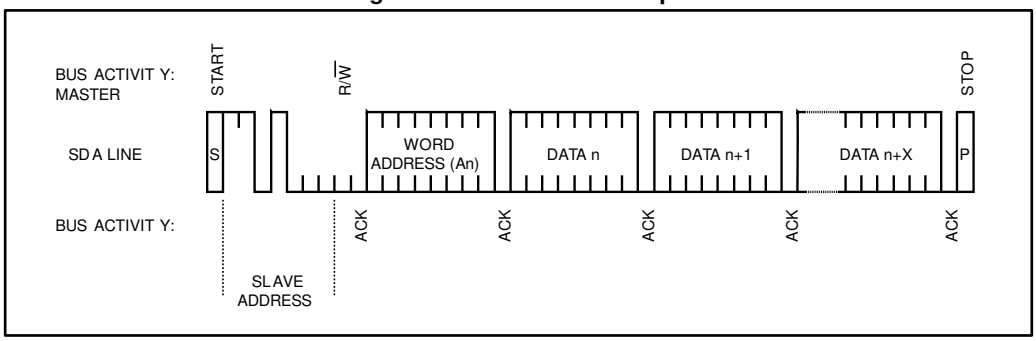
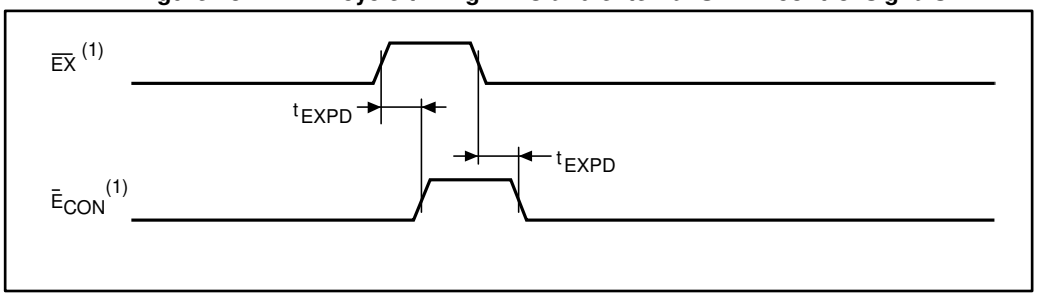


Figure 13: WRITE cycle timing: RTC and external SRAM control signals



1. Available in SOX28 package only.

2.4 Data retention mode

With valid V_{CC} applied, the M41ST87Y/W can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41ST87Y/W will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min) (see *Figure 28: "Power down/up mode AC waveforms"*, *Table 21: "Power down/up AC characteristics"*). This is accomplished by internally inhibiting access to the clock registers. At this time, the reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{E}_{CON}$ to a high level. This level is within 0.2 volts of the V_{BAT}. $\overline{E}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition. When V_{CC} falls below the battery backup switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the battery, and the clock registers and external SRAM are maintained from the attached battery supply.

All signal outputs become high impedance. The V_{OUT} pin is capable of supplying 100 µA of current to the attached memory with less than 0.3 volts drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{rec} by inhibiting

$\overline{E}_{CON}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 28: "Power down/up mode AC waveforms"*).

Note: Most low power SRAMs on the market today can be used with the M41ST87Y/W RTC SUPERVISOR. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41ST87Y/W and SRAMs to be "Don't Care" once V_{CC} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC} = 2.0 volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M41ST87Y/W to determine the total current requirements for data retention. The available battery capacity for the battery of your choice can then be divided by this current to determine the amount of data retention available.

For a further more detailed review of lifetime calculations, please see application note AN1012.

2.5 Tamper detection circuit

The M41ST87Y/W provides two independent input pins, the tamper pin 1 input ($TP1_{IN}$) and tamper pin 2 input ($TP2_{IN}$), which can be used to monitor two separate signals which can result in the associated setting of the tamper bits (TB1 and/or TB2, in flag register 0Fh) if the tamper enable bits (TEB1 and/or TEB2) are enabled, for the respective tamper 1 or tamper 2 channels. The $TP1_{IN}$ pin or $TP2_{IN}$ pin may be set to indicate a tamper event has occurred by either 1) closing a switch to ground or V_{OUT} (normally open), or by 2) opening a switch that was previously closed to ground or V_{OUT} (normally closed), depending on the state of the TCM_X bits and the TPM_X bits in the tamper register (14h and/or 15h).

2.6 Tamper register bits (tamper 1 and tamper 2)

2.6.1 Tamper enable bits (TEB1 and TEB2)

When set to a logic '1,' this bit will enable the tamper detection circuit. This bit must be set to '0' in order to clear the associated tamper bits (TB_X, in 0Fh).

Note: TEB_X should be cleared then set again whenever the tamper detect condition is modified.

When servicing a tamper interrupt, the TEB_x bits must be cleared to clear the TB_x bits, then set to 1 to again enable the tamper detect circuits.

2.6.2 Tamper bits (TB1 and TB2)

If the TEB_X bit is set, and a tamper condition occurs, the TB_X bit will be set to '1.' This bit is "Read-only" and is reset only by setting the TEB_X bit to '0.' These bits are located in the flags register 0Fh.

2.6.3 Tamper interrupt enable bits (TIE1 and TIE2)

If this bit is set to a logic '1,' the $\overline{IRQ}$/OUT pin will be activated when a tamper event occurs. This function is also valid in battery backup if the ABE bit (alarm in battery backup) is also set to '1' (see *Figure 15: "Basic tamper detect options"*).

Note: In order to avoid an inadvertent activation of the $\overline{IRQ}$/OUT pin due to a prior tamper event, the flag register (0Fh) should be read prior to clearing and again setting the TEB_X bit.

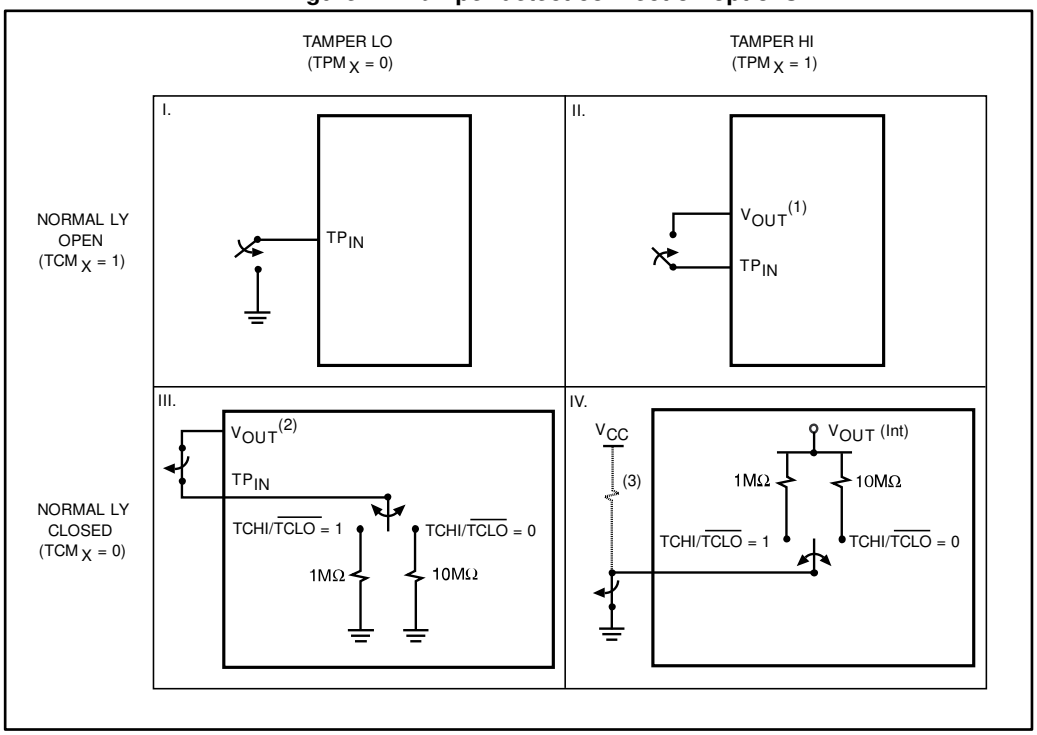
2.6.4 Tamper connect mode bit (TCM1 and TCM2)

This bit indicates whether the position of the external switch selected by the user is in the normally open (TCM_X = '1') or normally closed (TCM_X = '0') position (see *Figure 14: "Tamper detect connection options"* and *Figure 16: "Tamper detect output options"*).

2.6.5 Tamper polarity mode bits (TPM1 and TPM2)

The state of this bit indicates whether the tamper pin input will be taken high (to V_{OUT} if TPM_X = '1') or low (to V_{SS} if TPM_X = '0') to trigger a tamper event (see *Figure 14: "Tamper detect connection options"* and *Figure 16: "Tamper detect output options"*).

Figure 14: Tamper detect connection options



Note: These options are summarized in Table 4: "Tamper detection truth table".

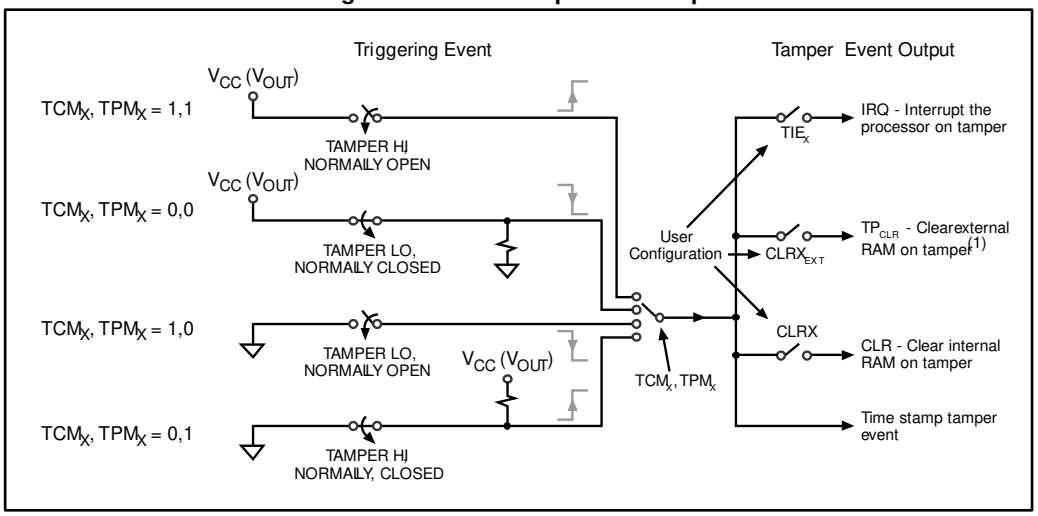
1. If the $CLRX_{EXT}$ bit is set, a second tamper to V_{OUT} (TPM2 = '1') during t_{CLR} will not be detected.
2. If the $CLRX_{EXT}$ bit is set, a second tamper to V_{OUT} (TPM2 = '1') will trigger automatically.
3. Optional external resistor to V_{CC} allows the user to bypass sampling when power is "on."

Table 4: Tamper detection truth table

Option	Mode	TCM_X	TPM_X
I	Normally open/tamper to GND (1)	1	0
II	Normally open/tamper to V_{OUT} (1)	1	1
III	Normally closed/tamper to GND	0	0
IV	Normally closed/tamper to V_{OUT}	0	1

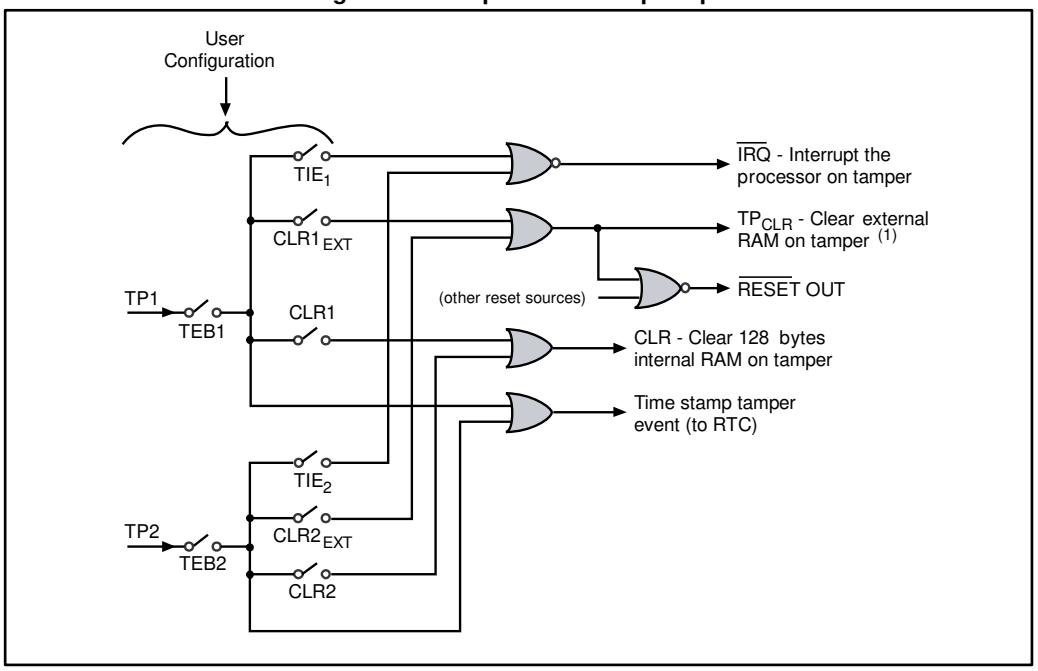
Notes:
(1) No battery current drawn during battery backup.

Figure 15: Basic tamper detect options



1. Available in SOX28 package only.

Figure 16: Tamper detect output options



1. Available in SOX28 package only.

2.6.6 Tamper detect sampling (TDS1 and TDS2)

This bit selects between a 1 Hz sampling rate or constant monitoring of the tamper input pin(s) to detect a tamper event when the normally closed switch mode is selected. This allows the user to reduce the current drain when the TEB_X bit is enabled while the device is in battery backup (see *Table 5: "Tamper detection current (normally closed - TCMX = '0')"* and *Figure 17: "Tamper detect sampling options"*). Sampling is disabled if the TCM_X bit is set to logic '1' (Normally Open). In this case the state of the TDS_X bit is a "Don't care."

Note: The crystal oscillator must be "on" for sampling to function. If the oscillator is stopped, the tamper detect circuit will revert to continuous monitoring.

2.6.7 Tamper current high/tamper current low (TCHI/$\overline{\text{TCLO}}$1 and TCHI/$\overline{\text{TCLO}}$2)

This bit selects the strength of the internal pull-up or pull-down used during the sampling of the normally closed condition. The state of the TCHI/$\overline{\text{TCLO}}_X$ bit is a "Don't care" for normally open (TCM_X = '1') mode (see *Figure 18: "Tamper current options"*).

2.6.8 RAM clear (CLR1 and CLR2)

When either CLR1 or CLR2 and the TEB_X bit are set to a logic '1,' the internal 128 bytes of user RAM (see *Figure 15: "Basic tamper detect options"*) will be cleared to all zeros in the event of a tamper condition. Furthermore, the 128 bytes of user RAM will be deselected (inaccessible) until the corresponding TEB_X bit is reset to '0.' Any data read during this time will be invalid. (ie. the cleared RAM values cannot be accessed.)

2.6.9 RAM clear external ($CLR1_{EXT}$ and $CLR2_{EXT}$) - available in SOX28 package only

When either $CLR1_{EXT}$ or $CLR2_{EXT}$ is set to a logic '1' and the TEB_X bit is also set to logic '1,' the TP_{CLR} signal will be asserted for clearing external RAM, and the RST output asserted upon detection of a tamper event (see *Figure 15: "Basic tamper detect options"* and *Figure 20: "RAM clear hardware hookup (SOX28 package only)"*).

Note: The reset output resulting from a tamper event will be the same as a reset resulting from a power-down condition, a watchdog time-out, or a manual reset ($\overline{\text{RSTIN1}}$ or $\overline{\text{RSTIN2}}$); the $\overline{\text{RST}}$ output will be asserted for t_{rec} seconds.

This is accomplished by forcing TP_{CLR} high, which if used to control the inhibit pin of the DC regulator (see *Figure 20: "RAM clear hardware hookup (SOX28 package only)"*) will also switch off V_{OUT}, depriving the external SRAM of power to the V_{CC} pin. V_{OUT} will automatically be disconnected from the battery if the tamper occurs during battery back-up (see *Figure 19: "Tamper output timing (with CLR1EXT or CLR2EXT = '1') - available in SOX28 package only"*). By inhibiting the DC regulator, the user will also prevent other inputs from sourcing current to the external SRAM, which would allow it to retain data otherwise.

The user may optionally connect an inverting charge pump to the V_{CC} pin of the external SRAM (see *Figure 20: "RAM clear hardware hookup (SOX28 package only)"*). Depending on the process technology used for the manufacturing of the external SRAM, clearing the memory may require varying durations of negative potential on the V_{CC} pin. This device configuration will allow the user to program the time needed for their particular application. Control Bits CLRPW0 and CLRPW1 determine the duration TP_{CLR} will be enabled (see *Figure 19: "Tamper output timing (with CLR1EXT or CLR2EXT = '1') - available in SOX28 package only"* and *Table 6: "Tamper detect timing"*).

Note: When using the inverting charge pump, the user must also provide isolation in the form of two additional small-signal power MOSFETs. These will isolate the V_{OUT} pin from both the negative voltage generated by the charge pump during a tamper condition, and

from being pulled to ground by the output of the charge pump when it is in shut-down mode ($\overline{SHDN}$ = logic low). The gates of both MOSFETs should be connected to TP_{CLR} as shown in Figure 20: "RAM clear hardware hookup (SOX28 package only)". One n-channel enhancement MOSFET should be placed between the output of the inverting charge pump and the V_{OUT} of the M41ST87. The other MOSFET should be an enhancement mode p-channel, and placed between V_{OUT} of the M41ST87 and V_{CC} of the external SRAM. When TP_{CLR} goes high after a tamper condition occurs, the n-channel MOSFET will turn on and the p-channel will turn off. During normal operating conditions, TP_{CLR} will be low and the p-channel will be on, while the n-channel will be off.

Table 5: Tamper detection current (normally closed - TCMX = '0')

TDS_X	$TCHI/\overline{TCLO}_X$	Tamper circuit mode	Current at 3.0 V (typ) (1)(2)	Unit
0	0	Continuous monitoring / 10 MW pull-up/-down	0.3	µA
0	1	Continuous monitoring / 1 MW pull-up/-down	3.0	µA
1	0	Sampling (1 Hz) / 10 MW pull-up/-down	0.3	nA
1	1	Sampling (1 Hz) / 1 MW pull-up/-down	3.0	nA

Notes:

(1)Per tamper detect input

(2)When calculating battery lifetime, this current should be added to I_{BAT} current listed in *Table 19: "DC characteristics"*.

Figure 17: Tamper detect sampling options

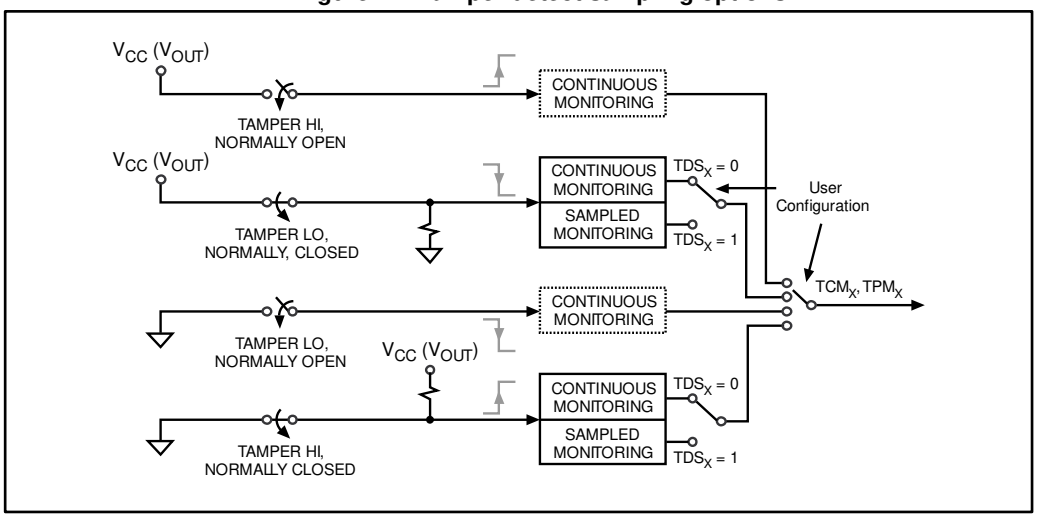


Figure 18: Tamper current options

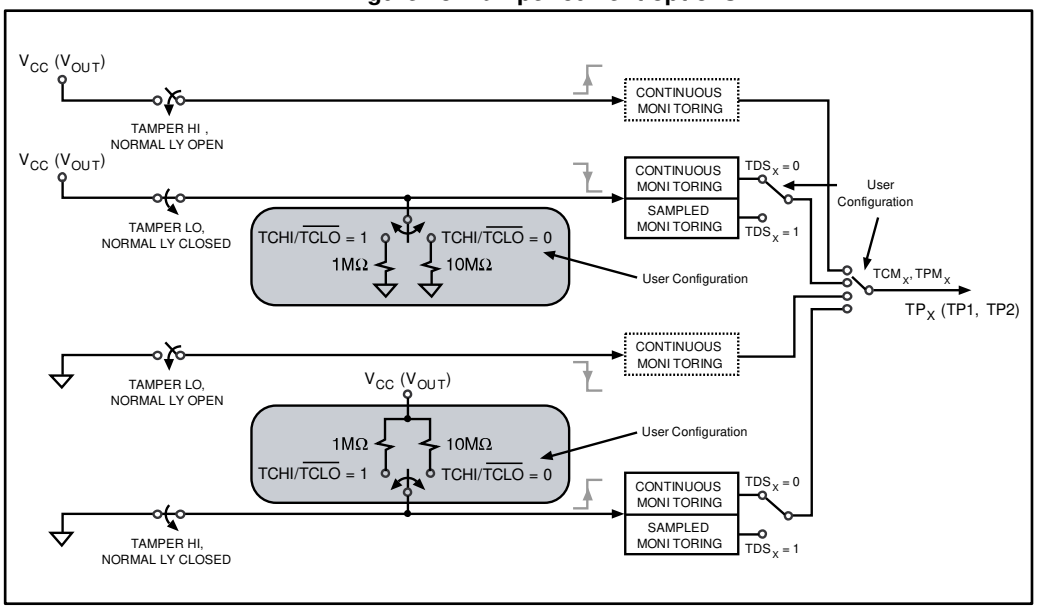
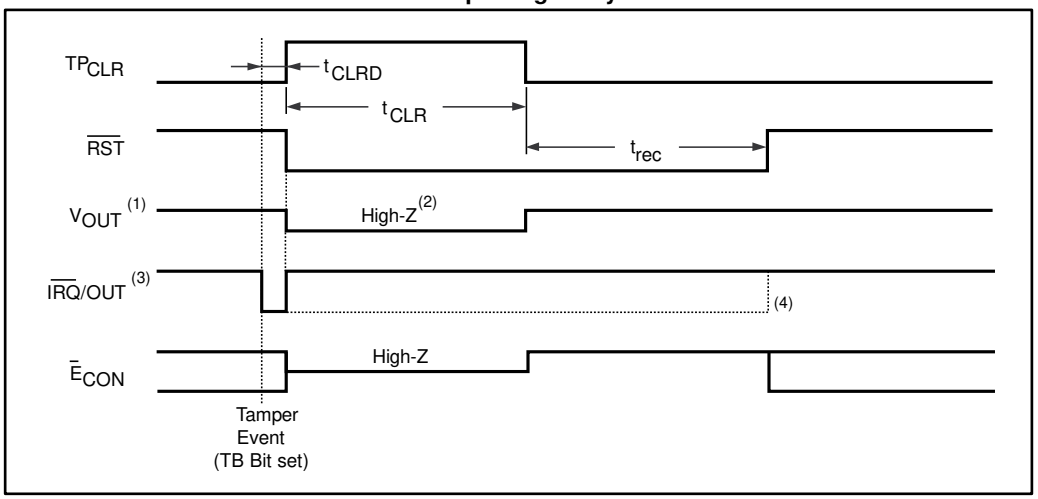


Figure 19: Tamper output timing (with CLR1EXT or CLR2EXT = '1') - available in SOX28 package only



1. If connected to a negative charge pump device, this pin must be isolated from the charge pump by using both n-channel and p-channel MOSFETs as illustrated in *Figure 20: "RAM clear hardware hookup (SOX28 package only)"*.
2. If the device is in battery back-up; NOT on V_{CC} (see *Section 2.6.9: "RAM clear external (CLR1EXT and CLR2EXT) - available in SOX28 package only"*). V_{OUT} is forced to GND during a tamper event when on V_{CC}.
3. If TIE_X = '1.'
4. If ABE = '1' and device is in battery backup mode.

Table 6: Tamper detect timing

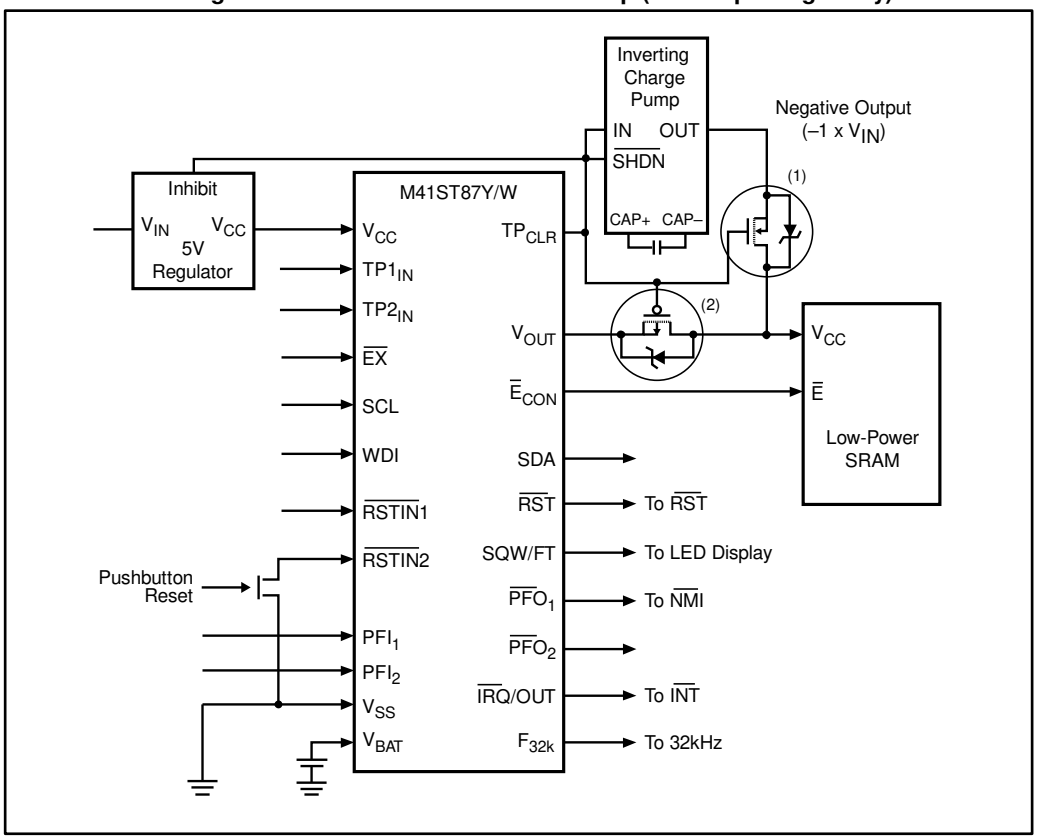
Symbol	Parameter	CLRPW1	CLRPW0	Min	Typ	Max	Unit
t_{CLRD} (1)	Tamper RAM clear ext delay	X	X	1.0 (2)	1.5	2.0	ms
t_{CLR}	Tamper clear timing	0	0		1		s
		0	1		4		s
		1	0		8		s
		1	1		16		s

Notes:

(1)With input capacitance = 70 pF and resistance = 50 Ω.

(2)If the OF bit is set, t_{CLRD}(min) = 0.5 ms.

Figure 20: RAM clear hardware hookup (SOX28 package only)



1. Most inverting charge pumps drive OUT to ground when device shut down is enabled ($\overline{SHDN}$ = logic low). Therefore, an n-channel enhancement mode MOSFET should be used to isolate the OUT pin from the V_{OUT} of the M41ST87.
2. In order to avoid turning on an on-chip parasitic diode when driving V_{OUT} negative, a p-channel enhancement mode MOSFET should be used to isolate the V_{OUT} pin from the negative voltage generated by the inverting charge pump.

2.7 Tamper detection operation

The tamper pins are triggered based on the state of an external switch. Two switch mode options are available, normally open or normally closed, based on the setting of the tamper connect mode bit (TCM_X). If the selected switch mode is normally open (TCM_X = '1'), the tamper pin will be triggered by being connected to V_{SS} (if the TPM_X bit is set to '0') or to V_{CC} (if the TPM_X bit is set to '1'), through the closing of the external switch. When the external switch is closed, the tamper bit (TB_x) will be immediately set, allowing the user to determine if the device has been physically tampered with. If the selected switch mode is normally closed (TCM_X = '0'), the tamper pin will be triggered by being pulled to V_{SS} or to V_{OUT} (depending on the state of the TPM_X bit), through an internal pull-up/pull-down resistor as a result of opening the external switch.

When a tamper event occurs, the tamper bits (TB1 and/or TB2) will be immediately set if TEB_X = '1.'

If the tamper interrupt enable bit (TIE_X) is set to a '1,' the $\overline{IRQ}$/OUT pin will also be activated. The $\overline{IRQ}$/OUT output is cleared by a READ of the flags register (as seen in *Figure 24: "Alarm interrupt reset waveform"*), a reset of the TIE bit to '0,' or the $\overline{RST}$ output is asserted.

Note: In order to avoid an inadvertent activation of the $\overline{IRQ}$/OUT pin due to a prior tamper event, the flag register (0Fh) should be read prior to resetting the TEB_X bit.

The tamper bits are “read only” bits and are reset only by writing the tamper enable bit (TEB_X) to '0.' Thus, when servicing a tamper interrupt, the user should read the flags register to clear the $\overline{IRQ}$ pin, then clear the TEB_x bit to clear the TB_x flag, followed by setting TEB_x to again enable the tamper circuit.

The tamper detect function operates both under normal power, and in battery backup. Even if the trigger event occurs during a power-down condition, the tamper flag bit(s) will be set correctly.

2.8 Sampling

As the switch mode normally closed (TCM_X = '0') requires a greater amount of current to maintain constant monitoring, the M41ST87Y/W offers a programmable tamper detect sampling bit (TDS_X) to reduce the current drawn on V_{CC} or V_{BAT} (see *Figure 17: "Tamper detect sampling options"*). When enabled, the sampling frequency is once per second (1Hz), for a duration of approximately 1 ms.

When TEB_X is disabled, no current will be drawn by the tamper detection circuit. After a tamper event has been detected, no additional current will be drawn.

Note: The oscillator must be running for tamper detection to operate in the sampling mode. If the oscillator is stopped, the tamper detection circuit will revert to constant monitoring.

Note: Sampling in the tamper high mode (TPM_X = '1') may be bypassed while on V_{CC} by connecting the TPx_{IN} pin to V_{CC} through an external resistor. This will allow constant monitoring when V_{CC} is “on” and revert to sampling when in battery backup (see Figure 14: "Tamper detect connection options").