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M41T00AUD

Serial real-time clock (RTC) with audio

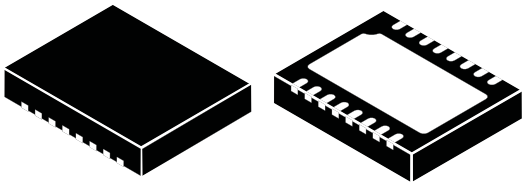
Features

Combination real-time clock with audio

- Serial real-time clock (RTC) based on M41T00
- Audio section provides:
  - 300 mW differential audio amplifier
  - 256 and 512 Hz tone generation
  - –33 to +12 dB gain, 3 dB steps (16 steps plus MUTE)
- 0 °C to 70 °C operation
- Small DFN16 package (5 mm x 4 mm)

Real-time clock details

- Superset of M41T00
- 3.0 to 3.6 V operation
  - Timekeeping down to 1.7 V
- Automatic backup switchover circuit
  - Ultra-low 400 nA backup current at 3.0 V (typ)
  - Suitable for battery or capacitor backup
  - On-chip trickle charge circuit for backup capacitor
- 400 kHz I^2C bus
- M41T00 compatible register set with counters for seconds, minutes, hours, day, date, month, years, and century
  - Automatic leap year compensation
  - HT bit set when clock goes into backup mode
- RTC operates using 32,768 Hz quartz crystal
  - Calibration register provides for adjustments of –63 to +126 ppm
  - Oscillator supports crystals with up to 40 kΩ series resistance, 12.5 pF load capacitance
- Oscillator fail detect circuit OF bit indicates when oscillator has stopped for four or more cycles



DFN16 (5 mm x 4 mm)

Audio section

- Power amplifier
  - Differential output amplifier
  - Provides 300 mW into 8 Ω (THD+N = 2% (max), f_{in} = 1 kHz)
- Summing node at audio input
  - Inverting configuration with summing resistors into the minus (-) terminal
  - 0 dB gain with 10 kΩ feedback resistor and 20 kΩ input summing resistors
  - Signal input centered at $V_{DD}/2$
  - 1.6 V_{P-P} analog input range (max)
- 256 or 512 Hz signal multiplexing with analog input to provide audio with beep tones
- Volume control, 4-bit register
  - Allows gain adjustment from –33 dB to +12 dB
  - 3 dB steps
  - MUTE bit
- Audio automatically shuts off in backup mode

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1 Description

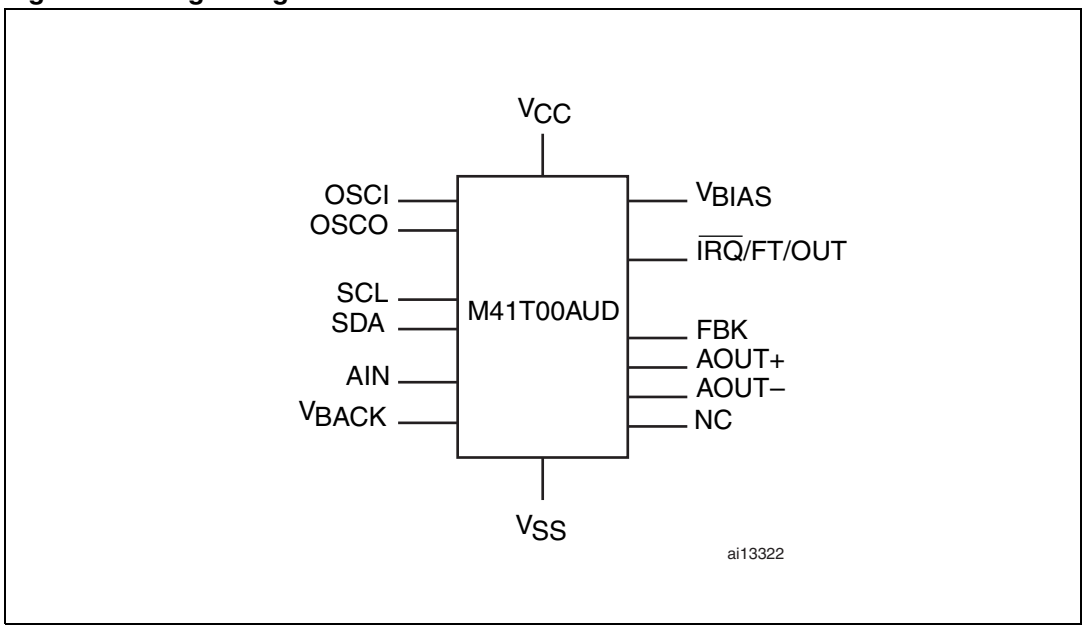
The M41T00AUD is a low-power serial real-time clock (RTC) with an integral audio section with tone generator and 300 mW output amplifier. The RTC is a superset of the M41T00 with enhancements such as a precision reference for switchover, an oscillator fail detect circuit, and storing of the time at power-down. The audio section includes a summing amplifier (inverting) at the input. An 8 kHz low-pass filter follows that with a 16-step programmable gain stage next. A 256 or 512 Hz audio tone can be switched into the filter in place of the input signal. From the gain stage, the 300 mW amplifier drives the output pins.

The M41T00AUD has a built-in power sense circuit which detects power failures and automatically switches to the backup input when V_{CC} is removed. Backup power can be supplied by a capacitor or by a battery such as a lithium coin cell. The device includes a trickle charge circuit for charging the capacitor.

The RTC includes a built-in 32.768 kHz oscillator controlled by an external crystal. Eight register bytes are used for the clock/calendar functions and are superset compatible with the M41T00. Two additional registers control the audio section and the trickle charger. The 10 registers (see *Table 2*) are accessed over a 400 kHz I^2C bus. The address register increments automatically after each byte READ or WRITE operation thus streamlining transfers by eliminating the need to send a new address for each byte to be transferred.

Typical data retention times will be in excess of 5 years with a 50 mAh 3 V lithium cell (see RTC DC characteristics, *Table 12* for more information).

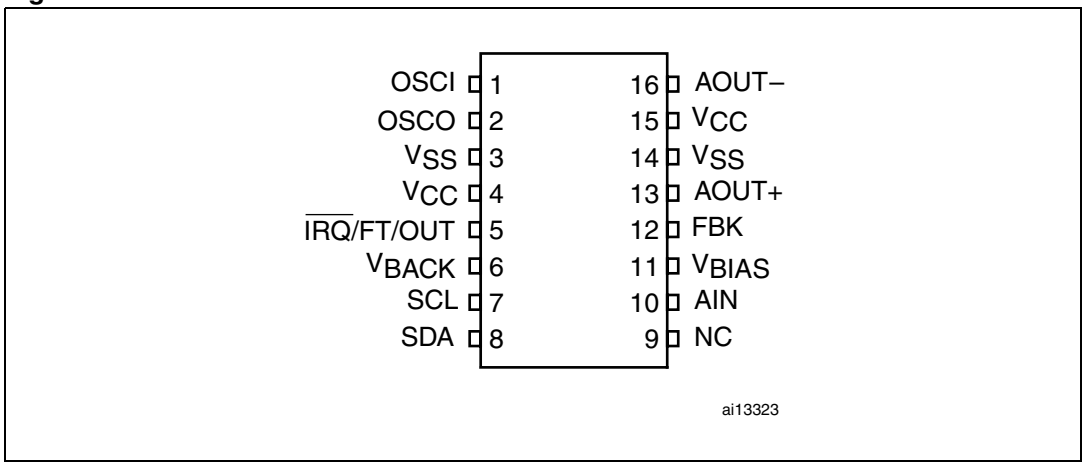
Figure 1. Logic diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection



2.2 Pin description

Table 1. Pin description

Symbol	Name and function
V_{CC}	Supply voltage
OSCI	Oscillator input
OSCO	Oscillator output
SCL	I^2C serial clock
SDA	I^2C serial data
AIN	Audio input
V_{BIAS}	Input for decoupling capacitor
V_{SS}	Ground
AOUT–	Analog out, 180 phase
AOUT+	Analog out, 0 phase
$\overline{IRQ}$/FT/OUT	Interrupt output for oscillator fail detect, frequency test output for calibration, or discrete logic output
V_{BACK}	Backup supply voltage
FBK	Feedback; connect feedback resistor between this pin and AIN
NC	No connection
No name; exposed pad on back of IC package	Must be connected to ground

3 Application

Figure 3. Application diagram

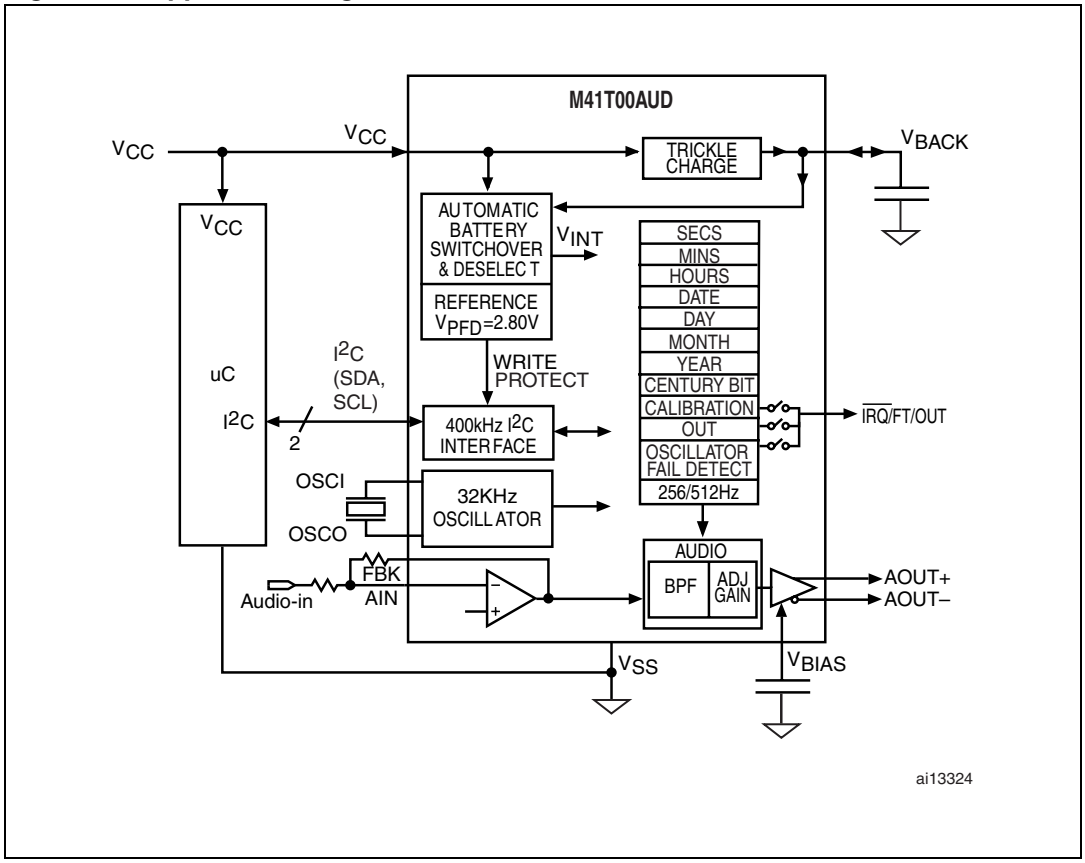
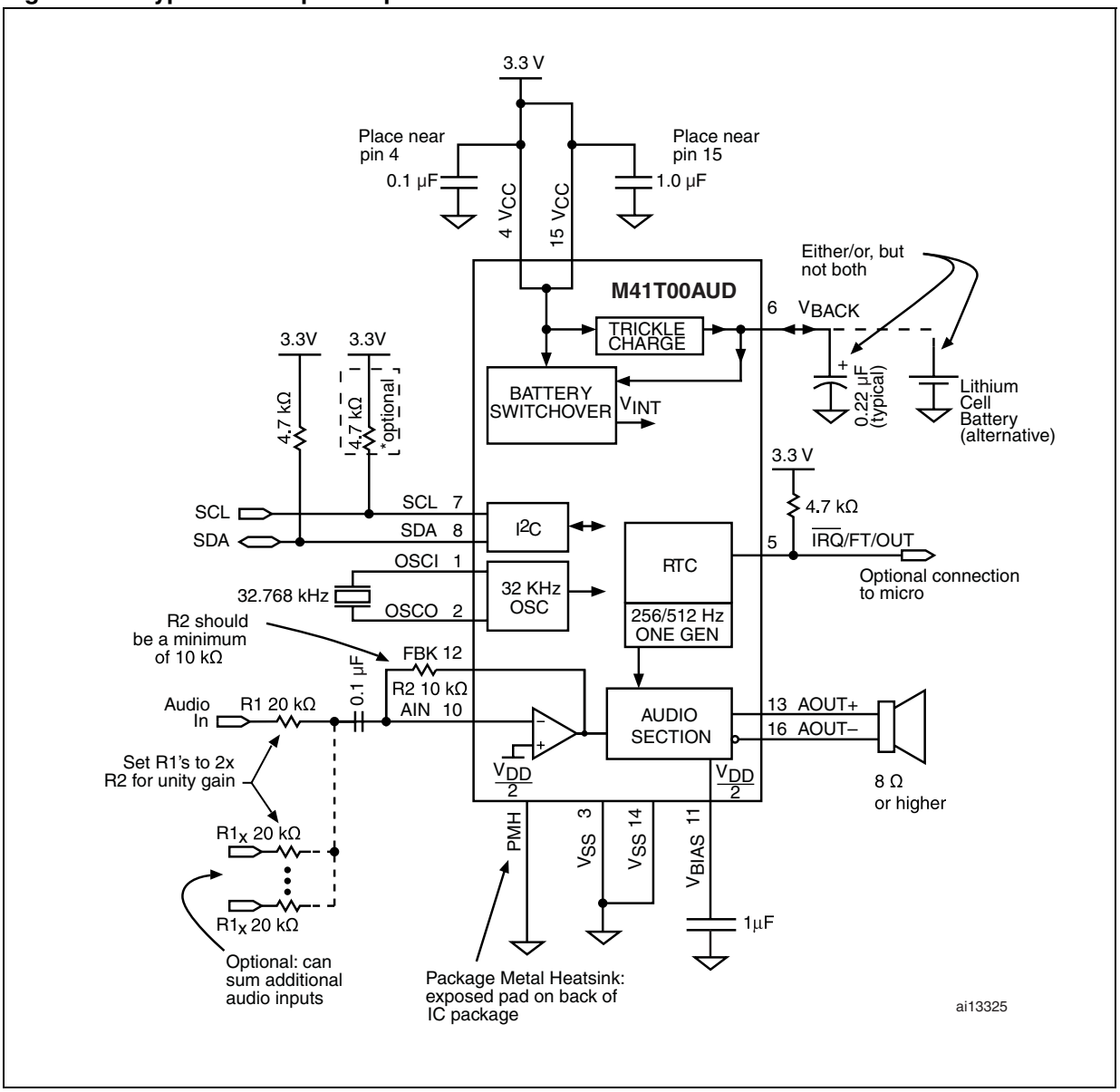


Figure 4. Typical hookup example



4 Operation

The M41T00AUD clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 10 bytes contained in the device can then be accessed sequentially in the following order:

Table 2. List of registers

Byte address	Contents
00h	Seconds register
01h	Minutes register
02h	Century/hours register
03h	Day register
04h	Date register
05h	Month register
06h	Years register
07h	Calibration/control register
08h	Audio register
09h	Control2 register

The M41T00AUD continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the backup battery or capacitor and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to V_{CC} at V_{SO} and recognizes inputs.

4.1 2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

- Bus not busy. Both data and clock lines remain high.
- Start data transfer. A change in the state of the data line, from high to low, while the clock is high, defines the START condition.
- Stop data transfer. A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.
- Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit. By definition, a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

- Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

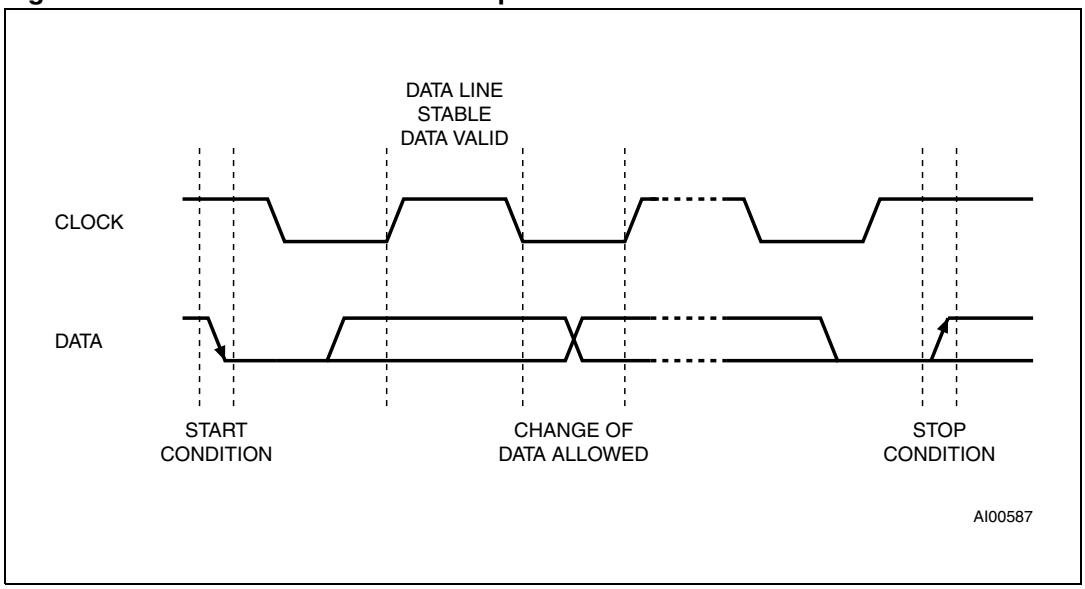


Figure 6. Acknowledgement sequence

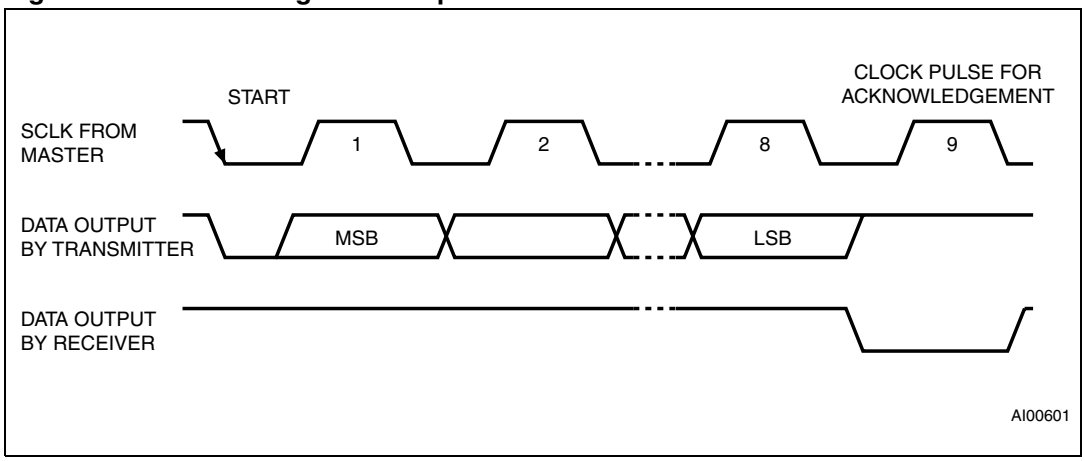
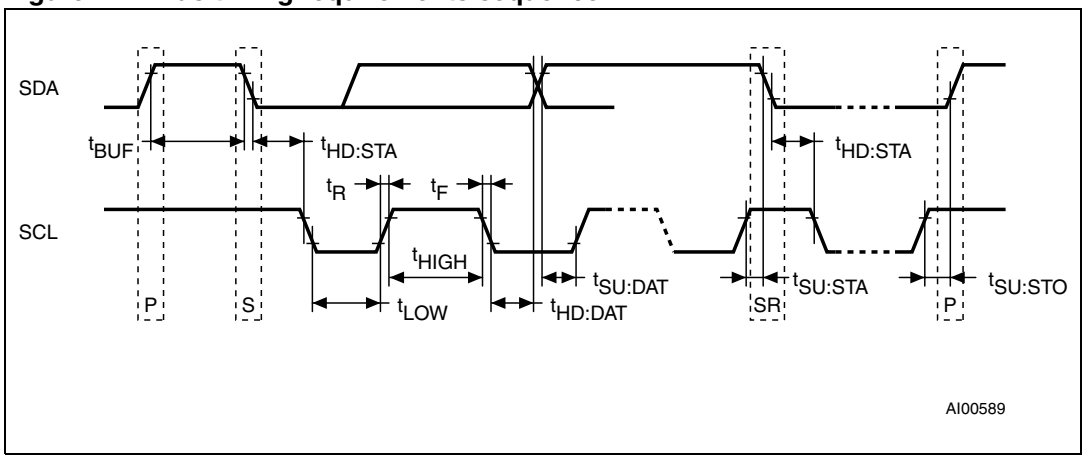


Figure 7. Bus timing requirements sequence



Note: P = STOP and S = START

4.2 Characteristics

Table 3. AC characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

4.3 READ mode

In this mode, the master reads the M41T00AUD slave after setting the slave address (see *Figure 8*). Following the WRITE mode control bit (R/W = 0) and the acknowledge bit, the word (register) address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The device slave transmitter will now place the data byte at address An+1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the M41T00AUD slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 10*).

Figure 8. Slave address location

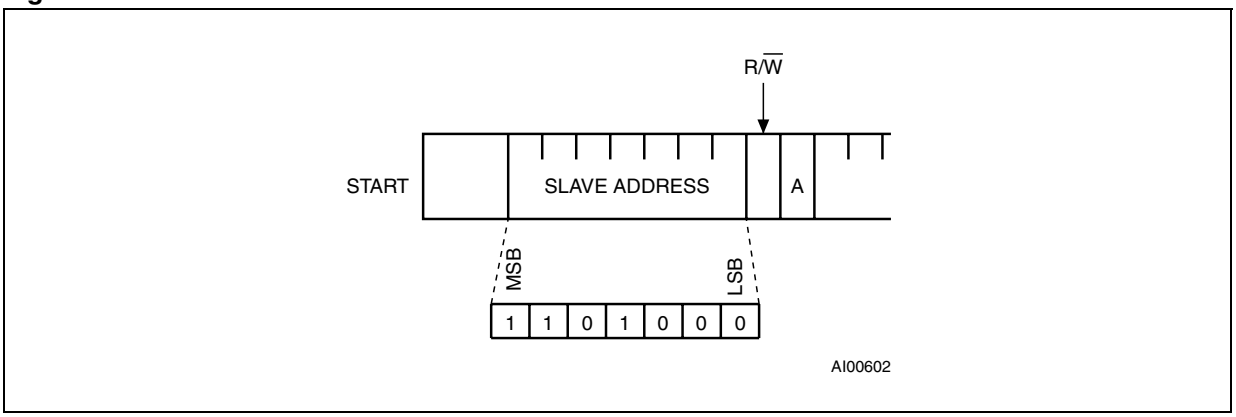


Figure 9. READ mode sequence

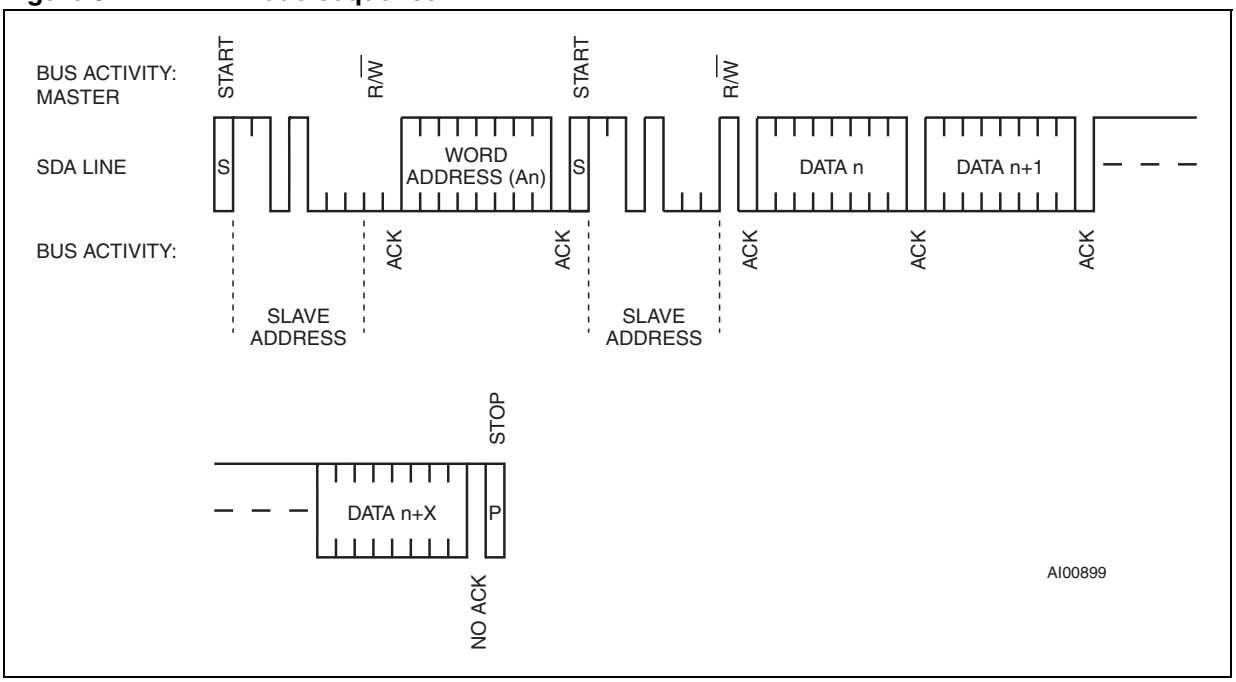
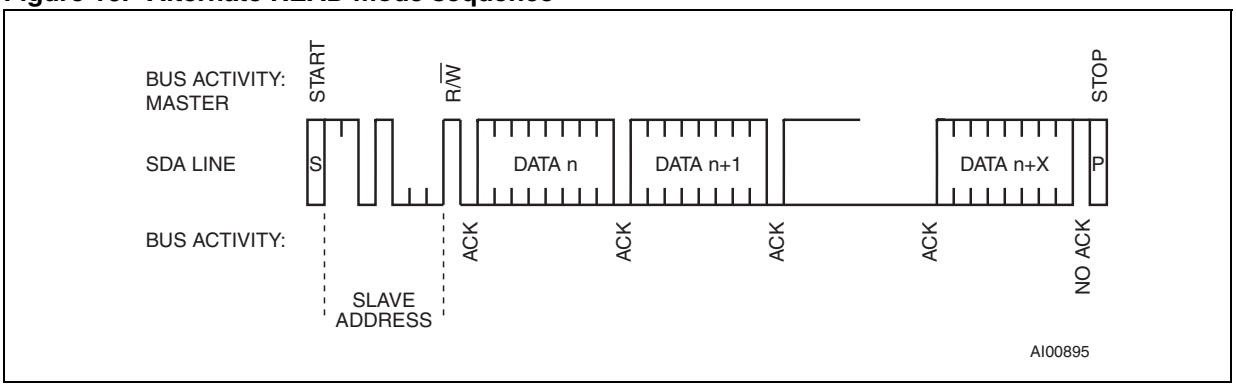


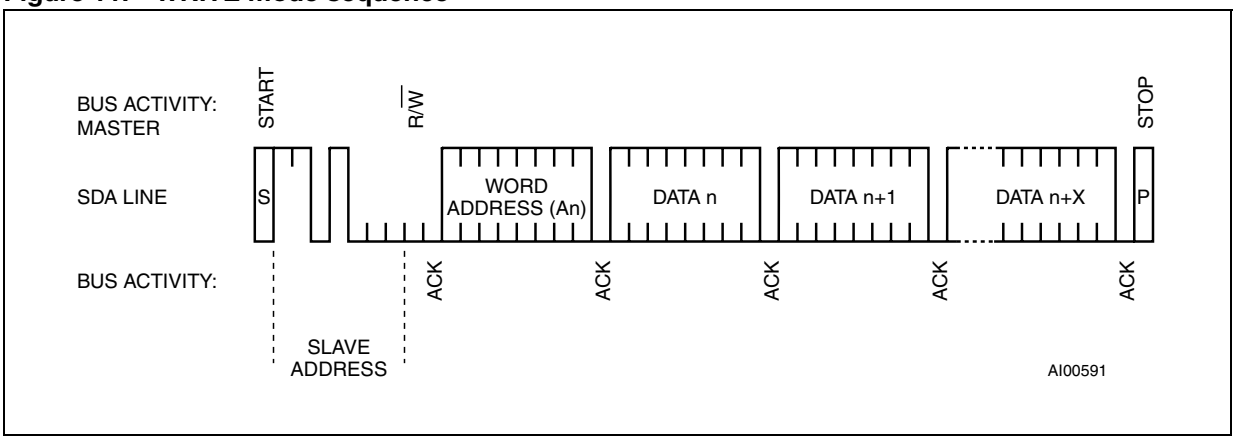
Figure 10. Alternate READ mode sequence



4.4 WRITE mode

In this mode the master transmitter transmits to the M41T00AUD slave receiver. Bus protocol is shown in *Figure 11*. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the device is strobed in next and the internal address pointer is incremented to the next location within the device on the reception of an acknowledge clock. The M41T00AUD slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see *Figure 8*).

Figure 11. WRITE mode sequence



4.5 Data retention mode

With valid V_{CC} applied, the M41T00AUD can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T00AUD will automatically deselect, write protecting itself when V_{CC} falls (see *Figure 13*).

5 M41T00AUD clock operation

5.1 Clock registers

The 10-byte register map (see *Table 2*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format.

Seconds, minutes, and hours are contained within the first three registers. Bits D6 to D0 or register 00h (seconds register) contain the seconds count in BCD format with values in the range 0 to 59. Bit D7 is the ST or stop bit, described below, and is not affected by the timekeeping operation, but users must avoid inadvertently altering it when writing the seconds register.

Setting the ST bit to a 1 will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain on the backup battery. When reset to a 0 the oscillator restarts within one second.

In order to ensure oscillator start-up after the initial power-up, set the ST bit to a 1 then write it to 0. This sequence enables the "kick start" circuit which aids the oscillator start-up by temporarily increasing the oscillator current. This will guarantee oscillator start-up under worst case conditions of voltage and temperature. This feature can be employed anytime the oscillator is being started but should not occur on subsequent power-ups when the oscillator is already running.

Bits D6 to D0 of register 01h (minutes register) contain the minutes count in BCD format with values in the range 0 to 59. Bit D7 always reads 0. Writing it has no effect.

Bits D5 to D0 of register 02h (century/ hours register) contain the hours in BCD format with values in the range 0 to 23. Bits D7 and D6 contain the century enable bit (CEB) and the century bit (CB). CB provides a one-bit indicator for the century. The user can apply his preferred convention for defining the meaning of this bit. For example, 0 can mean the current century, and 1 the next, or the opposite meanings may be used.

When enabled, CB will toggle every 100 years. Setting CEB to a 1 enables CB to toggle at the turn of the century, either from 0 to 1 or from 1 to 0, depending on its initial state, as programmed by the user. When CEB is a 0, CB will not toggle.

Bits D2 through D0 of register 03h (day register) contain the day of the week in BCD format with values in the range 0 to 7. Bits D3 and D7 will always read 0. Writes to them have no effect. Bits D6, D5 and D4 will power up in an indeterminate state.

Register 04h contains the date (day of month) in BCD format with values in the range 01 to 31. Bits D7 and D6 always read 0. Writes to them have no effect.

Register 05 h is the Month in BCD format with values in the range 1 to 12. Bits D7, D6 and D5 always read 0. Writes to them have no effect.

Register 06h is the years in BCD format with values in the range 0 to 99. Writing to any of the registers 00h to 06h, including the control bits therein, will result in updates to the counters and resetting of the internal clock divider chain including the 256/512 Hz tone generator. The updates do not occur immediately after the write(s), but occur upon completion of the current write access. This is described in greater detail in the next section.

Registers 07h and 09h also contain clock control and status information. These registers can be written at any time without affecting the timekeeping function.

Register 08 is the calibration register. Calibration is described in detail in the clock calibration section. Bit D7 is the OUT bit and controls the discrete output pin $\overline{IRQ}$/FT/OUT as described in *Table 5*.

5.1.1 Halt bit operation

Bit D7 of register 09 h is the HT or halt bit. Whenever the device switches to backup power, it sets the HT bit to 1 and stores the time of power-down in the transfer buffer registers. This is known as power-down time stamp. During normal timekeeping, once per second, the transfer buffer registers are updated with the current time. When HT is 1, that updating is halted. The clock continues to keep time but the periodic updates do not occur.

Upon power-up, reads of the clock registers will return the time of power-down (assuming adequate backup power was maintained while V_{CC} was off). After the user clears the HT bit by writing it to 0, subsequent reads of the clock registers will return the current time.

At power-up, the user can read the time of power-down, and then clear the HT bit to allow updates. The next read will return the current time. Knowing both the power-up time and the power-down time allows the user to calculate the duration of power-off.

In addition to the HT bit getting set to 1 automatically at power-down, the user can also write it to 1 to halt updating of the registers.

5.1.2 Oscillator fail detect operation

Bits D5 and D4 of register 09 h contain the oscillator fail flag (OF) and the oscillator fail interrupt enable bit (OFIE). If the 32 KHz oscillator drops four or more pulses in a row, as might occur during an extended outage while backed up on a capacitor, the OF bit will be set to 1. This provides an indication to the user of the integrity of the timekeeping operation. Whenever the OF bit is a 1, the system should consider the time to be possibly corrupted due to operating at too low a voltage. The OF bit will always be 1 at the initial power-up of the device. The OF bit is cleared by writing it to 0. At the initial power-up, users should wait three seconds for the oscillator to stabilize before clearing the OF bit.

OFIE can be used to enable the device to assert its interrupt output whenever an oscillator failure is detected. The oscillator fail interrupt will drive the $\overline{IRQ}$/FT/OUT pin as described in Table 5. The interrupt is cleared by writing the OF bit to 0. Setting OFIE enables the oscillator fail interrupt. Clearing it to 0 disables it, but the OF will continue to function regardless of OFIE.

5.1.3 Trickle charger

Bits D6 and D3 to D0, of register 09h, control the trickle charge function. It is described in detail in the trickle charge circuit section.

5.2 Reading and writing the clock registers

The counters used to implement the timing chain in the real-time clock are not directly accessed by the serial interface. Instead, as depicted in *Figure 12*, reads and writes are buffered through a set of transfer registers. This ensures coherency of the timekeeping function.

During writes of the timekeeping registers (00h to 06h), the write data is stored in the buffer transfer registers until all the data is written, then the register contents are simultaneously transferred to the counters thus updating them. The update is triggered either by a STOP condition or by a write to one of the non RTC registers, 07h to 09h. If any of the buffer transfer registers are not written, then the corresponding counters are not updated. Instead, those counters will retain their previous contents when the update occurs.

Similar to the writes, reads access the buffer transfer registers. The device periodically updates the registers with the counter contents. But during reads, the updates are suspended. Timekeeping continues, but the registers are frozen until after a STOP condition or a non RTC register (07h to 09h) is read. Suspending the updates ensures that a clock roll-over does not occur during a user read cycle.

The seven clock registers may be read one byte at a time, or in a sequential block. The calibration, audio and Control2 registers, location 07 h to 09 h, may be accessed independently.

Provision has been made to ensure that a clock update does not occur while any of the seven clock addresses are being read. During a clock register read (addresses 00h to 06h), updates of the clock transfer buffer registers are halted. The clock counters continue to keep time, but the contents of the transfer buffer registers is frozen at the time that the read access began.

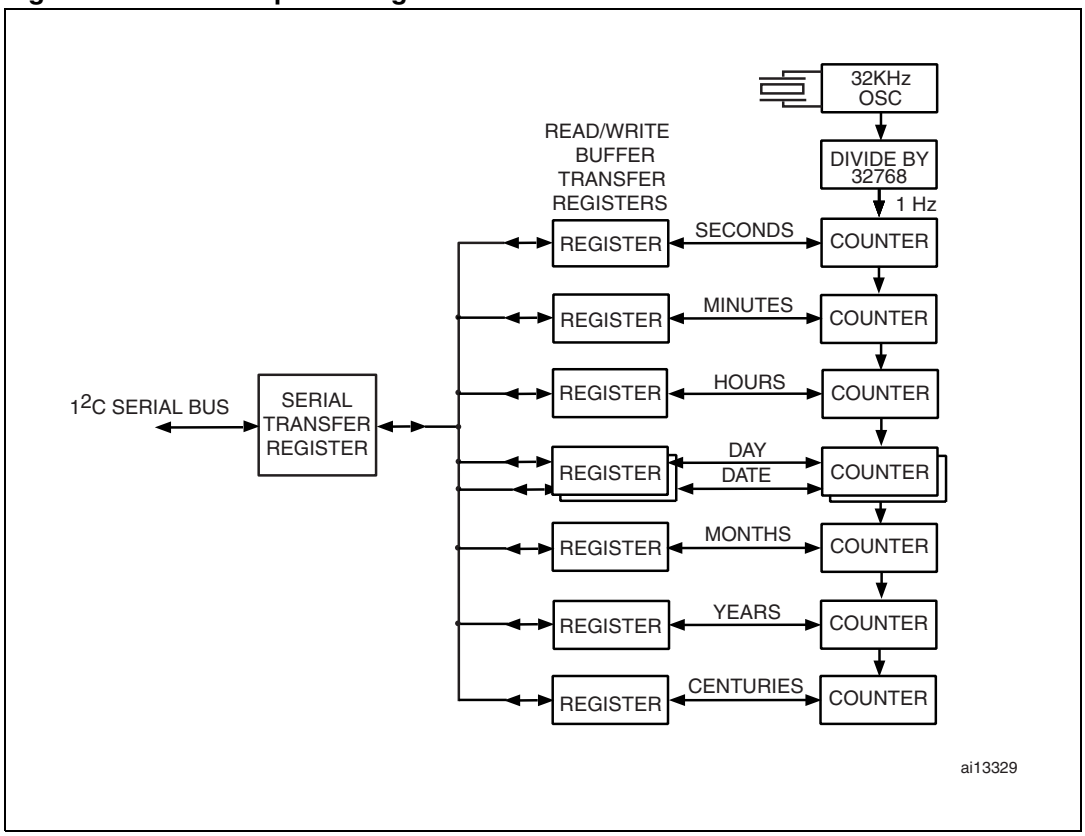
This prevents a transition of data during the READ. For example, without the halt function, if the time incremented past midnight in the middle of an access sequence, the user might begin reading at 11:59:59pm and finish at 12:00:00am. The data read might appear as 12:59:59 because the seconds and minutes were read before midnight while the hours were read after. The device prevents this by halting the updates of the registers until after the read access has occurred.

Table 4. M41T00AUD register map(1)

Addr	Bit								Register name	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	ST	10 seconds			Seconds				Seconds	00-59
01h	0(2)	10 minutes			Minutes				Minutes	00-59
02h	CEB	CB	10 hours		Hours (24 hour format)				Century/hours	0-1/00-23
03h	0	Y(3)	Y	Y	0	Day of week			Day	1-7
04h	0	0	10 date		Date: day of month				Date	01-31
05h	0	0	0	10M	Month				Month	01-12
06h	10 years				Year				Year	00-99
07h	OUT	FT	S	<---------- Calibration ---------->					Cal/control	
08h	256/512	TONE	TCH2	MUTE	<----------GAIN ---------->				Audio	
09h	HT	TCFE	OF	OFIE	TCHE3	TCHE2	TCHE1	TCHE0	Control2	

1. Key:
   S = SIGN bit
   FT = Frequency test bit
   ST = STOP bit
   OF = Oscillator fail detect flag
   OFIE = Oscillator fail interrupt enable
   OUT = Logic output
   TCHE3:TCHEO = Trickle charge enable bits
   TCFE = Trickle charge FET bypass enable
   HT = Halt bit
   TCH2 = Trickle charge enable #2
   TONE = Tone on/off select
   CB = Century bit
   CEB = Century enable bit
   256/512 = Tone frequency select bit
2. 0 bits always read as 0. Writing them has no effect.
3. Y bits are indeterminate at power-up. These are the factory test mode bits, and must be written to 0.

Figure 12. Counter update diagram



5.3 Priority for $\overline{IRQ}$/FT/OUT pin

Three functions share pin 5 of the M41T00AUD. The oscillator fail interrupt ($\overline{IRQ}$), the calibration frequency test output (FT) and the discrete logic output (OUT) all use this pin.

In normal operation, when operating from V_{CC}, the interrupt function has priority over the frequency test function which in turn has priority over the discrete output function.

In the backup mode, when operating from V_{BACK}, the priorities are different. The interrupt and frequency test functions are disabled, and only the discrete output function can be used.

When operating from V_{CC}, if the oscillator fail interrupt enable bit is set (OFIE, D4 of register 09h), the pin is an interrupt output which will be asserted anytime the OF bit (D5 of register 09h) goes true. (See *Section 5* for more details.)

During calibration, the pin can be used as a frequency test output. When FT is a 1 (and OFIE a 0), the device will output a 512 Hz test signal on this pin. Users can measure this with a frequency counter and use that result to determine the appropriate calibration register value.

Otherwise, when OFIE is a 0 and FT is a 0, it becomes the discrete logic OUT pin and reflects the value of the OUT bit (D7 of register 07h).

When operating from V_{BACK}, the discrete output function can still be used. The $\overline{IRQ}$/FT/OUT pin will reflect the contents of the out bit.

Note: The $\overline{IRQ}$/FT/OUT pin is open drain and requires an external pull-up resistor.

Table 5. Priority for $\overline{IRQ}$/FT/OUT pin

State	Register bits			$\overline{IRQ}$/FT/OUT pin
	OFIE	FT	OUT	
On V_{CC}	1	X	X	$\overline{OF}$
	0	1	X	512 Hertz
	0	0	1	1
	0	0	0	0
On V_{BACK}	X	X	1	1
	X	X	0	0

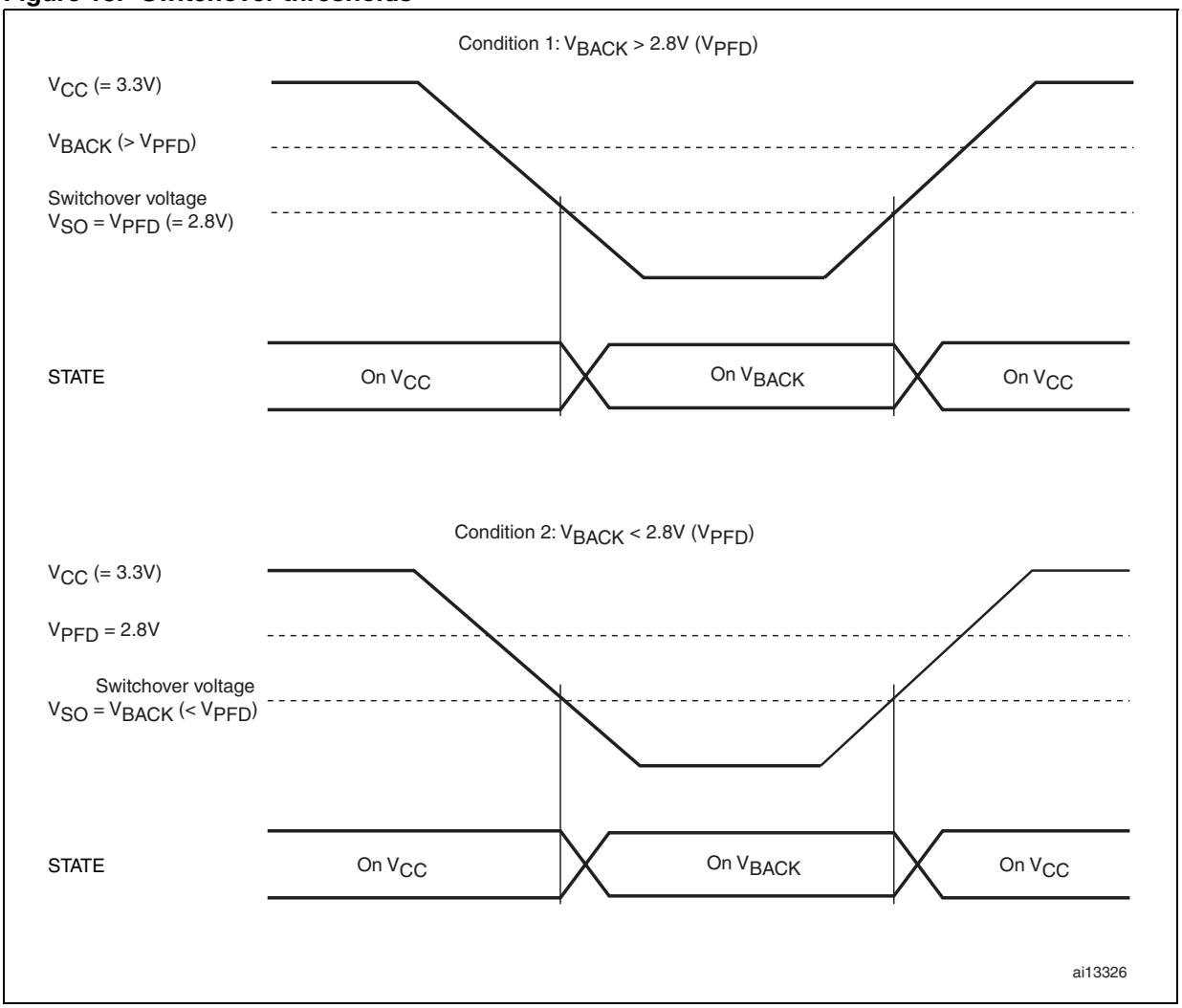
5.4 Switchover thresholds

While the M41T00AUD includes a precision reference for the backup switchover threshold, it is not a fixed value, but depends on the backup voltage, V_{BACK}. The device will always switchover at the lesser of the reference voltage (V_{PFD}, approximately 2.8 V) and V_{BACK}. This ensures that it stays on V_{CC} as long as possible before switching to the backup supply.

As shown in *Figure 13*, whenever V_{BACK} is greater than V_{PFD}, switchover occurs when V_{CC} drops below V_{PFD}.

Conversely, when V_{BACK} is less than V_{PFD}, switchover occurs when V_{CC} drops below V_{BACK}. *Table 14* provides the values of these voltages.

Figure 13. Switchover thresholds



5.5 Trickle charge circuit

The M41T00AUD includes a trickle charge circuit to be used with a backup capacitor. It is illustrated in *Figure 14*. V_{BACK} is a bi-directional pin. Its primary function is as the backup supply input. (The input nature is not depicted in the figure.) The trickle charge output function is a secondary capability, and reduces the need for external components.

To enable trickle charging, two switches must be closed. A diode is present to prevent current from flowing backwards from V_{BACK} to V_{CC}. A current limiting resistor is also in the path.

An additional switch allows the diode to be bypassed through a 20 k resistor. This should charge the capacitor to a higher level thus extending backup life. This switch automatically opens when the device switches to backup thus preventing capacitor discharge to V_{CC}.

Furthermore, at switchover to backup, the other switches open as well. The application must close them after power-up to re-enable the trickle charge function.

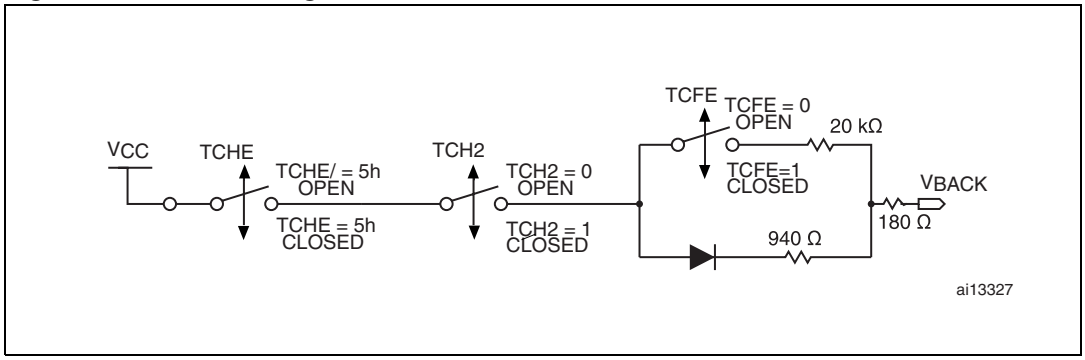
The use of two switches in the chain is to protect against accidental, unwanted charging as might be the case when using battery backup. Additionally, one of the two switches requires four bits to be changed from the default value before it will close. This prevents single bit errors from closing the switch. The four bits, TCHE3:TCHE0, reside in register 09h at bits D3 to D0.

The control bit for the second switch, TCH2, resides in register 08h at bit D5. With this bit in a separate register, two bytes must be written before charging will occur, again protecting against inadvertent charging due to errors.

The control bit for the bypass switch, TCFE, resides in register 09h at bit D6.

To enable trickle charging, the user must set TCHE3:TCHE0 to 5h, and TCH2 to 1. To bypass the diode, TCFE must be set to 1. All three fields must be enabled after each power-up.

Figure 14. Trickle charge circuit



6 Clock calibration

The M41T00AUD oscillator is designed for use with a 12.5 pF crystal load capacitance. With a nominal ±20 ppm crystal, the M41T00AUD will be accurate to ±35 ppm. When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25 °C.

The M41T00AUD design provides the following method for clock error correction.

6.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the number of cycles of the internal 512 Hz signal counted in a second. By adding an extra cycle, for 513, a long second is counted for slowing the clock. By reducing it to 511 cycles, a short second is counted for speeding up the clock.

Not every second is affected. The calibration value (bits D4-D0 of register 07h) and its sign bit (D5 of same register) control how often a short or long second is generated.

The basic nature of a 32 KHz crystal is to slow down at temperatures above and below 25 °C. Whether the temperature is above or below 25 °C, the device will tend to run slow. Therefore, most corrections will need to speed the clock up. Hence, the M41T00AUD calibration circuit uses a non-symmetric calibration scheme. Positive values, for speeding the clock up, have more effect than negative values, for slowing it down. A positive value will speed the clock up by approximately 4 ppm per step. A negative value will slow it by approximately 2 ppm per step.

In the M41T00AUD's calibration circuit, positive correction is applied every 8^{th} minute whereas negative correction is applied every 16^{th} minute. Because positive correction is applied twice as often, it has twice the effect for a given calibration number, N. When the calibration sign bit is positive, N seconds of every 8^{th} minute will be shortened to 511 cycles of the 512 Hz clock. When the calibration sign bit is negative, N seconds of every 16^{th} minute will be lengthened to 513 cycles of the 512 Hz clock.

When N is positive, one minute will have N seconds which are 511 cycles and the remaining seconds will be 512 cycles. The next seven minutes are nominal with all seconds 512 cycles each.

Example 1:

Sign is 1 and N is 2 (00010b)

The 8-minute interval will be:

2 * 511 + (60-2) * 512 + 7 * 60 * 512 = 245758 cycles long out of a possible

512 * 60 * 8 = 245760 cycles of the 512 Hz clock in an 8-minute span.

This gives a net correction of (245760-245758) / 245760 = -8.138 ppm

When N is negative, one minute will have N seconds which are 513 cycles and the remaining seconds will be 512 cycles. The next 15 minutes are nominal with all seconds 512 cycles each.

Example 2:

Sign is 0 and N is 3 (00010b). The 16-minute interval will be:

3 * 513 + (60-3) * 512 + 15 * 60 * 512 = 491523 cycles long out of a possible

512 * 60 * 16 = 491520 cycles of the 512 Hz clock in an 16-minute span.

This gives a net correction of (491520-491523) / 491520 = +6.104 ppm

Therefore, each calibration step has an effect on clock accuracy of either -4.068 or +2.034 ppm. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 steps in the calibration byte would represent subtracting 10.7 or adding 5.35 seconds per month, which corresponds to a total range of –5.5 or +2.75 minutes per month.

Note: The modified pulses are not observable on the frequency test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.