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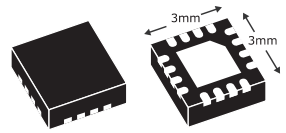
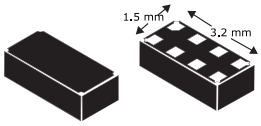
M41T62, M41T64, M41T65

Low-power serial real-time clocks (RTCs) with alarm

Datasheet - production data



QFN16 3 x 3 mm



Embedded crystal LCC8 1.5 x 3.2 mm
No external crystal required

Features

- Serial real-time clock (RTC) with alarm functions
  - 400 kHz I^2C serial interface
  - Memory mapped registers for seconds, minutes, hours, day, date, month, year, and century
  - Tenths/hundredths of seconds register
- 350 nA timekeeping current at 3 V
- Timekeeping down to 1.0 V
- 1.3 V to 4.4 V I^2C bus operating voltage
  - 4.4 V max V_{CC} suitable for lithium-ion battery operation
- Low operating current of 35 µA (at 400 kHz I^2C speed)
- 32 KHz square wave output is on at power-up. Suitable for driving a microcontroller in low-power mode. Can be disabled. (M41T62/64)
- Programmable 1 Hz to 32 KHz square wave output (M41T62/64)
- Programmable alarm with interrupt function (M41T62/65)
- 32 KHz crystal oscillator integrates crystal load capacitors, works with high series resistance crystals
- Oscillator stop detection monitors clock operation
- Accurate programmable watchdog
  - 62.5 ms to 31 min timeout
- Software clock calibration. Can adjust timekeeping to within ±2 parts per million (±5 seconds per month)
- Automatic leap year compensation
- –40 to +85 °C operation
- Two package options
  - Very small 3 x 3 mm, lead-free & halogen-free (ECOPACK2®) 16-lead QFN
  - Ultra-small 1.5 x 3.2 mm, lead-free & halogen-free (ECOPACK2®) 8-pin ceramic leadless chip carrier with embedded 32 KHz crystal - no external oscillator components required (M41T62)

Contents

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1 Description

The M41T6x is a low-power serial real-time clock (RTC) with a built-in 32.768 kHz oscillator. Eight registers are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. An additional eight registers provide status/control of alarm, 32 KHz output, calibration, and watchdog functions. Addresses and data are transferred serially via a two-line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

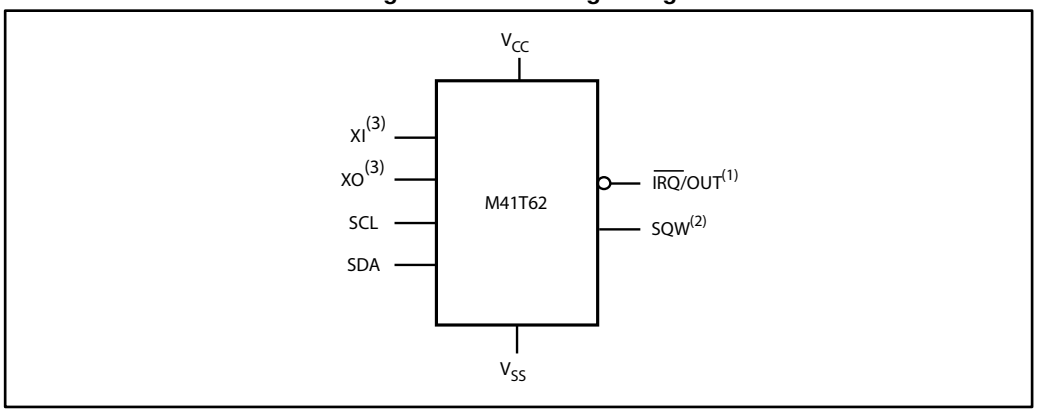
Functions available to the user include a time-of-day clock/calendar, alarm interrupts (M41T62/65), 32 KHz output (M41T62/64), programmable square wave output (M41T62/64), and watchdog output (M41T65). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28-, 29- (leap year), 30- and 31-day months are made automatically.

The M41T6x is supplied in two very small packages: a tiny, 3 x 3 mm 16-pin QFN which requires a user-supplied 32 KHz crystal, and an ultra-small 1.5 x 3.2 mm LCC with embedded crystal - no external crystal is required.

Table 1: Device summary

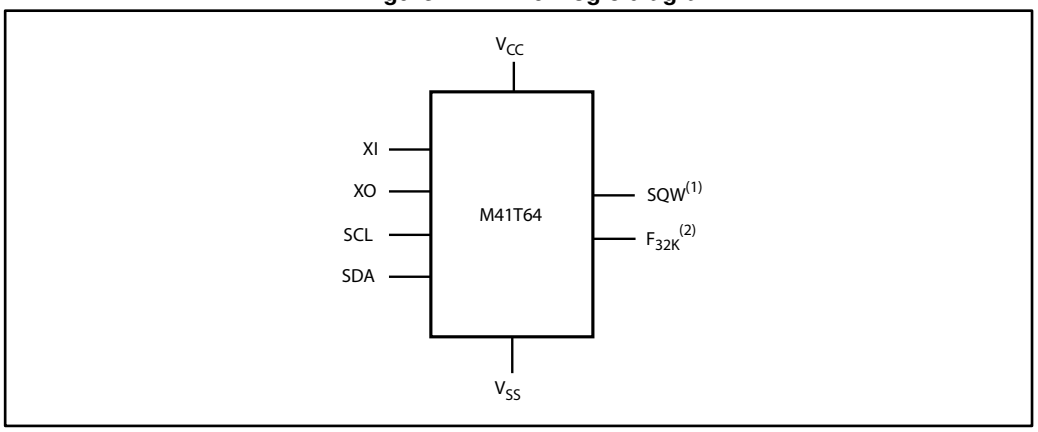
Device	Basic RTC	Alarms	OSC fail detect	Watchdog timer	Calibration	SQW output	$\overline{IRQ}$ output	$\overline{WDO}$ output	F_{32K} output
M41T62	✓	✓	✓	✓	✓	✓	✓		
M41T64	✓	✓	✓	✓	✓	✓			✓
M41T65	✓	✓	✓	✓	✓		✓	✓	

Figure 1: M41T62 logic diagram



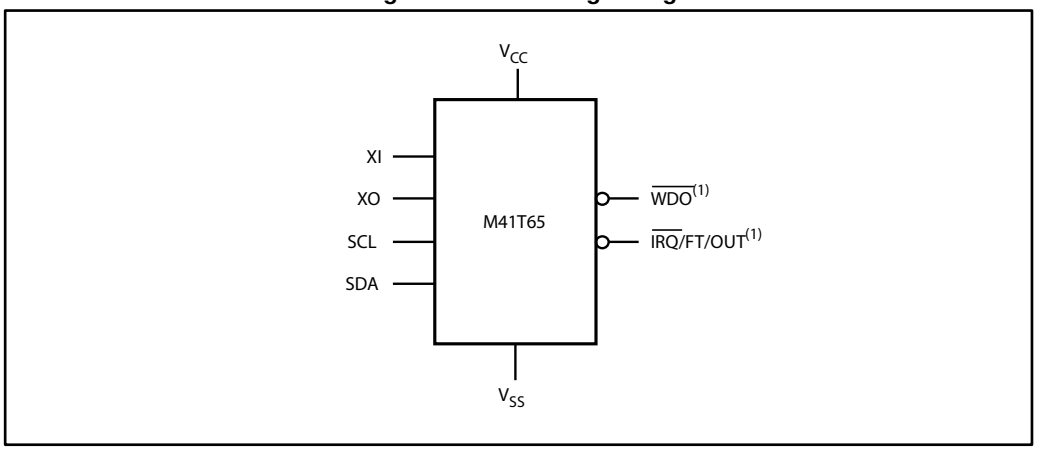
1. Open drain.
2. Defaults to 32 KHz on power-up.
3. Not bonded on LCC package.

Figure 2: M41T64 logic diagram



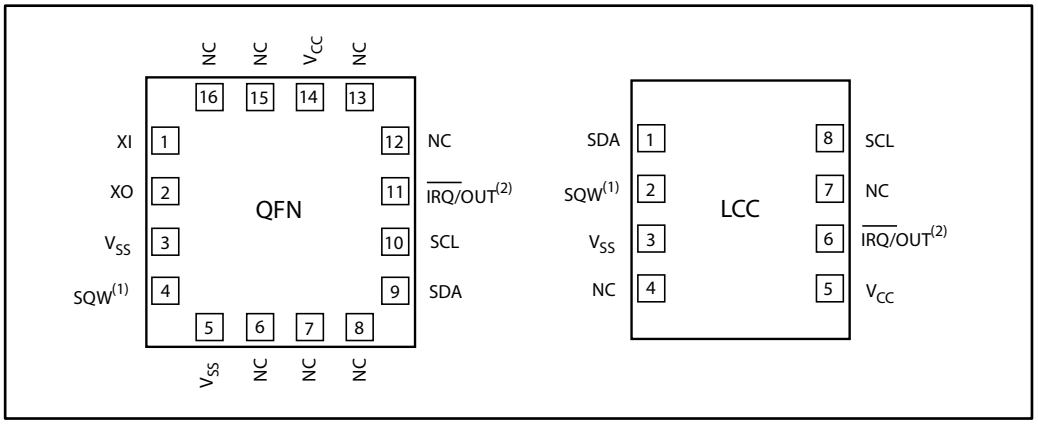
1. Open drain.
2. Defaults to 32 KHz on power-up.

Figure 3: M41T65 logic diagram



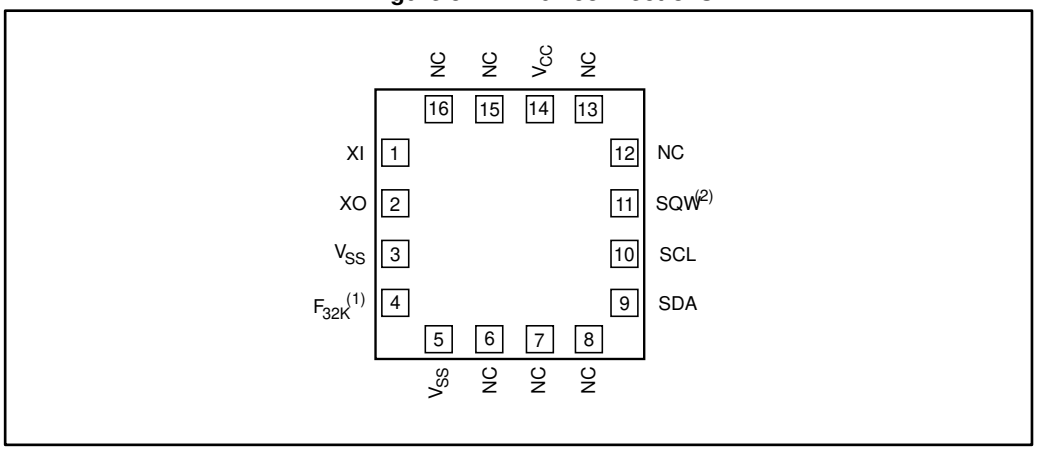
1. Open drain.

Figure 4: M41T62 connections



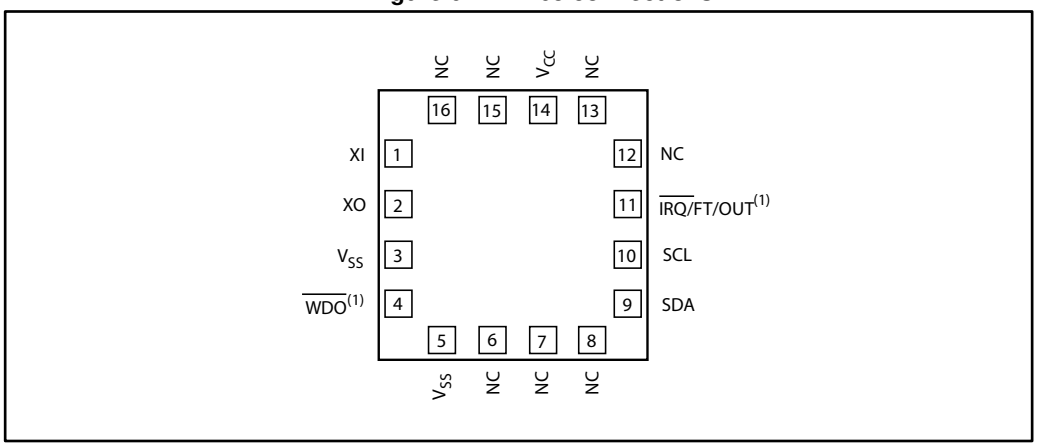
1. SQW output defaults to 32 KHz upon power-up.
2. Open drain.

Figure 5: M41T64 connections



1. Enabled on power-up.
2. Open drain.

Figure 6: M41T65 connections

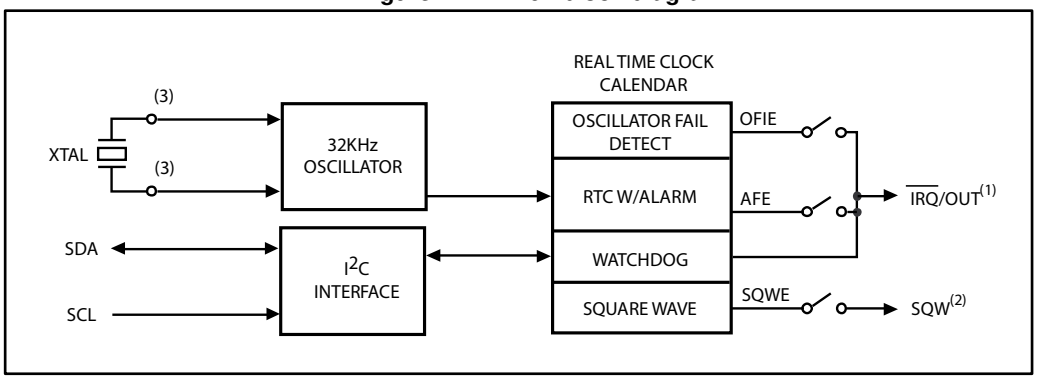


1. Open drain.

Table 2: Signal names

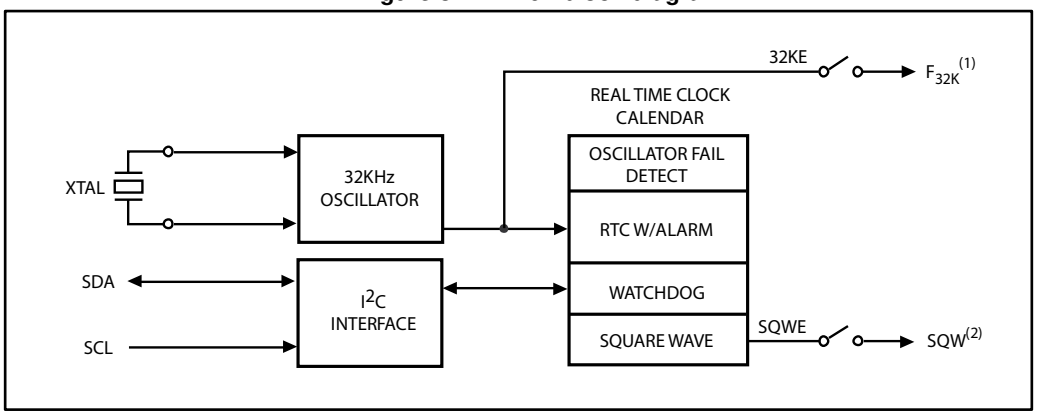
XI	Oscillator input
XO	Oscillator output
SDA	Serial data input/output
SCL	Serial clock input
$\overline{IRQ}$/OUT	Interrupt or OUT output (open drain)
$\overline{IRQ}$/FT/OUT	Interrupt, frequency test, or OUT output (open drain)
SQW	Programmable square wave - defaults to 32 KHz on power-up (open drain for M41T64 only)
F_{32K}	Dedicated 32 KHz output (M41T64 only)
$\overline{WDO}$	Watchdog timer output (open drain)
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 7: M41T62 block diagram



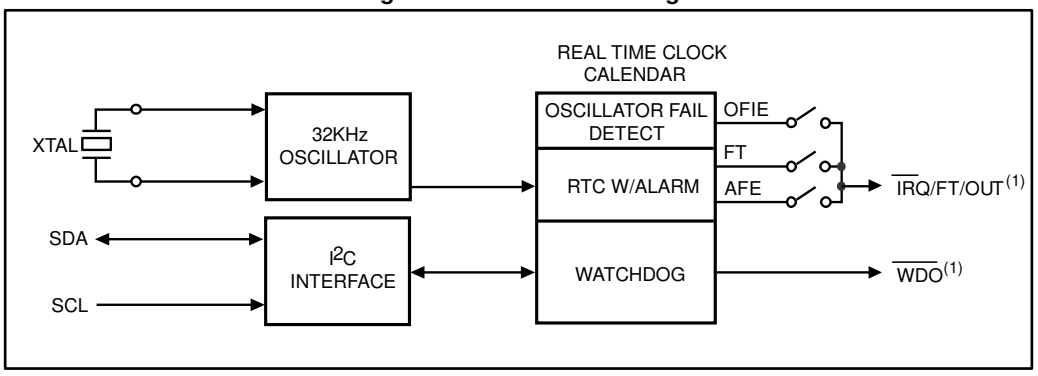
1. Open drain.
2. Defaults to 32 KHz on power-up.
3. Not bonded on embedded crystal (LCC) package.

Figure 8: M41T64 block diagram



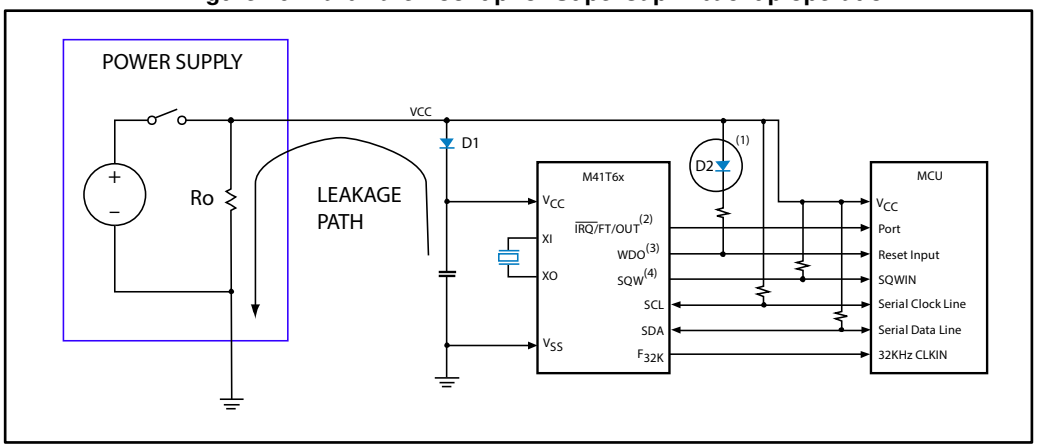
1. Defaults enabled on power-up.
2. Open drain.

Figure 9: M41T65 block diagram



1. Open drain.

Figure 10: Hardware hookup for SuperCap™ backup operation



1. Diode D2 required on open drain pin (M41T65 only) when using SuperCap (or battery) backup. Low threshold BAT42 schottky diode recommended (see note below). D1 and D2 should be of the same type.
2. For M41T62 and M41T65 (open drain).
3. For M41T65 (open drain).
4. For M41T64 (open drain).

Note: Some power supplies, when shut off, can present a leakage path to ground which will shorten the backup time provided by the SuperCap (or battery). In such cases, a very low leakage diode is recommended for D1 (and D2). A non-schottky such as the 1N4148 will have very low reverse leakage.

2 Operation

The M41T6x clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 16 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: hours register
- 5th byte: square wave/day register
- 6th byte: date register
- 7th byte: century/month register
- 8th byte: year register
- 9th byte: calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm registers
- 16th byte: flags register

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined.

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 11: Serial bus data transfer sequence

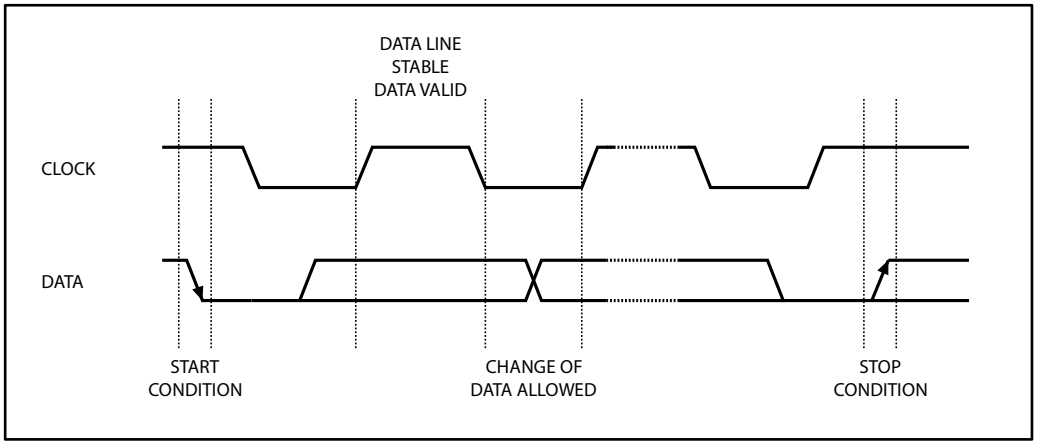
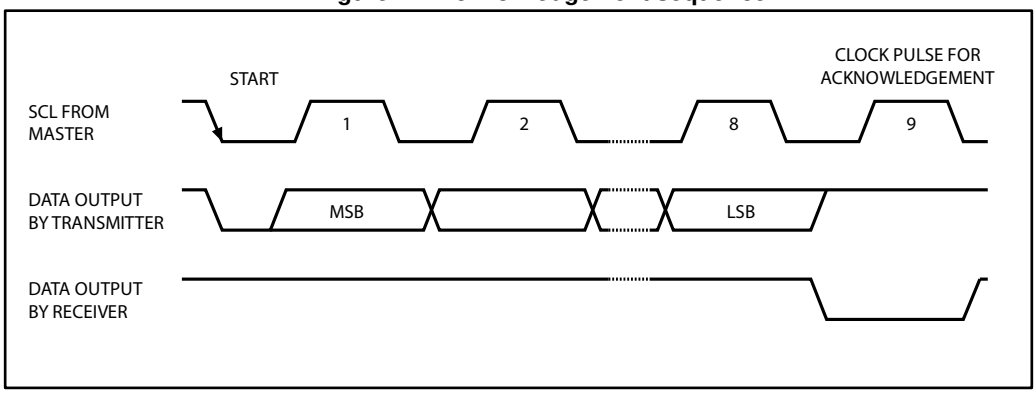


Figure 12: Acknowledgement sequence



2.2 READ mode

In this mode the master reads the M41T6x slave after setting the slave address (see *Figure 14: "READ mode sequence"*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. the address pointer is only incremented on reception of an acknowledge clock. The M41T6x slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (08h-0Fh).

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41T6x slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 15: "Alternative READ mode sequence"*).

Figure 13: Slave address location

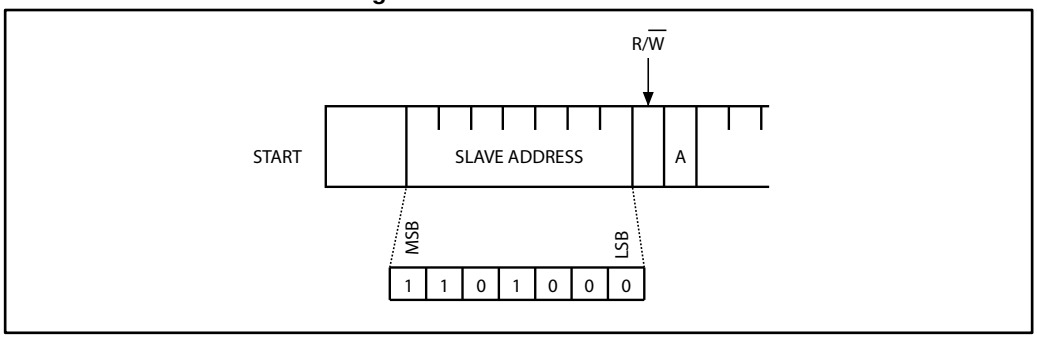


Figure 14: READ mode sequence

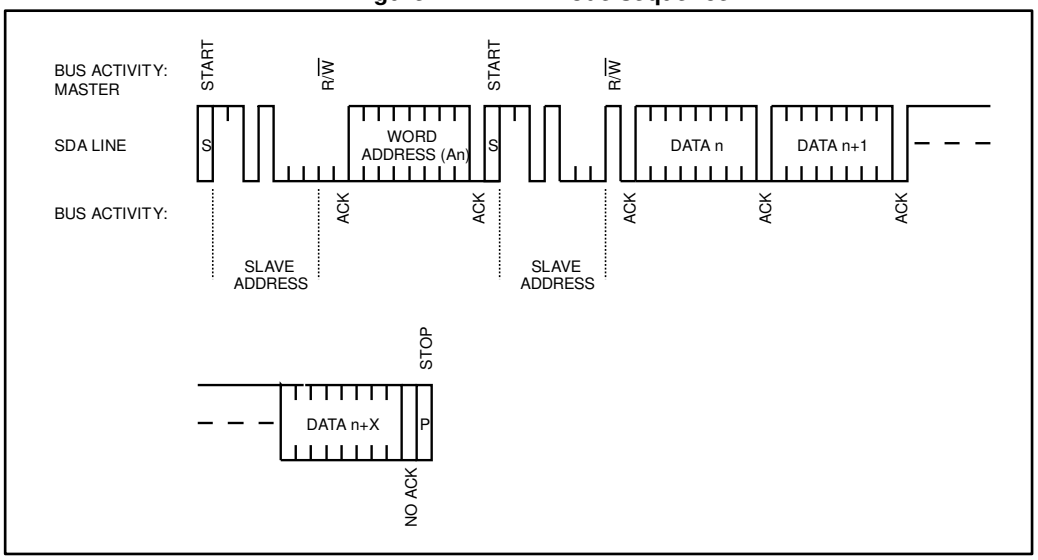
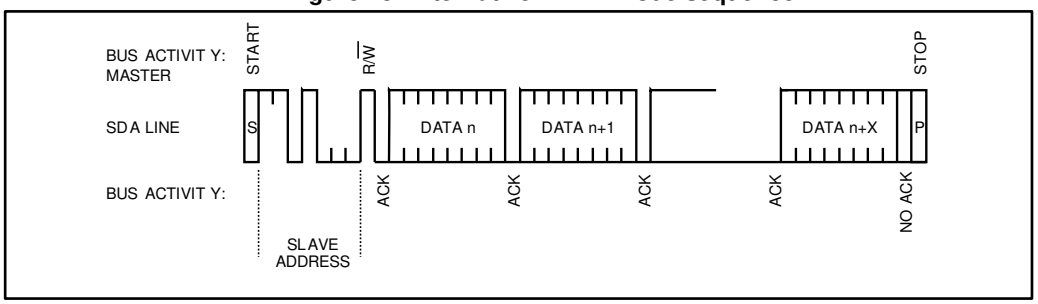


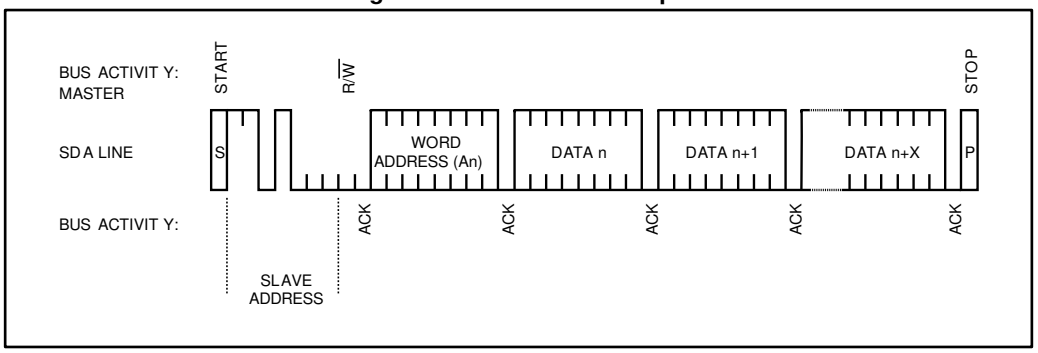
Figure 15: Alternative READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41T6x slave receiver. Bus protocol is shown in *Figure 16: "WRITE mode sequence"*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T6x slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see *Figure 13: "Slave address location"* and again after it has received the word address and each data byte.

Figure 16: WRITE mode sequence



3 Clock operation

The M41T6x is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The eight byte clock register (see *Table 3: "M41T62 register map"*, *Table 4: "M41T64 register map"*, and *Table 5: "M41T65 register map"*) is used to both set the clock and to read the date and time from the clock, in a binary-coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to “00,” and tenths/hundredths of seconds cannot be written to any value other than “00.”

Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional “kick-start” to the oscillator circuit.

Bit D7 of register 02h (minute register) contains the oscillator fail interrupt enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the oscillator fail bit (OF) (see *Section 3.11: "Oscillator stop detection"*) will also generate an interrupt output.

Bits D6 and D7 of clock register 06h (century/month register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1).

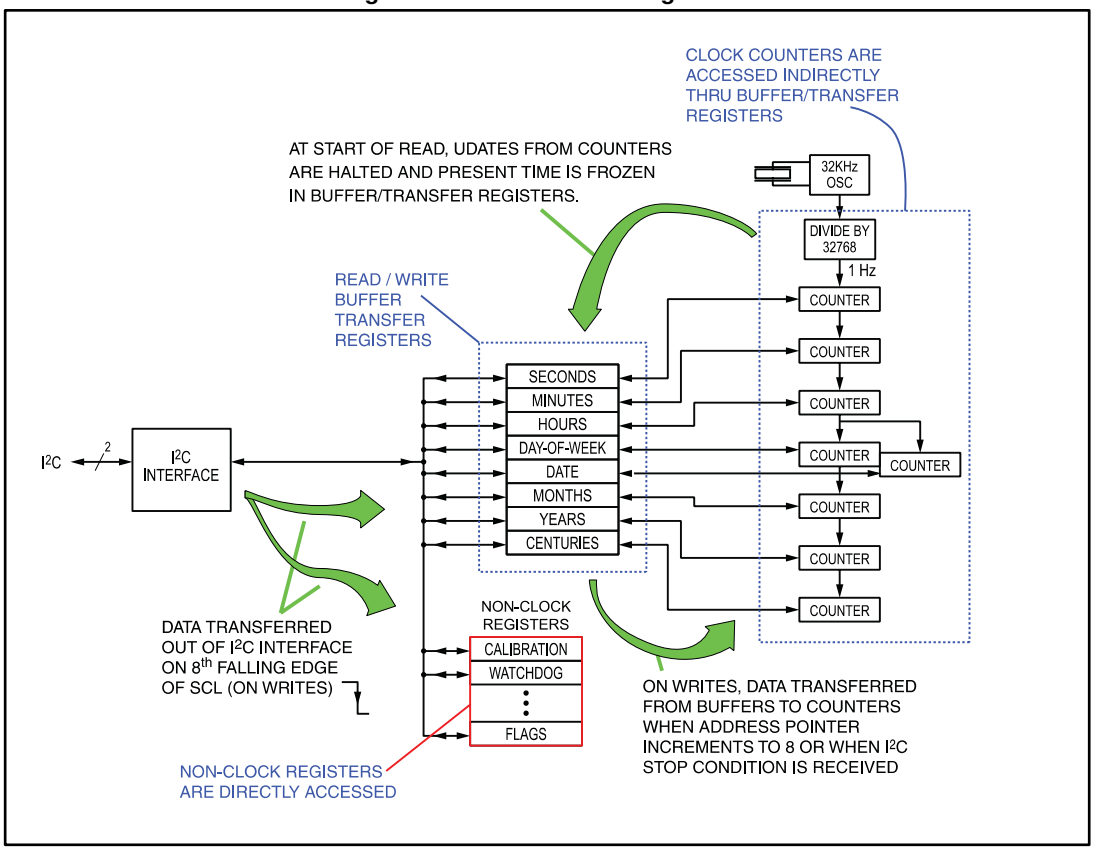
A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the OFIE bit, RS0-RS3 bit, and CB0-CB1 bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 RTC registers

The M41T6x user interface is comprised of 16 memory mapped registers which include clock, calibration, alarm, watchdog, flags, and square wave control. The eight clock counters are accessed indirectly via a set of buffer/transfer registers while the other eight registers are directly accessed. Data in the clock and alarm registers is in BCD format.

Figure 17: Buffer/transfer registers



Updates

During normal operation when the user is not accessing the device, the buffer/transfer registers are kept updated with a copy of the RTC counters. At the start of an I^2C read or write cycle, the updating is halted and the present time is frozen in the buffer/transfer registers.

Reads of the clock registers

By halting the updates at the start of an I^2C access, the user is ensured that all the data transferred out during a read sequence comes from the same instant in time.

Write timing

When writing to the device, the data is shifted into the M41T62's I^2C interface on the rising edge of the SCL signal. As shown in *Figure 17: "Buffer/transfer registers"*, on the 8th clock cycle, the data is transferred from the I^2C block into whichever register is being pointed to by the address pointer (not shown).

Writes to the clock registers (addresses 0-7)

Data written to the clock registers (addresses 0-7) is held in the buffer registers until the address pointer increments to 8, or an I^2C stop condition occurs, at which time the data in the buffer/registers is simultaneously copied into the counters, and then the clock is re-started.

Table 3: M41T62 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	RS3	RS2	RS1	RS0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	OUT	0	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	0	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:

0 = must be set to '0'

AF = alarm flag (read only)

AFE = alarm flag enable flag

BMB0 - BMB4 = watchdog multiplier bits

CB0-CB1 = century bits

OF = oscillator fail bit

OFIE = oscillator fail interrupt enable bit

OUT = output level

RB0 - RB2 = watchdog resolution bits

RPT1-RPT5 = alarm repeat mode bits

RS0-RS3 = SQW frequency bits

S = sign bit

SQWE = square wave enable bit

ST = stop bit

WDF = watchdog flag bit (read only)

Table 4: M41T64 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	RS3	RS2	RS1	RS0	0	Day of week			Day	01-7
05h	0	0	10 Date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	0	0	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	0	SQWE	32KE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:

0 = must be set to '0'

32KE = 32 KHz enable bit

AF = alarm flag (read only)

BMB0 - BMB4 = watchdog multiplier bits

CB0-CB1 = century bits

OF = oscillator fail bit

RB0 - RB2 = watchdog resolution bits

RPT1-RPT5 = alarm repeat mode bits

RS0-RS3 = SQW frequency bits

S = sign bit

SQWE = square wave enable bit

ST = stop bit

WDF = watchdog flag bit (read only)

Table 5: M41T65 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	0	0	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:

0 = must be set to '0'

AF = alarm flag (read only)

AFE = alarm flag enable flag

BMB0 - BMB4 = watchdog multiplier bits

CB0-CB1 = century bits

FT = frequency test bit

OF = oscillator fail bit

OFIE = oscillator fail interrupt enable bit

OUT = output level

RB0 - RB2 = watchdog resolution bits

RPT1-RPT5 = alarm repeat mode bits

S = sign bit

ST = stop bit

WDF = watchdog flag bit (read only)

3.2 Calibrating the clock

The M41T6x real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. This provides the time-base for the RTC. The accuracy of the clock depends on the frequency accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. The M41T6x oscillator is designed for use with a 6 - 7 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25 °C.

The oscillation rate of crystals changes with temperature (see *Figure 18: "Crystal accuracy across temperature"*). Therefore, the M41T6x design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 19: "Calibration waveform"*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per day which corresponds to a total range of +5.5 or –2.75 minutes per month (see *Figure 19: "Calibration waveform"*).

Two methods are available for ascertaining how much calibration a given M41T6x may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.
- The second approach is better suited to a manufacturing environment, and involves the use of either the SQW pin (M41T62/64) or the $\overline{\text{IRQ}}$/FT/OUT pin (M41T65). The SQW pin will toggle at 512 Hz when RS3 = '0,' RS2 = '1,' RS1 = '1,' RS0 = '0,' SQWE = '1,' and ST = '0.' Alternatively, for the M41T65, the $\overline{\text{IRQ}}$/FT/OUT pin will toggle at 512 Hz when FT and OUT bits = '1' and ST = '0.'

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test or square wave output frequency.

Figure 18: Crystal accuracy across temperature

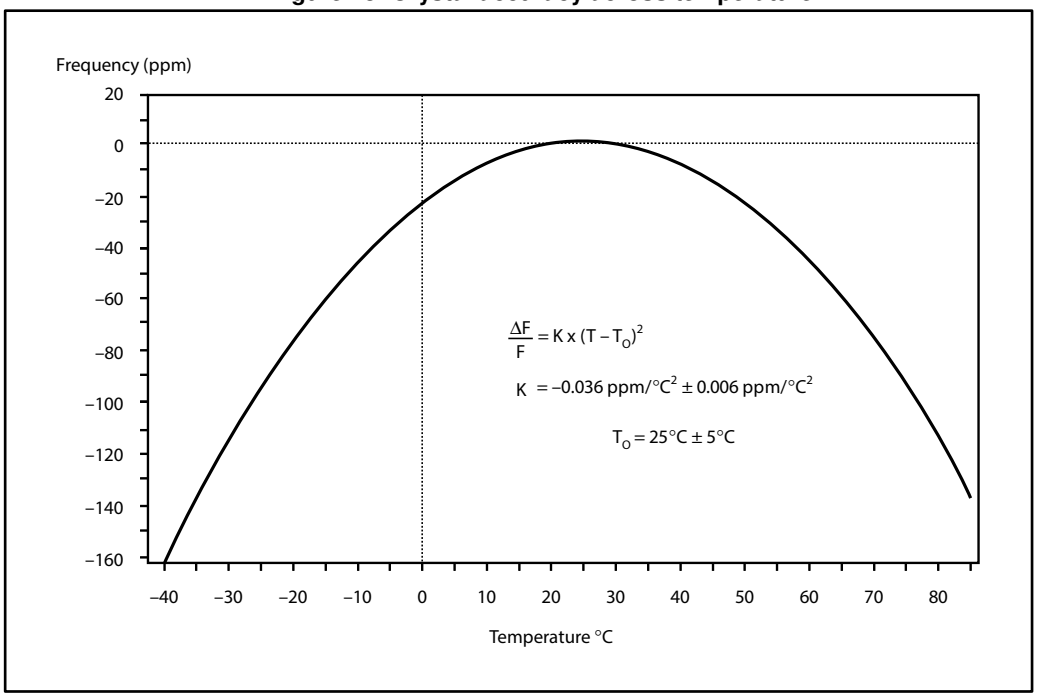
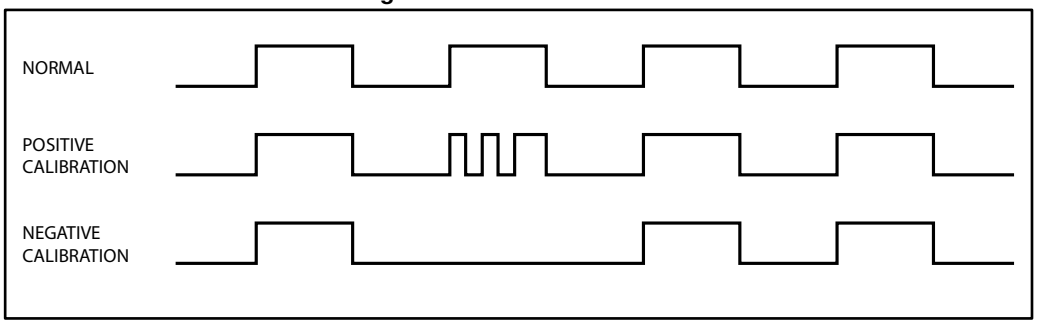


Figure 19: Calibration waveform



3.3 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT5–RPT1 put the alarm in the repeat mode of operation. *Table 6: "Alarm repeat modes"* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set (M41T62/65), the alarm condition activates the $\overline{IRQ}$/OUT or $\overline{IRQ}$/FT/OUT pin. To disable the alarm, write '0' to the alarm date register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{IRQ}$ output is cleared by a READ to the flags register as shown in *Figure 20: "Alarm interrupt reset waveform"*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

Figure 20: Alarm interrupt reset waveform

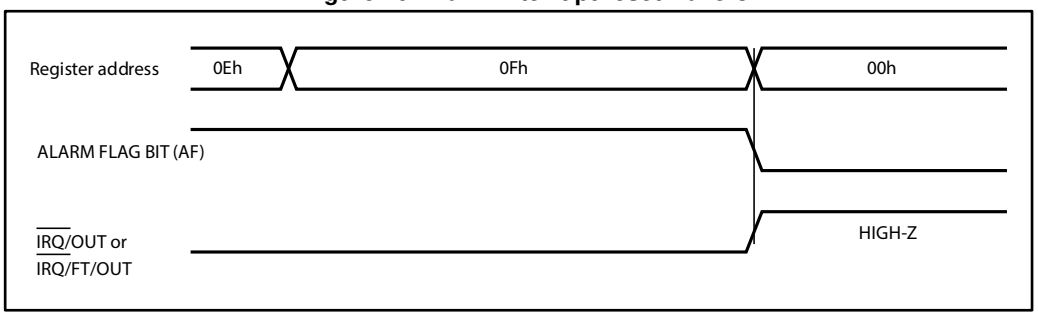


Table 6: Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.4 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h.

Bits BMB4-BMB0 store a binary multiplier and the three bits RB2-RB0 select the resolution where:

000=1/16 second (16 Hz);

001=1/4 second (4 Hz);

010=1 second (1 Hz);

011=4 seconds (1/4 Hz); and

100 = 1 minute (1/60 Hz).

Note: Invalid combinations (101, 110, and 111) will NOT enable a watchdog time-out. Setting BMB4-BMB0 = 00000 with any combination of RB2-RB0, other than 000, will result in an immediate watchdog time-out.

The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds). If the processor does not reset the timer within the specified period, the M41T6x sets the WDF (watchdog flag) and generates an interrupt on the $\overline{\text{IRQ}}$ pin (M41T62), or a watchdog output pulse (M41T65 only) on the $\overline{\text{WDO}}$ pin. The watchdog timer can only be reset by having the microprocessor perform a WRITE of the watchdog register. The time-out period then starts over.

Should the watchdog timer time-out, any value may be written to the watchdog register in order to clear the $\overline{\text{IRQ}}$ pin. A value of 00h will disable the watchdog function until it is again programmed to a new value. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh). The watchdog function is automatically disabled upon power-up, and the watchdog register is cleared.

Note: A WRITE to any clock register will restart the watchdog timer.

3.5 Watchdog output ($\overline{\text{WDO}}$ - M41T65 only)

If the processor does not reset the watchdog timer within the specified period, the watchdog output ($\overline{\text{WDO}}$) will pulse low for t_{rec} (see *Table 7: "Square wave output frequency"*). This output may be connected to the reset input of the processor in order to generate a processor reset. After a watchdog time-out occurs, the timer will remain disabled until such time as a new countdown value is written into the watchdog register.

Note: The crystal oscillator must be running for the $\overline{\text{WDO}}$ pulse to be available. The $\overline{\text{WDO}}$ output is an N-channel, open drain output driver (with I_{OL} as specified in Table 13: "DC characteristics").

3.6 Square wave output (M41T62/64)

The M41T62/64 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 04h establish the square wave output frequency. These frequencies are listed in *Table 7: "Square wave output frequency"*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

The SQW output is an N-channel, open drain output driver for the M41T64, and a full CMOS output driver for the M41T62. The initial power-up default for the SQW output is 32 KHz (except for M41T64, which defaults disabled).

Table 7: Square wave output frequency

Square wave bits				Square wave	
RS3	**RS2**	**RS1**	**RS0**	**Frequency**	**Units**
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.7 Full-time 32 KHz square wave output (M41T64)

The M41T64 offers the user a special 32 KHz square wave function which is enabled on power-up to output on the F_{32K} pin as long as $V_{CC} \geq 1.3$ V, and the oscillator is running (ST bit = '0'). This function is available within one second (typ) of initial power-up and can only be disabled by setting the 32KE bit to '0' or the ST bit to '1.' If not used, the F_{32K} pin should be disconnected and allowed to float.