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M41T81S

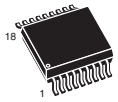
Serial access real-time clock (RTC) with alarms

Datasheet – production data

Features

- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- 32 KHz crystal oscillator with integrated load capacitance (12.5 pf) which provides exceptional oscillator stability and high crystal series resistance operation)
- Oscillator stop detection (monitors clock operation)
- Serial interface supports I^2C bus (400 kHz protocol)
- Ultra-low battery supply current of 0.6 µA (typ)
- 2.0 to 5.5 V clock operating voltage
- Automatic switchover and deselect circuitry (fixed reference) which provides full operation in 3.0 V applications)
- V_{CC} = 2.7 to 5.5 V
- 2.5 V ≤ V_{PFD} ≤ 2.7 V
- Power-down time-stamp (HT bit) which allows determination of time elapsed in battery backup
- Battery low flag
- Programmable alarm and interrupt function (valid even during battery backup mode)
- Accurate programmable watchdog timer (from 62.5 ms to 128 s)
- Software clock calibration (to compensate for crystal deviation due to temperature)
- Operating temperature of –40 to 85 °C
- Package options include an 8-lead SOIC or 18-lead embedded crystal SOIC

SO8
8-pin SOIC



SOX18
18-pin (300 mil) SOIC
with embedded crystal

Contents

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1 Description

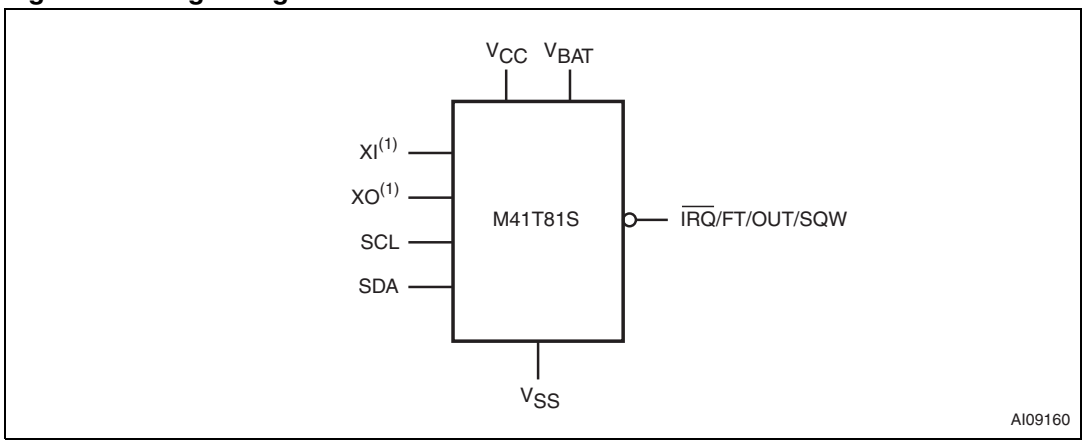
The M41T81S is a low-power serial real-time clock (RTC) with a built-in 32.768 kHz oscillator (external crystal controlled). Eight bytes of the SRAM are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. An additional 12 bytes of SRAM provide status/control of alarm, watchdog and square wave functions. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T81S has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button supply when a power failure occurs. Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, watchdog timer and programmable square wave output. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The M41T81S is supplied in either an 8-pin SOIC or an 18-pin 300 mil SOIC package which includes an embedded 32 KHz crystal.

The 18-pin, embedded crystal SOIC requires only a user-supplied battery to provide non-volatile operation.

Figure 1. Logic diagram



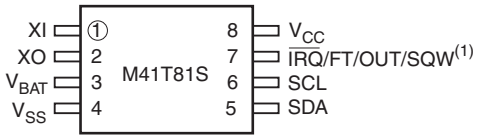
1. For SO8 package only

Table 1. Signal names

XI(1)	Oscillator input
XO(1)	Oscillator output
$\overline{IRQ}$/OUT/FT/SQW	Interrupt / output driver / frequency test / square wave (open drain)
SDA	Serial data input/output
SCL	Serial clock input
V_{BAT}	Battery supply voltage
V_{CC}	Supply voltage
V_{SS}	Ground
NC(2)	No connect
NF(2)	No function

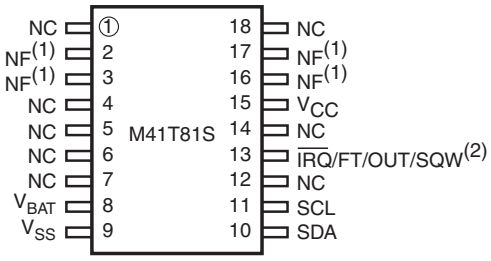
1. For SO8 package only.
2. NC and NF pins should be tied to V_{SS}.

Figure 2. 8-pin SOIC (M) connections



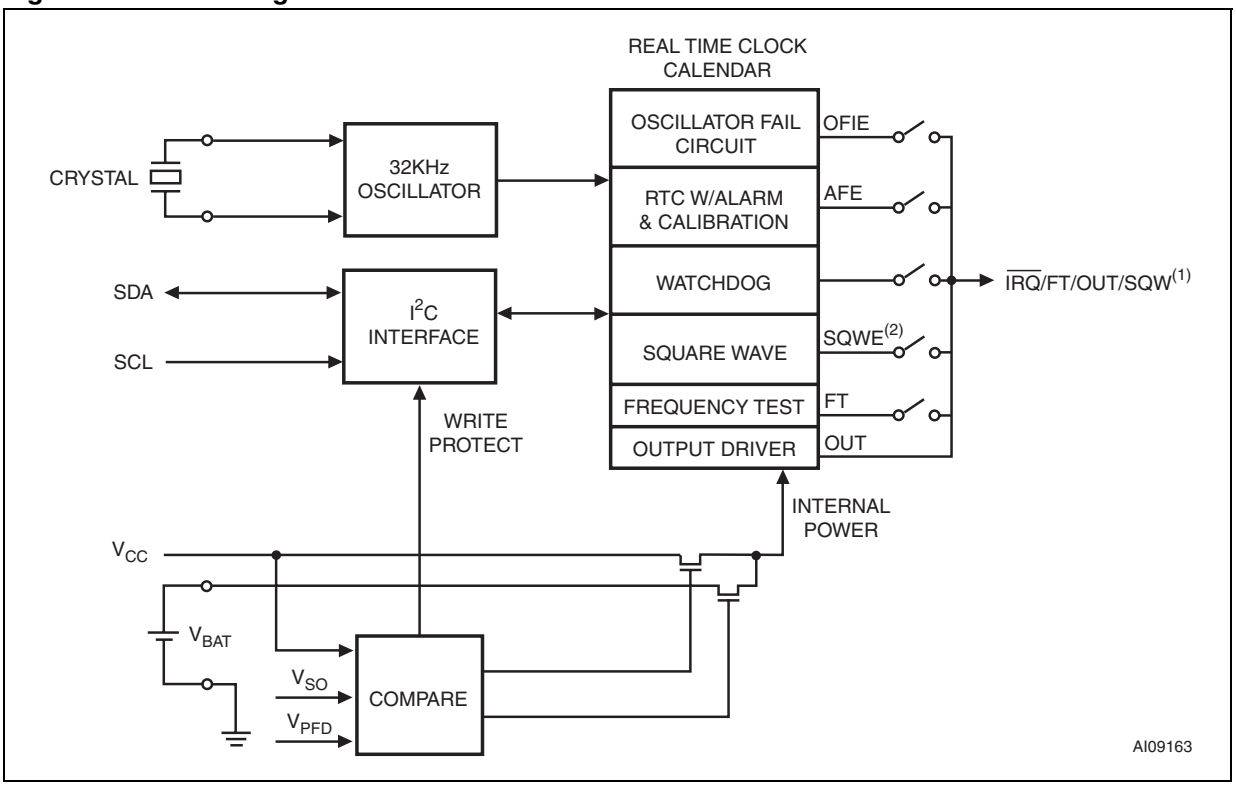
1. Open drain output

Figure 3. 18-pin, 300 mil SOIC (MY) connections



1. NC and NF pins should be tied to V_{SS}. Pins 2 and 3 are internally shorted together. Pins 17 and 16 are internally shorted together.
2. Open drain output

Figure 4. Block diagram



1. Open drain output
2. Square wave function has the highest priority on $\overline{IRQ}$/FT/OUT/SQW output.

2 Operation

The M41T81S clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 20 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/hundredths of a second register
2. Seconds register
3. Minutes register
4. Century/hours register
5. Day register
6. Date register
7. Month register
8. Year register
9. Calibration register
10. Watchdog register

11 - 15. Alarm registers

16. Flags register

17 - 19. Reserved

20. Square wave register

The M41T81S clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. Once V_{CC} falls below the switchover voltage (V_{SO}), the device automatically switches over to the battery and powers down into an ultra-low current mode of operation to preserve battery life. If V_{BAT} is less than V_{PFD}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. If V_{BAT} is greater than V_{PFD}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PFD}. Upon power-up, the device switches from battery to V_{CC} at V_{SO}. When V_{CC} rises above V_{PFD}, it will recognize the inputs.

For more information on battery storage life refer to application note AN1012, "Predicting the battery life and data retention period of NVRAMs and serial RTCs" .

2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain high.

Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this

case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

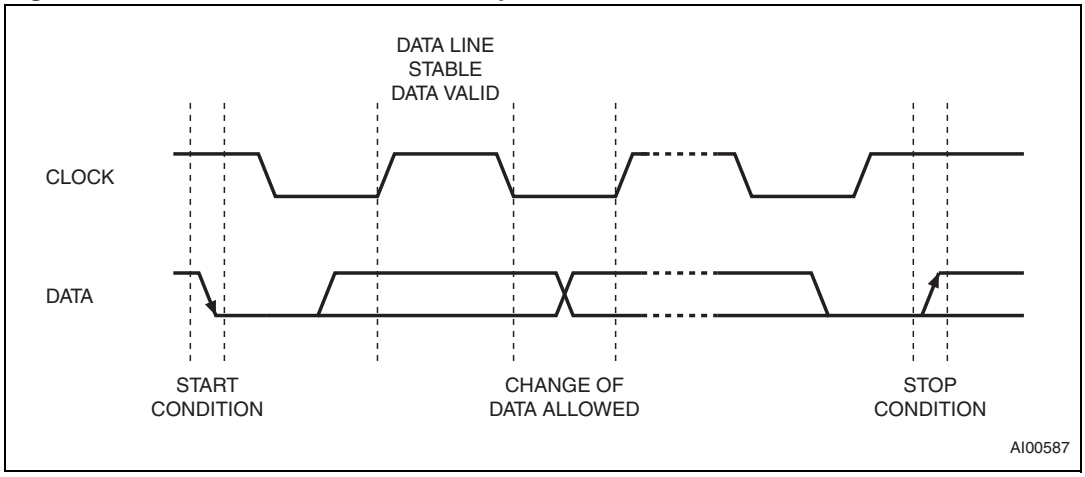
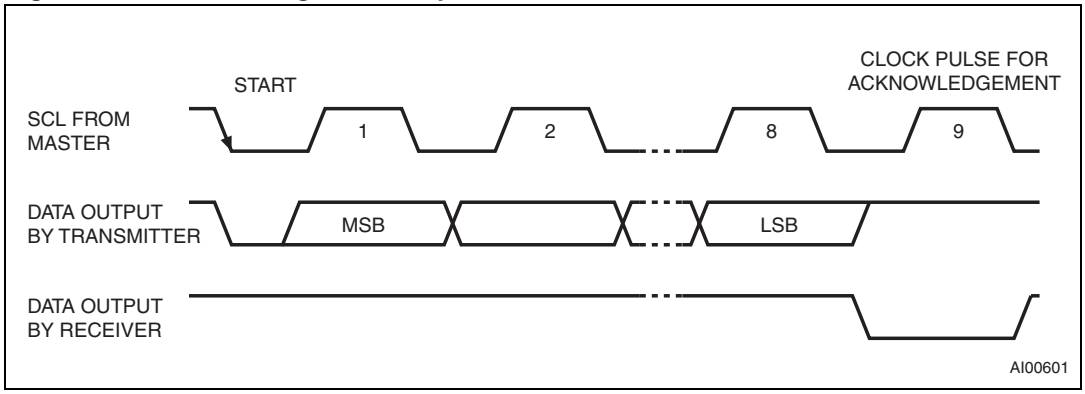


Figure 6. Acknowledgement sequence



READ mode

In this mode the master reads the M41T81S slave after setting the slave address (see *Figure 8 on page 12*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T81S slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (08h-13h).

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41T81S slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 9 on page 12*).

Figure 7. Slave address location

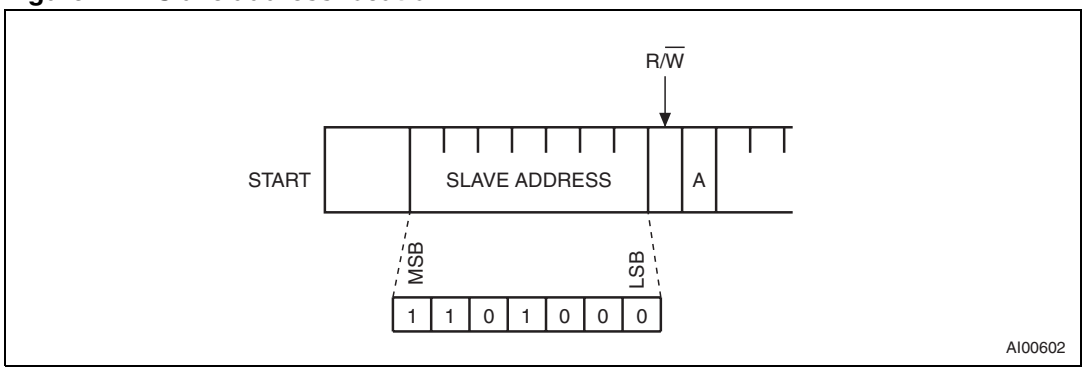


Figure 8. READ mode sequence

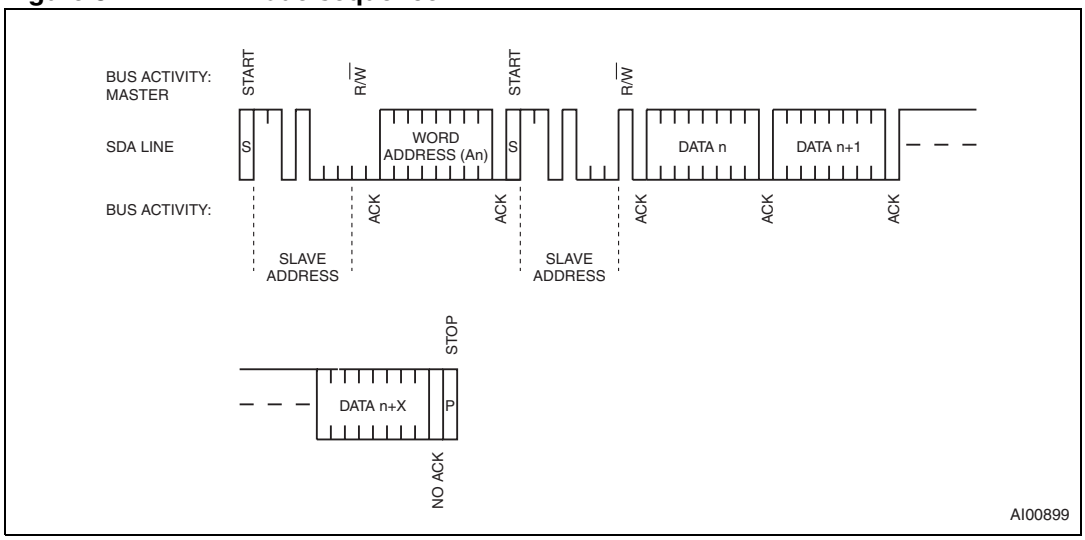
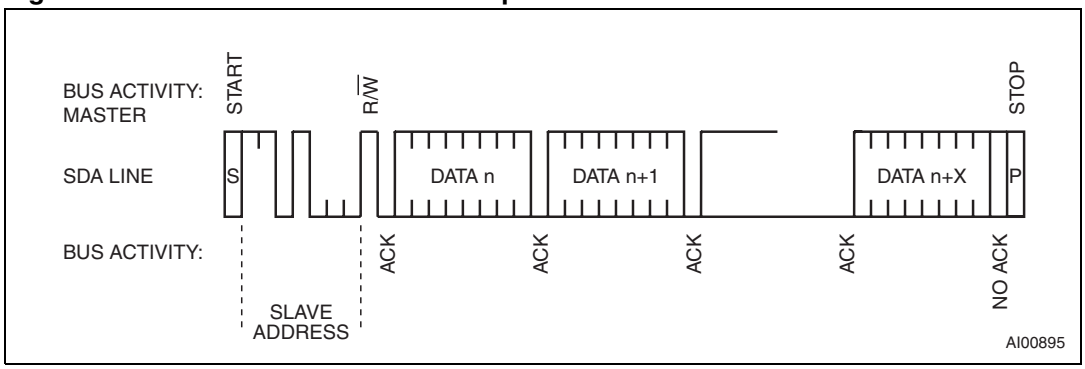


Figure 9. Alternative READ mode sequence



WRITE mode

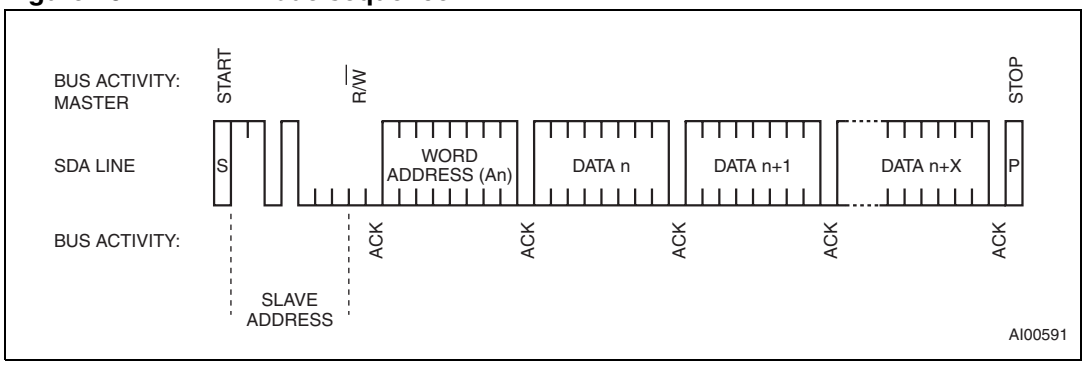
In this mode the master transmitter transmits to the M41T81S slave receiver. Bus protocol is shown in *Figure 10 on page 13*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T81S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see *Figure 7 on page 12* and again after it has received the word address and each data byte.

Data retention mode

With valid V_{CC} applied, the M41T81S can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the power input will be switched from the V_{CC} pin to the battery when V_{CC} falls below the battery backup switchover voltage (V_{SO}). At this time the clock registers will be maintained by the attached battery supply. On power-up, when V_{CC} returns to a nominal value, write protection continues for t_{REC}.

For a further, more detailed review of lifetime calculations, please see application note AN1012.

Figure 10. WRITE mode sequence



3 Clock operation

The 20-byte register map (see *Table 2: Clock register map on page 15*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Note: Tenths/hundredths of seconds cannot be written to any value other than "00."

Bits D6 and D7 of clock register 03h (century/hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month and years. The ninth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

Power-down time-stamp

When a power failure occurs, the HALT (HT) bit will automatically be set to a '1.' This will prevent the clock from updating the registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a '0' will allow the clock to update the registers with the current time. For more information, please refer to AN1572, "Power-down time-stamp function in serial real-time clocks (RTCs)".

Clock registers

The M41T81S offers 20 internal registers which contain clock, alarm, watchdog, flags, square wave and calibration data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to any non-clock address (08h-13h).

Clock and alarm registers store data in BCD. Calibration, watchdog and square wave registers store data in binary format.

Table 2. Clock register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 Seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 hours		Hours (24-hour format)				Century/hours	0-1/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQW	ABE	AI	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	HT	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	BL	0	OF	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

0 = Must be set to '0'

ABE = Alarm in battery backup mode enable bit

AF = Alarm flag (read only)

AFE = Alarm flag enable flag

BL = Battery low bit

BMB0-BMB4 = Watchdog multiplier bits

CB = Century bit

CEB = Century enable bit

FT = Frequency test bit

HT = Halt update bit

OF = Oscillator fail flag

OFIE = Oscillator fail interrupt enable

OUT = Output level

RB0-RB1 = Watchdog resolution bits

RPT1-RPT5 = Alarm repeat mode bits

RS0-RS3 = SQW frequency

S = Sign bit

SQWE = Square wave enable

ST = Stop bit

WDF = Watchdog flag (read only)

Calibrating the clock

The M41T81S is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about +1.9 to –1.1 minutes per month (see *Figure 11 on page 17*). When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature. The M41T81S design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 12 on page 17*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the calibration register 08h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register (see *Figure 12 on page 17*). Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T81S may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT/OUT/SQW pin. The pin will toggle at 512 Hz, when the stop bit (ST, D7 of 01h) is '0,' the frequency test bit (FT, D6 of 08h) is '1,' the alarm flag enable bit (AFE, D7 of 0Ah) is '0,' and the square wave enable bit (SQWE, D6 of 0Ah) is '0' and the watchdog register (09h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{IRQ}$/FT/OUT/SQW pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500-10 k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 11. Crystal accuracy across temperature

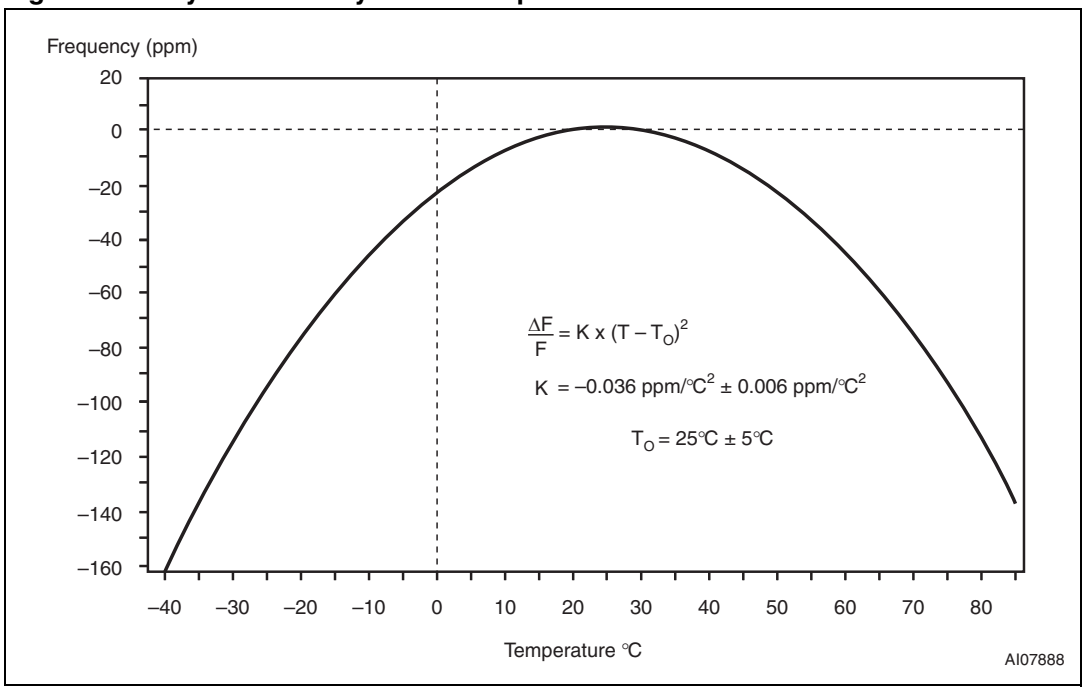
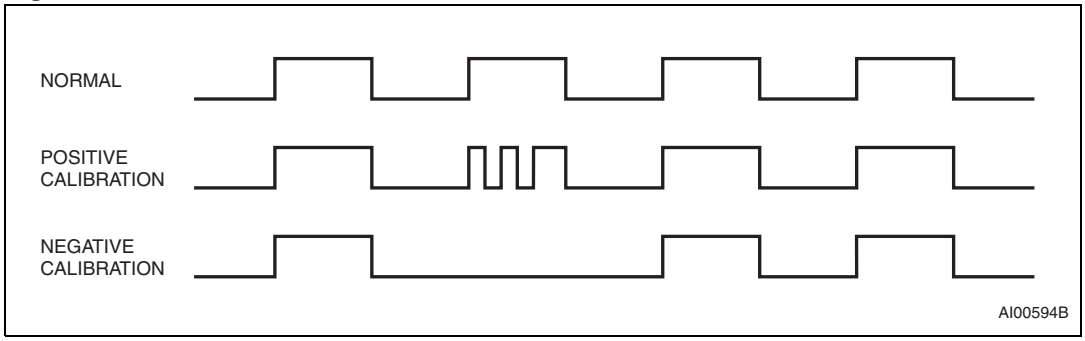


Figure 12. Clock calibration



Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41T81S is in the battery backup mode to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 3 on page 19* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set (and SQWE is '0.'), the alarm condition activates the $\overline{IRQ}$/FT/OUT/SQW pin.

Note: If the address pointer is allowed to increment to the flags register address, an alarm condition will not cause the Interrupt/Flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{IRQ}$/FT/OUT/SQW output is cleared by a READ to the flags register as shown in *Figure 13*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{IRQ}$/FT/OUT/SQW pin can also be activated in the battery backup mode. The $\overline{IRQ}$/FT/OUT/SQW will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. *Figure 14* illustrates the backup mode alarm timing.

Figure 13. Alarm interrupt reset waveform

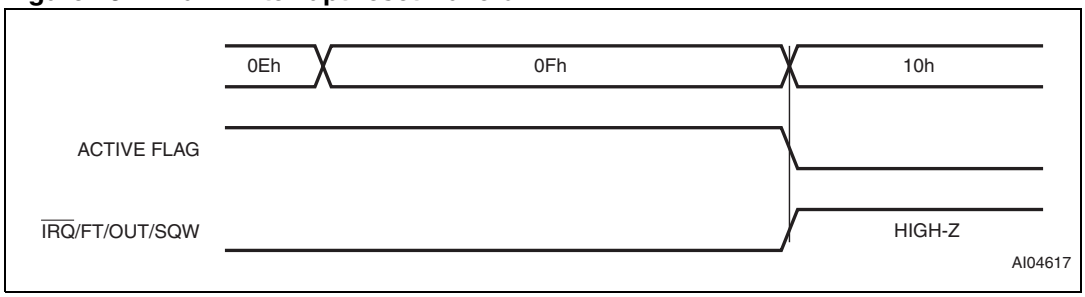


Figure 14. Backup mode alarm waveform

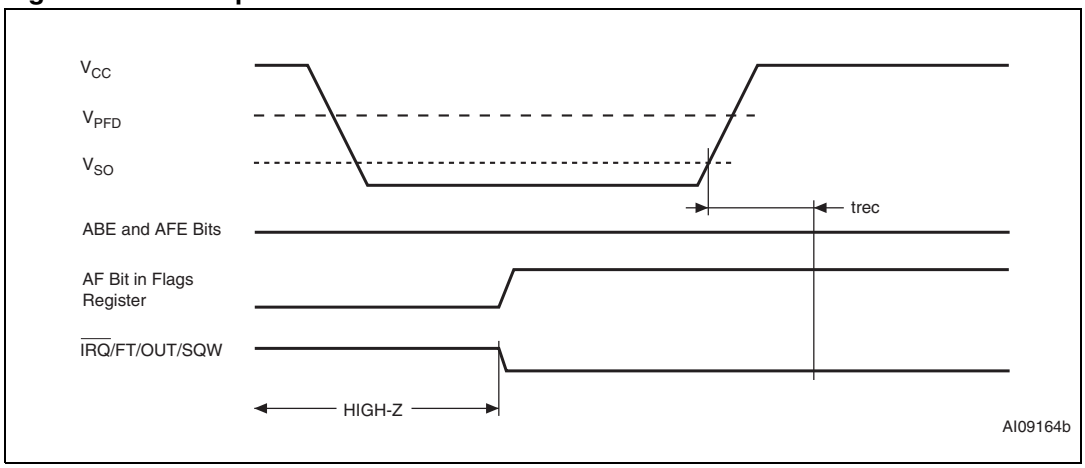


Table 3. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1, or 3 seconds). If the processor does not reset the timer within the specified period, the M41T81S sets the WDF (watchdog flag) and generates a watchdog interrupt.

The watchdog timer can be reset by having the microprocessor perform a WRITE of the watchdog register. The time-out period then starts over.

Should the watchdog timer time-out, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{\text{IRQ}}$/FT/OUT/SQW pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared. If the watchdog function is set, the frequency test function is activated, and the SQWE bit is '0,' the watchdog function prevails and the frequency test function is denied.

Square wave output

The M41T81S offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 4*. Once the selection of the SQW frequency has been completed, the $\overline{IRQ}$/FT/OUT/SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Table 4. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	-
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

Century bit

Bits D7 and D6 of clock register 03h contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Battery low warning

The M41T81S automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity. Clock data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced.

The M41T81S only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

Oscillator fail detection

If the oscillator fail bit (OF) is internally set to '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator.

The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).
- The voltage present on V_{CC} is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal.

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to '0.'

Oscillator fail interrupt enable

If the oscillator fail interrupt bit (OFIE) is set to a '1,' the $\overline{IRQ}$ pin will also be activated. The $\overline{IRQ}$ output is cleared by resetting the OFIE or OF bit to '0' (not be reading the flags register).

Output driver pin

When the FT bit, AFE bit, SQWE bit, and watchdog register are not set, the $\overline{IRQ}$/FT/OUT/SQW pin becomes an output driver that reflects the contents of D7 of the calibration register. In other words, when D7 (OUT bit) and D6 (FT bit) of address location 08h are a '0,' then the $\overline{IRQ}$/FT/OUT/SQW pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT/SQW pin is an open drain which requires an external pull-up resistor.

Preferred initial power-on default

Upon initial application of power to the device, the following register bits are set to a '0' state: watchdog register; AFE; ABE; SQWE; OFIE; and FT. The following bits are set to a '1' state: ST; OUT; OF; and HT (see *Table 5*).

Table 5. Preferred default values

Condition	ST	HT	Out	FT	AFE	SQWE	ABE	WATCHDOG register(1)	OF	OFIE
Initial power-up(2)	1	1	1	0	0	0	0	0	1	0
Subsequent power-up (with battery backup)(3)	UC	1	UC	0	UC	UC	UC	0	UC	UC

1. BMB0-BMB4, RB0, RB1
2. State of other control bits undefined
3. UC = Unchanged

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Sym	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 7	V
T_{SLD}	Lead solder temperature for 10 seconds	SO8(1)	260	°C
		SOX18(2)	240	°C
V_{IO}	Input or output voltages		–0.3 to V_{CC} + 0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For SO8 package, Lead-free (Pb-free) lead finish, reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. For SOX18 package, reflow at peak temperature of 240 °C. The time above 235 °C must not exceed 20 seconds.

Caution: Negative undershoots below –0.3 volts are not allowed on any pin while in the battery backup mode.

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC measurement conditions

Parameter	M41T81S
Supply voltage (V_{CC})	2.7 to 5.5 V
Ambient operating temperature (T_A)	–40 to 85 °C
Load capacitance (C_L)	100 pF
Input rise and fall times	≤ 50 ns
Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 15. AC measurement I/O waveform

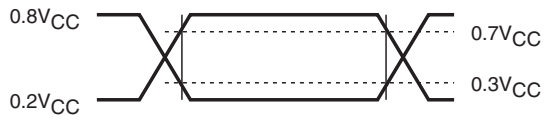


Table 8. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	7	pF
C_{OUT}[3]	Output capacitance	-	10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)	-	50	ns

1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz
3. Outputs deselected

Table 9. DC characteristics

Sym	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	0 V ≤ V_{IN} ≤ V_{CC}			±1	µA
I_{LO}	Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC}			±1	µA
I_{CC1}	Supply current	Switch freq = 400 kHz			400	µA
I_{CC2}	Supply current (standby)	SCL = 0 Hz All inputs ≥ V_{CC} – 0.2 V ≤ V_{SS} + 0.2 V			100	µA
V_{IL}	Input low voltage		–0.3		$0.3V_{CC}$	V
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 3.0 mA			0.4	V
	Output low voltage (open drain)(2)	I_{OL} = 10 mA			0.4	V
	Pull-up supply voltage (open drain)	$\overline{IRQ}$/OUT/FT/SQW			5.5	V
V_{BAT}(3)	Backup supply voltage		2.0		3.5(4)	V
I_{BAT}	Battery supply current	T_A = 25 °C, V_{CC} = 0 V Oscillator ON, V_{BAT} = 3 V		0.6	1	µA

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 2.7 to 5.5 V (except where noted).
2. For $\overline{IRQ}$/FT/OUT/SQW pin (open drain)
3. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.
4. For rechargeable back-up, V_{BAT} (max) may be considered to be V_{CC}.

Table 10. Crystal electrical characteristics

Sym	Parameter(1)and(2)	Min	Typ	Max	Units
f_O	Resonant frequency	-	32.768		kHz
R_S	Series resistance	-		60(3)	kΩ
C_L	Load capacitance	-	12.5		pF

1. Externally supplied if using the SO8 package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.
2. Load capacitors are integrated within the M41T81S. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. For applications requiring back-up supply operation below 2.5 V, R_S (max) should be considered 40 kΩ.

Figure 16. Power down/up mode AC waveforms